High Efficiency Buck-Boost Converter with Three Modes Selection for HV Applications using 0.18 μm Technology

Fouad Farah[*†], **Mustapha El Alaoui**[*], **Abdelali El Boutahiri**[*], **Mounir Ouremchi**[*], **Karim El Khadiri**[**], **Ahmed Tahiri**[**], and **Hassan Qjidaa**[*], Non-members

ABSTRACT

In this paper, we aim to make a detailed study on the evaluation and the characteristics of the non-inverting buck–boost converter. In order to improve the behaviour of the buck-boost converter for the three operating modes, we propose an architecture based on peak current-control. Using a three modes selection circuit and a soft start circuit, this converter is able to expand the power conversion efficiency and reduce inrush current at the feedback loop. The proposed converter is designed to operate with a variable output voltage. In addition, we use LDMOS transistors with low on-resistance, which are adequate for HV applications. The obtained results show that the proposed buck-boost converter performs perfectly compared to other architectures and it is successfully implemented using 0.18 μm CMOS TSMC technology, with an output voltage regulated to 12 V and input voltage range of 4–20 V. The power conversion efficiency for the three operating modes buck, boost and buck-boost are 97.6%, 96.3% and 95.5% respectively at load current of 4 A.

Keywords: Buck-Boost Converter, Three Modes Selection, High Efficiency, Soft Start, Li-Ion Batteries

1. INTRODUCTION

Recently, the automotive sector has experienced a very remarkable revolution in the production of electric vehicles, in accordance with the global policy on the application of renewable energies and alternative energies. In this respect, the electric vehicle represents a large field of research concerning its operation, its autonomy, batteries used and also its impact on the environment. Among the batteries used in electric vehicles are the lithium-ion batteries; they promise increased storage capacity, high efficiency, lower cost, greater durability and even faster charging [1]. Energy management systems have become a major element in the charge process of the Li-ion battery; these systems should be able to sufficiently cover the battery output voltage for application systems. In [2–4], the architecture used is based on LDO regulator which offers high accuracy, fast charging, and high integration.

But this charging circuit has a major disadvantage which is low power efficiency caused by the time lag between power supply and battery voltage V_{BAT}. On the other hand, the charging circuits in [5–10] such as switching capacitors, switching mode power supply or DC-DC converter are typified by high efficiency. However, these structures are not appropriate for integration in a single chip and also, they have low accuracy.

The four switches dc-dc converter (Fig. 1) is widely used as a power management system for Li-ion batteries either as buck, boost or buck-boost mode because of its high efficiency [9, 12]. However, buck-boost converters suffer from a lower efficiency compared with buck or boost, and this is due to several factors: switching loss (number of switches twice than that in buck or boost), and integration and design of two control loops (current or voltage) is complex. Additionally, the conduction loss of a buck-boost is higher than that of other modes. In this paper, a peak current-control non-inverting buck-boost converter is designed to provide a stable and unruffled mode transition. The proposed architecture is based on the current mode control, it represents a simple compensation, fast dynamic response, improved regulation, and over-current protection compared with the voltage mode control. In addition, a three modes selection circuit is proposed to control the operating mode transition; also, a soft start circuit is used to decrease the inrush current at the feedback loop.

This paper is planned as follows: in Section 2, the architecture and circuits description are presented. Results and discussion are shown in Section 3 and finally, conclusion is giving in Section 4.

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[*]The authors are with the Department of physics FSDM, Sidi Mohamed Ben Abdellah University, Fez, Morocco.

[**]The author is with the Laboratory of Computer Science and Interdisciplinary Physics ENS, Sidi Mohamed Ben Abdellah University, Fez, Morocco.

[†]Corresponding author. E-mail: fouad.farah@usmba.ac.ma

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Table 1: *Operation of the buck-boost converter.*

Switches	Inductance mode	Buck mode	Boost mode	Buck-boost mode
S_1	Inductor charge	ON	ON	ON
	Inductor discharge	OFF	ON	OFF
S_2	Inductor charge	OFF	OFF	ON
	Inductor discharge	ON	OFF	OFF
S_3	Inductor charge	OFF	ON	ON
	Inductor discharge	OFF	OFF	OFF
S_4	Inductor charge	ON	OFF	OFF
	Inductor discharge	ON	ON	ON
Average load voltage		$V_{out} = DV_s$	$V_{out} = \frac{1}{1-D}V_s$	$V_{out} = \frac{D}{1-D}V_s$

2. ARCHITECTURE AND CIRCUITS DESCRIPTION

2.1 Architecture

As shown in Fig. 1, the non-inverting buck-boost converter can increase or decrease the supply voltage according to the output needs. However, when the input signal V_{in} is lower than that of the output V_{out}, the converter is operating in boost mode: transistor S_1 is always ON and S_2 is always OFF. This operating mode is achieved by controlling power switches S_3 and S_4. On the other side, when V_{in} is higher than V_{out}, the converter is operating in buck mode: transistor S_4 is always ON and S_3 is always OFF, the conductor is charging and discharging by switching the power transistors S_1 and S_2. The last state is when the input V_{in} is close to the required voltage, the converter is operating in buck-boost mode. In this case, all the transistors are activated to make two groups, (S_1-S_3) and (S_2-S_4) in order to control the inductor cycle (charge, discharge). The different states of the transistors, inductor charge and discharge and the output voltage are given in Table 1.

The proposed architecture of the peak current-control buck-boost converter is given in Fig. 2. The power stage is composed of four LDMOS power transistors (S_1, S_2, S_3 and S_4) [13], an output capacitor, an inductor and peak current controller feedback. The signals (V_{S1}–V_{S4}) are generated by the driver blocks to control the switching activities of the transistors (S_1–S_4). A three modes selection circuit is used to select the operating mode for buck, boost or buck-boost considering the input and output voltages.

The soft-start circuit is designed to decrease the inrush current at the feedback loop. Additionally, a control logic block is used to generate the main control signals V_{Buck} and V_{Boost}. Finally, a ramp generator and a bandgap reference (BGR) are utilized to provide the ramp signal and the reference voltage, respectively.

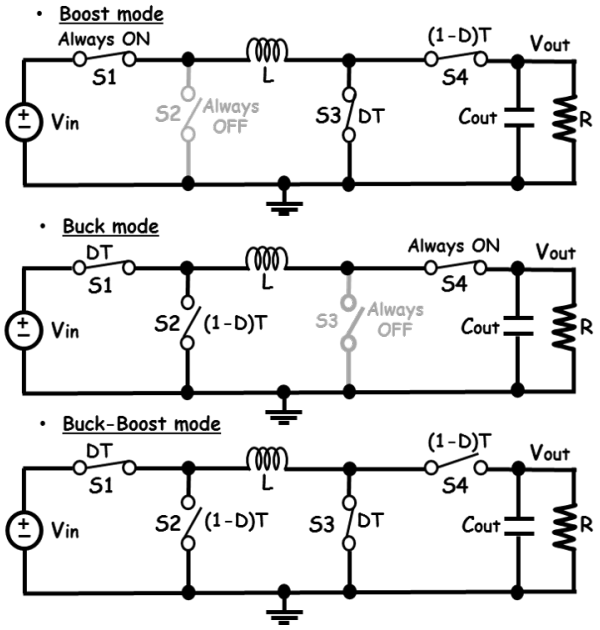


Fig.1: *Buck-boost converter states.*

2.2 Circuits Description

To solve the problem of efficiency regarding the buck-boost converter, several studies have been published in literature [14–16]. In this approach [14], they used an architecture with fixed output voltage, which is not applicable with variable output. [15] used a constant ramp and a level-shifted error voltage. But this approach is inapplicable to current controlled mode. Additional study to control the buck-boost converter based on the digital control is proposed in [16]. However, this method is not able to work with higher load current condition. Therefore, to have a fast system with high integration, able to work in low or high load current condition and especially with high efficiency, we propose a three modes selection circuit (Fig. 3). The output voltage V_{out} is divided into two voltages V_L and V_H and V_{in} into V_1; their equations are proportional to W/L ratio such as:

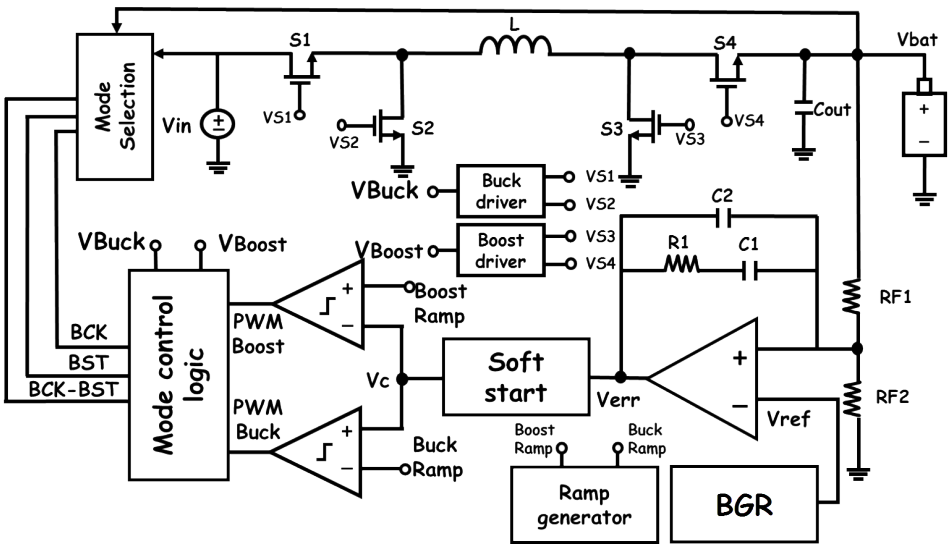


Fig.2: *Block diagram of the proposed buck-Boost converter.*

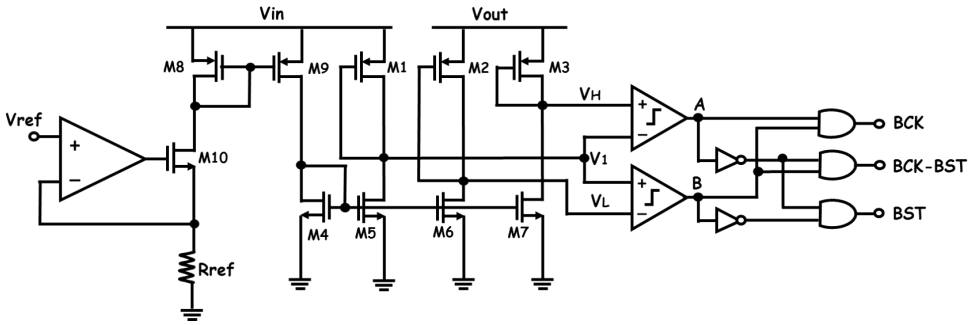


Fig.3: *The proposed three modes selection circuit.*

$$V_1 = V_{in} - |V_{TH}| - \sqrt{\frac{2I_B}{\mu_P C_{ox}\,(W/L)_{M_1}}} \quad (1)$$

$$V_L = V_{out} - |V_{TH}| - \sqrt{\frac{2I_B}{\mu_P C_{ox}\,(W/L)_{M_2}}} \quad (2)$$

$$V_H = V_{out} - |V_{TH}| - \sqrt{\frac{2I_B}{\mu_P C_{ox}\,(W/L)_{M_3}}} \quad (3)$$

where V_{TH} is the threshold voltage, I_B is the bias current, W/L is the aspect ratio, and $\mu_P C_{ox}$ is the mobility and gate capacitance per unit area.

The three modes selection circuit is designed to work with two blocks, one to generate the comparison signals V_1, V_L and V_H in order to have, $V_L < V_H$ and V_1 between V_L and V_H when input voltage V_{in} is equal to V_{out}, and the second, to provide the selection signals BCK, BST and BCK-BST. As shown in Fig. 3 the circuit works in three states BCK, BST and BCK-BST which represent modes buck, boost, and buck boost respectively.

- State 1: $V_1 < V_L < V_H$

We start by comparing the input voltage V_{in} with output voltage V_{out}. In this state V_{in} is much lower than V_{out}, so the converter will be operating in boost mode and this implies that BST turns into high and the both signals BCK and BST-BCK into low.

- State 2: $V_L < V_1 < V_H$

In this state V_{in} is close or equal to V_{out}; the converter will be working in buck-boost mode. In this case, BCK-BST turns into high and the signals BCK and BST into low.

- State 3: $V_L < V_H < V_1$

When V_{in} increments until it becomes higher than V_{out}, so the converter is set to the buck mode. Therefore, the BCK switches into high and the signals BST and BCK- BST into low.

The values of the three selection signals BCK, BST and BCK-BST depend on the outputs A and B of the two comparators such as:

$$BCK = A \oplus B \quad (4)$$

$$BST = \overline{A} \oplus \overline{B} \quad (5)$$

$$BCK - BST = \overline{A} \oplus B \quad (6)$$

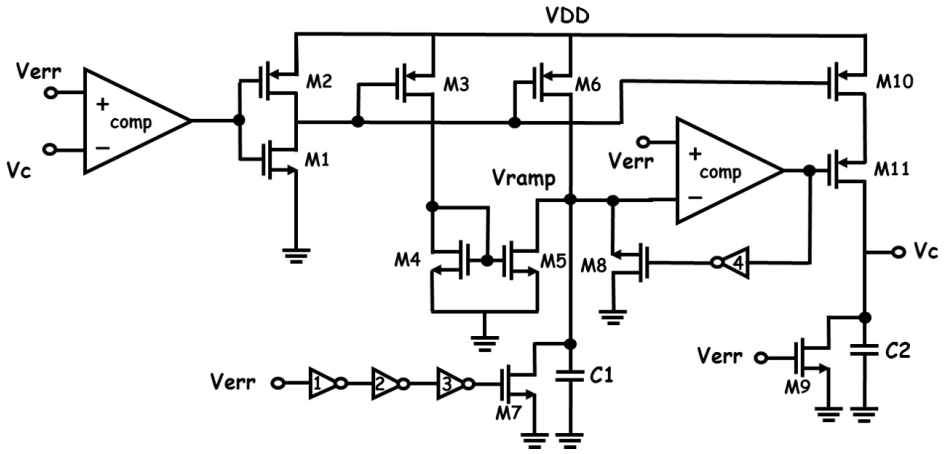


Fig.4: *Soft start circuit.*

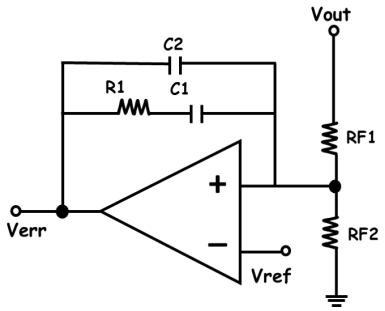


Fig.5: *The type-II compensation circuit.*

In our study, the operation range of the buck–boost mode is regulated to ±150 mV higher and lower than required output voltage.

2.2.1 Soft start circuit

During the operation of the DC-DC buck-boost converter, a perturbation current is present called inrush current. This current is caused by several factors: buck-boost converter environment, transistors switching and input variation. The inrush current generates undesirable effects such as radiated and conducted electromagnetic interference [17]. Furthermore, this current represents a major disadvantage that can disrupt the battery charge as it can reduce the efficiency of the system. However, to solve the inrush current problem, it is necessary to apply a simple circuit which can adapt with the input variation.

Fig. 4 shows the soft start circuit. It is composed of two blocks, one for providing the ramp voltage V_{ramp} and the other one for comparing that with the error voltage V_{err}, in order to charge and discharge the capacitors C_1 and C_2 and get the soft start time. Before starting this operation, we have to reset the output voltage V_C by switching on M_7 and M_9 transistors. C_1 and C_2 are discharged.

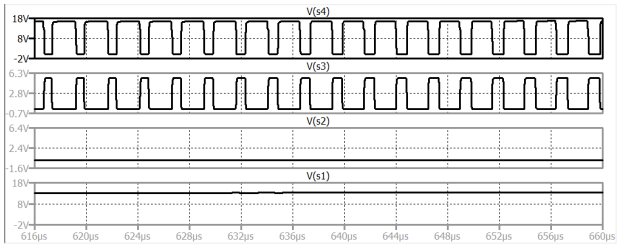
In initial state V_{err} is higher than V_C which provides current for transistors M_3, M_{10} and M_6. The value of aspect ratio (W/L) of M_4 and M_5 are predefined to set the ratio of current I_{drain} $(M_5,\ M_6)$ to α. When α reaches 1, a microampere order current is provided in the capacitor C_1, then V_{ramp} begins to increase. Once V_{ramp} is higher than V_{err}, the ramp voltage switchs to a lower state and activates the transistor M_{11} to charge C_2. Thereafter, the transistor M_8 turns on by the reverse voltage of V_{ramp} through inverter 4, then V_{err} gets higher than V_{ramp}, M_{11} switches off and C_2 stops charging. On the other hand, the voltage V_{err} increases during the charging time. When the transistor M_8 is turned off, C_1 begins charging with a low current. Once V_C surpasses V_{err}, the transistors M_3, M_{10} and M_6 switch off. Finally, the soft start time is provided using a simple technique.

2.2.2 Compensation circuit and Ramp generator

The compensation circuit used in this work is type-II, it represents a typical compensation for the peak-current controlled converters. The main role of this circuit is to assure a stable operation for the three modes of operation buck, boost and buck-boost. The type-II compensation circuit (Fig. 5) is broadly used in the literature [18, 19]. It is composed of an amplifier, two capacitors, resistors and divider point. The transfer function of the compensation circuit is giving by:

$$\frac{V_{err}}{V_{out}} = \frac{1 + sR_2C_1}{sR_{F1}\left(C_1 + C_2\right)\left(1 + sR_2\dfrac{C_1C_2}{C_1 + C_2}\right)} \tag{7}$$

We used a ramp generator which is already published by our team in [6]. The same circuit is implemented and adapted with high voltage in order to provide a symmetry ramp signal.



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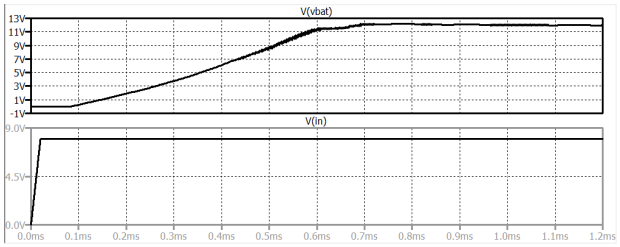
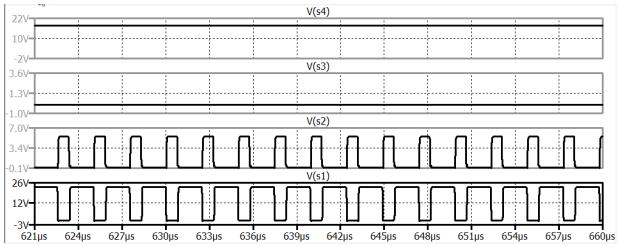
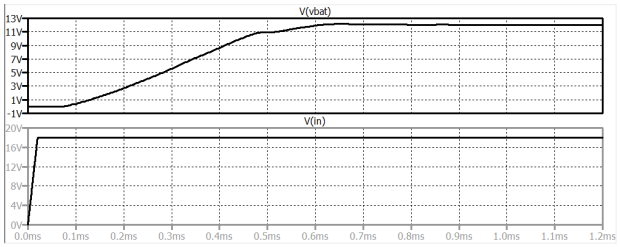


(b)

Fig.6: *(a) Control signals waveforms for boost mode and (b) input voltage ($V_{in} = 8\ V$) and output voltage ($V_{out} = 12.05\ V$).*



(a)



(b)

Fig.7: *(a) Control signals waveforms for buck mode and (b) input voltage ($V_{in} = 18\ V$) and output voltage ($V_{out} = 12.05\ V$).*

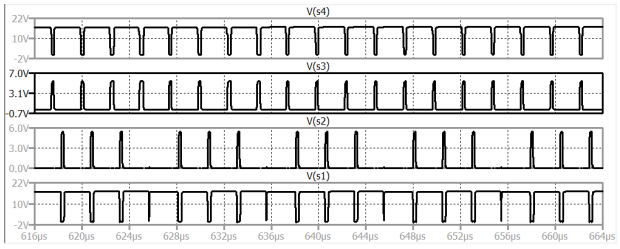
3. RESULTS AND DISCUSSIONS

The proposed non-inverter converter is designed in 0.18 μm CMOS TSMC technology. The measurement results of our buck boost converter are shown in the following Figs. 6, 7, and 8. The simulations are presented in three operating modes: buck, boost and buck-boost, where the output voltage desired is 12 V. The control voltages of each transistor for boost operating mode are shown in Fig. 6(a). As we already said in Section 2, once the selection mode BST is activated, the transistor S_1 is always ON and S_2 is always OFF and the switching activities are in transistors S_3 and S_4. The converter output is 12 V even when the input voltage is 8 V. Fig. 6(b) present input and output voltage.

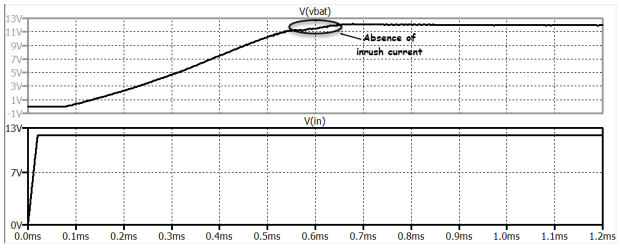
Figs. 7(a) and (b) show control voltages of each transistor for buck operating mode and input and output voltage respectively. Once the selection mode BCK is activated, transistor S_4 is always ON and S_3 is always OFF and the switching activities are in transistors S_1 and S_2. The converter input drops from 18 V to the desired output 12 V.

Figs. 8(a) and (b) show control voltages of each transistor for buck-boost mode and input and output voltage respectably. Once the input voltage is near to the output, the selection mode BCK-BST is activated and all transistors switch in order to regulate the output voltage at 12 V.

The power conversion efficiency of the proposed buck-boost converter is presented in Fig. 9. The proposed buck–boost shows high efficiency for the three operating modes buck, boost or buck–boost. As shown in Fig. 9, our converter operates in three input voltages, for buck mode the power efficiency is



(a)



(b)

Fig.8: *(a) Control signals waveforms for buck-boost mode and (b) input voltage ($V_{in} = 12\ V$) and output voltage ($V_{out} = 12.05\ V$).*

97.5%, for boost mode it equal to 96.5% and even for the buck-boost mode we have high efficiency of 95.5% at load current of 4A.

As expected, the obtained results are much better compared with other works. However, the developed techniques of three modes selection and soft start circuit presents an excellent solution to control the mode transition, to have a stable output signal (phase margin equal to 63.42° presented in Fig. 10) without inrush current and furthermore to enhance the converter efficiency. Table 2 shows a comparison of

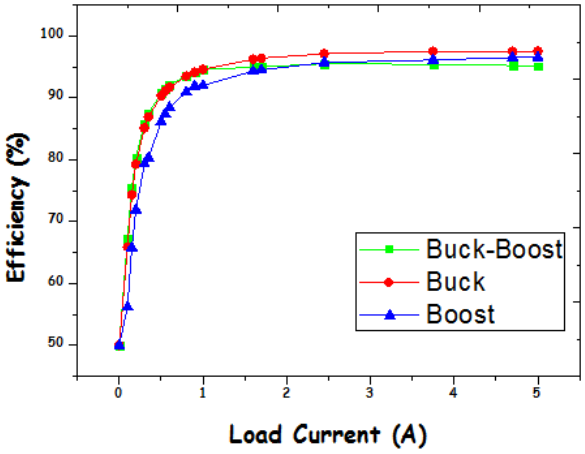
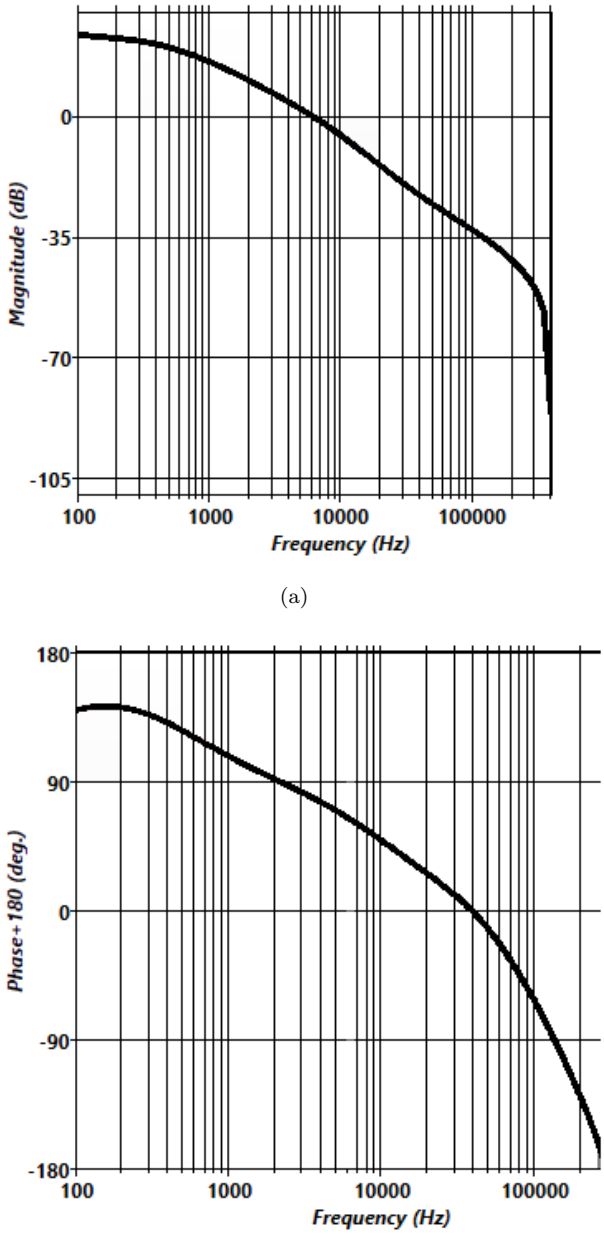


Fig.9: *Power efficiency of the proposed DC-DC converter for the three operating modes. In boost mode,* $V_{in} = 8\ V$ *and* $V_{out} = 12.05\ V$. *In buck mode,* $V_{in} = 18\ V$ *and* $V_{out} = 12.05\ V$. *In buck-boost mode,* $V_{in} = 12\ V$ *and* $V_{out} = 12.05\ V$.

Table 2: *Comparison of performances with other works.*

	[9]	[11]	This work
Technology (μm)	0.18	0.18	0.18
Modes	Buck-boost	Buck-boost	Buck-boost
Efficiency (%)	91	94.8	95.5
Switching Freq (MHz)	2.5	3.2	2.5
Input range (V)	2.7–5.7	3–8	4–20
Output (V)	5	5	12

the proposed architecture with previous buck–boost converters with similar specifications. The approach [9] leads to a high leakage current at the transistors disabled during the light load current mode. This reduces the efficiency of the converter. In [11], a self-tracking zero current detector was proposed to minimize the time error when the current of the inductor came to zero and improved the efficiency of the converter. However, the efficiency of those structures is still not enough when the load becomes extremely low; for this condition the power loss of the feedback loop is serious. Compared with [9,11], the power conversion efficiency of the proposed converter is higher, due to use of LDMOS Switches with low on-resistance to reduce the power loss. In addition, the proposed three modes selection allows the converter to work in the buck–boost mode in the narrow input voltage range to avoid the lower efficiency.



(a)

(b)

Fig.10: *Simulation of the frequency responses of the proposed converter for buck-boost mode:* $V_{in} = 12\ V$ *and* $V_{out} = 12.05\ V$, *(a) gain response (dB) and (b) phase margin response (deg).*

4. CONCLUSION

In conclusion, the proposed architecture represents a good choice for automotive systems as an energy management system. The proposed converter is able to switch from one operating mode to another without reducing its efficiency, and also it can perform for a high range of input voltages from 4 V to 20 V using the proposed three modes selection circuit. For fixed output voltage of 12 V, the results of simulations of the proposed buck-boost converter confirm the cor-

rect operation and the high-power efficiency of our converter. The circuit is designed in 0.18 μm CMOS TSMC technology. The power conversion efficiency is higher for the three operating modes and for different load current.

It appears that:

- The buck-boost converter can perform with high power efficiency in the three operating modes: 97.5% for buck mode, 96.5% for boost mode, and 95.5% for buck-boost mode.
- The buck-boost converter can work with variable output from 3 V to 25 V due to the three modes selection.
- The obtained output voltages are presented in the above figures without any inrush current.

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Fouad Farah received his Master degree in Microelectronics from Faculty of Sciences Dhar EL Mahraz, Fez, Morocco, in 2016. He is now a Ph.D. student in the Department of Physics, Sidi Mohammed Ben Abdellah University, Fez, Morocco, LESSI laboratory. His main research interest includes renewable energy, switch mode audio amplifier, CMOS mixed-mode integrated circuit design, design techniques for RFID, Li-ion battery charger, and power management.

Mustapha El Alaoui received his Master degree in Microelectronics from Faculty of Sciences Dhar EL Mahraz, Fez, Morocco, in 2017. He is now a Ph.D. student in the Department of Physics, Sidi Mohammed Ben Abdellah University, Fez, Morocco, LESSI laboratory. His main research interest includes renewable energy, switch mode audio amplifier, CMOS mixed-mode integrated circuit design, design techniques for RFID, Li-ion battery charger, and power management.

Abdelali El Boutahiri received his Master degree in Microelectronics from Faculty of Sciences Dhar EL Mahraz, Fez, Morocco, in 2017. He is now a Ph.D. student in the Department of Physics, Sidi Mohammed Ben Abdellah University, Fez, Morocco, LESSI laboratory. His main research interest includes renewable energy, switch mode audio amplifier, CMOS mixed-mode integrated circuit design, design techniques for RFID, Li-ion battery charger, and power management.

Mounir Ouremchi received his Master degree in Microelectronics from Faculty of Sciences Dhar EL Mahraz, Fez, Morocco, in 2018. He is now a Ph.D. student in the Department of Physics, Sidi Mohammed Ben Abdellah University, Fez, Morocco, LESSI laboratory. His main research interest includes renewable energy, switch mode audio amplifier, CMOS mixed-mode integrated circuit design, design techniques for RFID, Li-ion battery charger, and power management.

Karim El Khadiri received M.Sc. and Ph.D. degrees in Faculty of Sciences from Sidi Mohammed Ben Abdellah University in 2011 and 2017, respectively. Since 2012, he served as a Research Scientist at Faculty of Science in the University of Sidi Mohammed Ben Abdellah, Fez, Morocco and Guest Researcher at LIMA laboratory in UQO Canada. He is now a Professor in Superior Normal School, ENS-FEZ, Morocco. His current interests include switch mode audio amplifier, CMOS mixed-mode integrated circuit design, design techniques for RFID, RF front-ends for passive tags, Li-ion battery charger, and power management.

Ahmed Tahiri received the graduate degree DES in Department of Physics, Sidi Mohammed Ben Abdellah University, Morocco in 1997, received the Ph.D. degree in Physics from the University Sidi Mohamed Ben Abdellah, Faculty of Science, Morocco in 2005. He completed his doctoral studies in Didactics of Science in the University of Sherbrooke in Canada in 2010. He is now a Professor in Superior Normal School, ENS-FEZ, Morocco. His research interests include image processing, computer science, and didactics of scientific disciplines.

Hassan Qjidaa received the M.S. and Ph.D. degrees in Electrical Engineering from Nuclear Physics Institute of Lyon, in France 1984 and 1987, respectively. Since 1987, he served as a Research Scientist at Faculty of Science in the University of Sidi Mohammed Ben Abdellah, Fez, Morocco. He has been a Professor with the Department of Physics. He is currently also a Director of the Information Analysis and Micro-system Teams (IAMS), and Vice Director of the electronic signal and systems laboratory (LESSI). His current research interests are in image processing, pattern recognition, data analysis, machine intelligence, low-power circuit design techniques for RFID, RF front-ends for passive tags, and CMOS mixed-mode integrated circuit design.