An FPGA Based Novel Digital Controller for DSTATCOM to Enhance Power Quality in Distribution System

Gokulananda Sahu[*],
Rajesh Kumar Patjoshi[**†], and **Rakhee Panigrahi**[***], Non-members

ABSTRACT

This paper proposes an FPGA based all-on-chip novel digital controller for DSTATCOM to compensate harmonics and reactive power existing in a power distribution system. The proposed methodology extracts reference current by considering an instantaneous symmetrical component active power (ISCAP) theory based phase delay compensation (PDC) approach. The proposed technique comprises positive sequence detector, PI-controller, low-pass filters (LPF) and hysteresis current controller (HCC). All these components are configured on high speed, low cost field programmable gate arrays (FPGA) hardware resources intended to mitigate harmonics and compensate reactive power in a power distribution network. Very high speed hardware description language (VHDL) implementation for each module are produced through a system generator and implemented on a SPARTAN-3 XC3S5000 FPGA chip through RT-XSG toolbox in Opal-RT platform. The functioning of the proposed controller is demonstrated via VHDL test bench, simulation and real-time experimental results concerning total harmonic distortion (THD) and power factor correction in steady state as well as transient condition.

Keywords: FPGA, Instantaneous Symmetrical Component Active Power Theory, Phase Delay Compensation, VHDL, System Generator, Total Harmonic Distortion, Power Factor

1. INTRODUCTION

In recent decades owing to proliferation of non-linear loads in various industrial sectors (use of dimmer, rectifiers, variable speed drives), tertiary sectors (data-processing or lighting in the offices, trades) and domestic sectors (television, electric and household appliances etc.) constitute the main harmonic sources of pollution, which cause power quality (PQ) problems in a distribution network [1, 2]. Indeed, this pollution is not only harmful to the power distribution equipment but also it affects control equipment utilized in various points in the power distribution network. Furthermore, it causes voltage contamination at the point of common coupling (PCC), heating of the cables and transformers, ageing of the material and the possible abnormal operations of sensitive electronic equipment.

To overcome the aforesaid issues, a suitable custom power device designated as distribution static compensator (DSTATCOM) [3] is introduced, which can compensate the harmonics and reactive power in the power distribution network. The DSTATCOM comprises of a power converter which is functioned with a specific control strategy. Thus, control strategy is one of the important aspects which can enhance the compensation capability of DSTATCOM. Therefore, this paper proposes an ISCAP theory based PDC technique for reference current generation, which extracts the reference current easily and quickly from the supply voltage during power system perturbation. Hence, operational speed and compensation capability of DSTATCOM is improved during a wide range of power system dynamic conditions.

Additionally, numerous authors have implemented different control strategies for DSTATCOM [4–6] by utilizing microcontrollers and digital signal processing (DSPs). However, these processors are overloaded owing to their heavy sequential computation for complex control algorithms. Hence, it produces latency during its processing time, which is not suitable for fast processing power system dynamic conditions. To reduce computational effort and latency time of the digital controller, aforesaid approaches have been dominated by FPGAs [5–9]

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[*]The author is with the Department of Electronics & Communication Engineering, Bhubaneswar College of Engineering, Bhubaneswar, India.

[**]The author is with the Department of Electronics and Communication Engineering, National Institute of Science and Technology, Berhampur, India.

[***]The author is with the Department of Electrical Engineering, Biju Patnaik University of Technology, Parala Maharaja Engineering College, Berhampur, India.

[†]Corresponding author. E-mail: rajeshpatjoshi1@gmail.com

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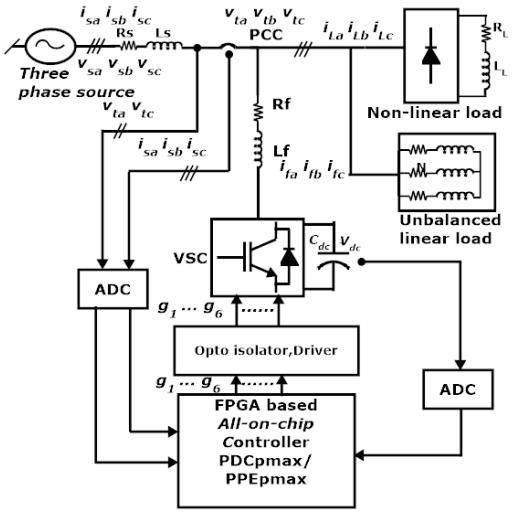
owing to their high degree of parallelism, low cost and high speed. In recent years, FPGAs have achieved relevance in various fields such as signal and image processing, neural networks, robotics, and communications [10–13]; however, in power electronics applications, few reports on all–on-chip integrated control are noticed through literature[14–16]. This work presents an all-on-chip controller of ISCAP-PDC (P_{max}) control structure on which several modules (PI-controller, positive sequence detector, instantaneous power estimator, low-pass infinite impulse response (IIR) filters, and HCC controller have been integrated for power quality improvement. To study the efficacy of the proposed structure, extensive simulations as well as experimentation have been carried out in MATLAB/Simulink and Real-time Opal-RT platform. The phase delay compensation PDC (P_{max}) structure is investigated through a distorted environment by introducing source side feeder impedance inside the system.

In this paper, the performance of the proposed all-on-chip controller is investigated in a three phase three wire system for balanced/distorted source and non-linear balanced/unbalanced load for mitigation of harmonics and compensation of reactive power. The performance is measured through the source current total harmonic distortion and power factor correction.

2. SYSTEM CONFIGURATION

Fig. 1(a) shows the basic circuit diagram of DSTATCOM [3] with a non-linear load connected to a three phase three wire distribution system. A nonlinear load is realized by using a three phase full bridge diode rectifier. A three phase voltage source converter (VSC) working as a DSTATCOM is realized using six insulated gate bipolar transistors (IGBTs) with anti-parallel diodes. At the ac side, the interfacing inductors are used to filter high frequency components of compensating currents. The switching of the inverter is done through monitoring the reference and actual currents and the reference error signal is fed to the HCC which is most suitable for all appliances owing to its unconditional stability, fast response, good accuracy and easy implementation with minimum hardware. The reference compensating currents are generated by the use of instantaneous symmetrical component and active power (ISCAP) which is most appropriate for distorted utility condition [4].

The dynamic of VSC is modeled by resolving differential equations governing a two-level inverter. The VSC model is based upon discrete switching variables g_a, g_b, g_c, dc-link Voltage V_{dc} and VSC



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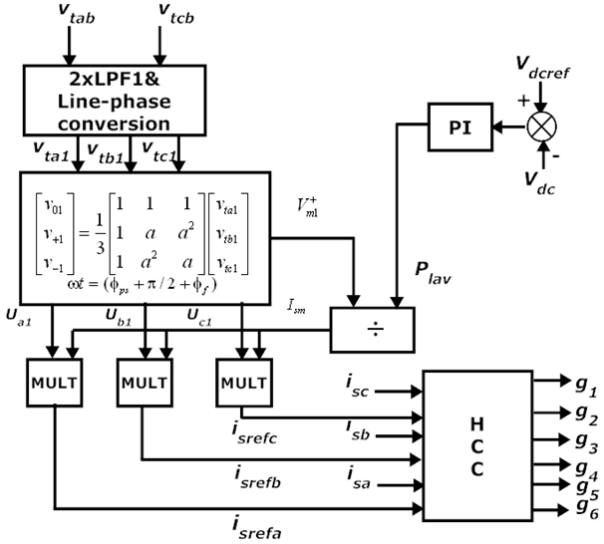


(b)

Fig.1: *System configuration and control structure of DSTATCOM; (a) system configuration and (b) ISCAP-PDC (P_{max}) control structure.*

voltages v_{fa}, v_{fb} and v_{fc}.

$$\begin{bmatrix} v_{fa} \\ v_{fb} \\ v_{fc} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} g_a \\ g_b \\ g_c \end{bmatrix} \tag{1}$$

The R–L network on the ac side of the converter is represented by three differential equations.

$$\begin{aligned} L_f \frac{di_{fa}}{dt} &= -i_{fa} \cdot R_f + v_{sa} - v_{fa} \\ L_f \frac{di_{fb}}{dt} &= -i_{fb} \cdot R_f + v_{sb} - v_{fb} \\ L_f \frac{di_{fc}}{dt} &= -i_{fc} \cdot R_f + v_{sc} - v_{fc} \end{aligned} \tag{2}$$

The dc side equations are represented as follows.

$$i_{dc} = g_a \cdot i_{fa} + g_b \cdot i_{fb} + g_c \cdot i_{fc} \tag{3}$$

$$-C_{dc} \cdot \frac{dV_{dc}}{dt} = i_{dc} \tag{4}$$

3. CONTROL STRUCTURE OF THE ALL-ON-CHIP CONTROLLER

Fig. 1(b) shows the control structure of the ISCAP-PDC (P_{max}) for reference generation scheme. This ISCAP-PDC (P_{max}) control structure estimates the peak value of the source current and average load power P_{lav} employing the PI-controller. Thus, the peak value of the source current is calculated as,

$$I^{+}_{sm1} = I_{sm} = \frac{P_{3\phi}}{3V^{+}_{m1}} \tag{5}$$

where $P_{lav} = P_{3\phi}/3$ is the load average power per phase and $P_{3\phi}$ is the three-phase instantaneous active power. Thus, the reference currents are generated as follows.

$$i^{*}_{sk} = i_{skref} = I_{sm} U_{k1} \tag{6}$$

where $k = a, b, c$ and U_{k1} is the fundamental unit vector template.

In PDC (P_{max}) control structure of the low pass filter one (LPF1), phase delay ϕ_f is determined through its magnitude response and it is constant for 50 Hz line frequency. The phase angle of the positive sequence voltage vector may be assumed to be ϕ_{ps}. So, the unit vectors can be computed as follows.

$$\begin{aligned} U_{a1} &= \sin\left(\phi_{ps} + \frac{\pi}{2} + \phi_f\right) \\ U_{b1} &= \sin\left(\phi_{ps} - \frac{\pi}{6} + \phi_f\right) \\ U_{c1} &= \sin\left(\phi_{ps} + \frac{7\pi}{6} + \phi_f\right) \end{aligned} \tag{7}$$

Fig. 1(b) shows the basic control structure of the proposed controller which constitutes one PI controller, low pass filters LPF1, hysteresis current controller (HCC) and arithmetic calculators (adders, multipliers (MULT)). The average power P_{lav} per phase is estimated by the PI controller. LPF1 is used to extract the fundamental from the distorted PCC voltage.

4. MODULE BASED DESIGN OF DIGITAL CONTROLLER

All the modules of the FPGA based digital controller have been designed with Xilinx fixed point block set [17] and VHDL implementations for all modules are generated through System Generator. This controller is designed for 3.3 V to work appropriately in FPGA board. Sensor signals are processed through signal conditioning circuits made available within 0–3.3V range. The module based design is carried out for each major block by employing Xilinx fixed point block set such as Adder, Subtractor, Multiplier, Constant, Convert, Logical, Mcode, Inverter, Relational, Reinterpret, Concatenation, Gateway In, Gateway out , Delay, Register, Mux, CORDIC SINCOS, CORDIC ATAN, CORDIC DIVIDER and CORDIC SQRT etc.

Table 1: *Processing speed and price comparison of DSPS and FPGAs digital processor.*

Performance Parameter	DSP eZdsp F2812 TMS32F2812	FPGA Spartan-3 XC3S5000
Clock in frequency	150 MHz	630 MHz
Peak multiply-accumulate (MAC) Unit	150 M/s	3600 M/s
RAM on chip	18 kBytes	529 + 1872 kBytes (Distributed + Block)
RAM on board	128 kBytes	5 MBytes
ROM on board	256 kbits	2 Mbits (Flash-ROM)
ADC	16 (2 S&H)	8 (External)
I/O	56	663
Price	$ 325.00	$ 189.00

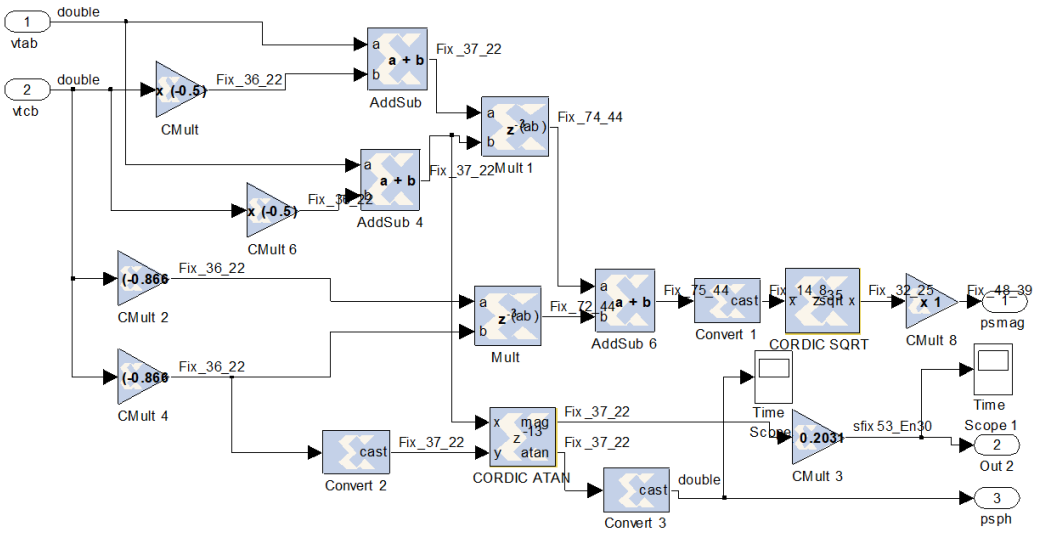
Furthermore, as described in the introduction sections, the ISCAP-PDC (P_{max}) based control algorithms can be employed on different digital processors such as DSPs and FPGAs. Table 1 shows the comparison between these processors based upon the performance, cost and hardware capabilities of the two starter boards depending on their technology. The starter boards are the Texas Instruments TMS320F2812 with eZdsp F2812 from Spectrum Digital Inc. DSP kit and the Digilent XCS5000 starter Board based on a low-cost Xilinx Spartan-3 FPGA device.

4.1 Positive Sequence Detector

The module depicted in Fig. 2(a) generates positive sequence peak magnitude (psmag) and phase angle ϕ (psph) from the line voltages v_{tab} and v_{tcb} based on the following Eqs. (8) and (9). The positive sequence magnitude and phase angle are depicted in Fig. 2(b) and (c), respectively.

$$\text{psmag} \quad V^{+}_{m1} = \frac{1}{3}\sqrt{\left(v_{tab} - \frac{1}{2}v_{tcb}\right)^2 + \left(-\frac{\sqrt{3}}{2}v_{tcb}\right)^2} \tag{8}$$

$$\text{psph} \quad \phi = \arctan\frac{-\frac{\sqrt{3}}{2}v_{tcb}}{v_{tab} - \frac{1}{2}v_{tcb}} \tag{9}$$



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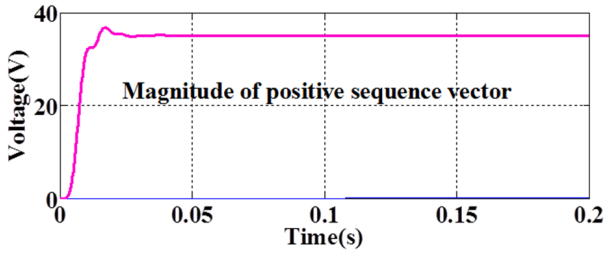

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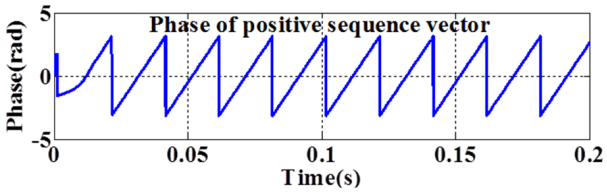


(c)

Fig.2: *Positive sequence detector design and its response; (a) positive sequence peak magnitude and phase angle generator block, (b) positive sequence vector magnitude, and (c) phase angle.*

4.2 Unit Vector and Reference Current (UVRC) and PI Controller

Employing the new reference generation control strategy ISCAP [4], the peak magnitude of the fundamental source current is evaluated. Then, this magnitude is multiplied with unit vectors to generate reference currents i^*_{sa}, i^*_{sb} and i^*_{sc}. The design of UVRC for three-phase is depicted in Fig. 3(a). The PI controller module shown in Fig. 3(b) estimates the optimized active power P_{max}, which is also equal to the load average active power P_{lav} depicted in Fig. 3(c). These terms are necessitated for calculation of peak magnitude of source reference current. Fig. 3(d) depicts the result of three-phase reference currents which are generated from the outputs of UVRC. This design is based upon the following Eq. (10), in which the output of the PI controller is $u(n)$ and the error $e(n)$ is the difference between V_{dcref} and V_{dc}.

$$\Delta u(n) = k_p \Delta e(n) + \frac{T_s}{2} k_i e(n) \tag{10}$$

where $\Delta u(n) = u(n) - u(n-1)$ and $\Delta e(n) = e(n) - e(n-1)$. T_s is the sampling frequency and k_p, k_i are the proportional and integral gain of the PI controller.

4.3 Low Pass Filter (LPF) and HCC Design

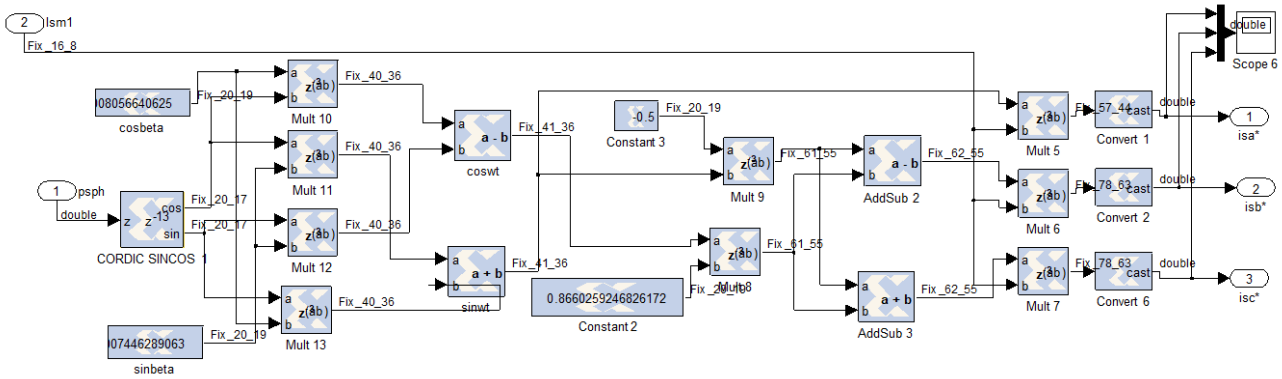
The design of the low pass filter LPF1 is based upon IIR Butterworth 6^{th} order (3×2^{nd} order section) direct form-II structure. Numerator and denominator coefficients are evaluated through FDA tool. The design of LPF1 comprises direct form-II structure, whereas the filter input and output configuration are shown in Fig. 4(a). The discrete transfer function of LPF1 is as follows. It constitutes three sections which are cascaded.

$$\begin{aligned} H(z) = k_1 \frac{1 + b_{11}z^{-1} + b_{12}z^{-2}}{1 - a_{11}z^{-1} - a_{12}z^{-2}} \\ \times k_2 \frac{1 + b_{21}z^{-1} + b_{22}z^{-2}}{1 - a_{21}z^{-1} - a_{22}z^{-2}} \\ \times k_3 \frac{1 + b_{31}z^{-1} + b_{32}z^{-2}}{1 - a_{31}z^{-1} - a_{32}z^{-2}} \end{aligned} \tag{11}$$

The gain and coefficients for each section are given below.

Gains:

$[k_1, k_2, k_3] = [0.00003900, 0.00003410, 0.99999999]$



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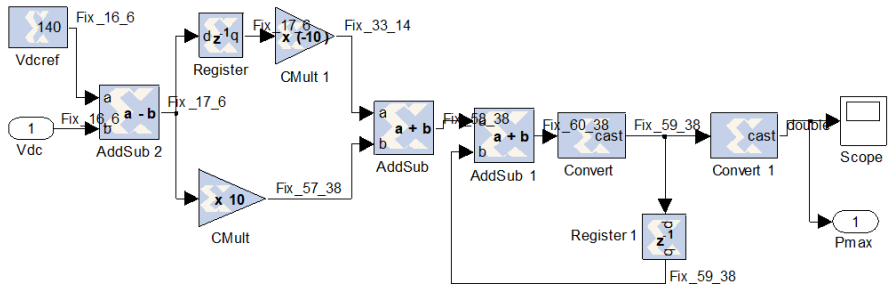

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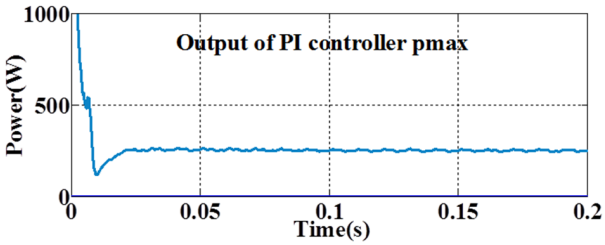

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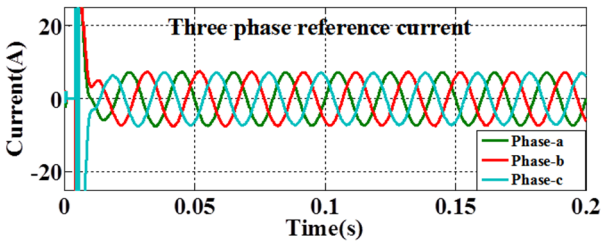


(d)

Fig.3: *Unit vector with reference current and PI controller design and response; (a) unit vector with reference current signal generator module block, (b) design structure of PI controller module for estimating optimized active power, (c) PI controller response P_{max}, and (d) three-phase reference current.*

Coefficients:

Section-1: $[b_{11}, b_{12}, a_{11}, a_{12}] = [2, 1, -1.976854, 0.976015]$
Section-2: $[b_{21}, b_{22}, a_{21}, a_{22}] = [2, 1, -1.993359, 0.993516]$
Section-3: $[b_{31}, b_{32}, a_{31}, a_{32}] = [2, 1, -1.982228, 0.982385]$

This filter eradicates any type distortion and contamination present in the supply voltage signal during reference signal generation. The corresponding input and output waveform of LPF1 for phase-a is presented in Fig. 4(b). The switching signals of each leg are generated by comparing the source current error with the hysteresis band. The gate pulses for the upper switch of phase-a leg are demonstrated in Fig. 4(c).

- If $i_{sk} \geq (i^*_{sk} + HB)$, then upper switch is ON and lower switch is OFF in each leg of DSTATCOM.
- If $i_{sk} \leq (i^*_{sk} - HB)$, then upper switch is OFF and lower switch is ON in each leg of DSTATCOM,

where k represents phases, i_{sk}, i^*_{sk} are actual and reference source currents in the system respectively. HB is the hysteresis band of the hysteresis current controller.

5. RESULTS AND DISCUSSION

To investigate the performance of the DSTATCOM, simulations are performed on MATLAB/Simulink platform. A three phase three wire distribution system with parameters given in Table 2 is considered for both simulation and real-time platforms.

5.1 Simulation Results

The response of the proposed ISCAP-PDC (P_{max}) based DSTATCOM system is depicted in Fig. 5. The figure comprises of load current, PCC voltage, source current, compensating current for phase-a. Similarly, Fig. 6 illustrates the dc-link voltage,

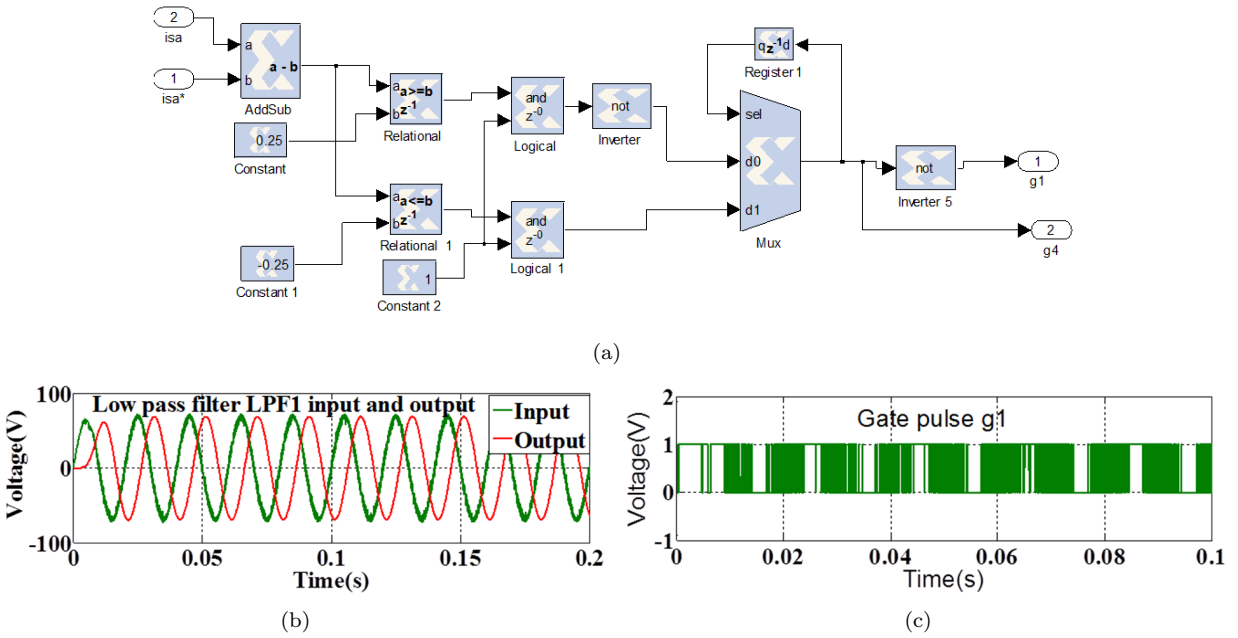


Fig.4: *Low pass filter and switching signal; (a) LPF input and output configuration structure design, (b) input and output waveform of LPF, and (c) switching signal waveform g1.*

Table 2: *System parameters for DSTATCOM.*

System	Parameters	Notation	Value
Source	Voltage	V_{sabc}	50 V_{rms} (L-N)
	Frequency	f_s	50 Hz
	Resistor	R_s	0.1 Ω
	Inductor	L_s	0.15 mH
Nonlinear load	Diode rectifier		6-diode
	Resistor	R_L	20 Ω
	Inductor	L_L	10 mH
DC storage Capacitor	DC-link capacitor	C_{dc}	2100 μF
	Reference voltage	V_{dcref}	140 V
DSTATCOM	Interface inductor	L_f	1.8 mH
	and resistor	R_f	0.1 Ω
	Switching frequency	f_{sw}	25 kHz
	Sampling frequency	f_s	50 kHz
PI-controller		k_{pr}	30
		k_{ir}	100
Hysteresis band			0.25 A
Low pass butterworth filter LPF1 and LPF2	Cut-off frequency	f_c1	100 Hz
	Sampling frequency	f_s	50 kHz
	Order Structure	6^{th} (3×2^{nd} order section) Direct form-II	

unity power factor, harmonics spectrum of load current and harmonics spectrum of source current after compensation for the proposed technique. Figs. 5(a) and (b) show the corresponding load current and PCC voltage waveform. Through extensive simulations it is found that harmonic compensation of source current is quite effective. The DSTATCOM injects equal and opposite amounts of harmonics to the PCC for harmonics compensation. The consistent harmonics compensation waveform is demonstrated in Fig. 5(d). Thus, harmonics compensation is performed efficiently with minimal steady-state error and the source current becomes perfectly sinusoidal as presented in Fig. 5(c).

The total harmonics distortion (THD) associated with the load current and compensated source current are illustrated in Figs. 6(c) and (d). From the figure it can be observed that the harmonic contents of the compensated source current are effectively reduced as compared to the load current. Further, the dc-link capacitor voltage is set at 140 V. Subsequently, the dc-link capacitor voltage is regulated by considering an outer control loop approach. From Fig. 6(a) it is observed that nearly 0.02 s is required for settling down of the dc-link voltage. Both source current and voltage are in phase indicating that the system is in unity power factor mode as displayed in Fig. 6(b).

Fig. 7 illustrates the load current transient state response of DSTATCOM with ISCAP-PDC (P_{max}) based control structure. Figs. 7(a) and (b) display the three phase load current before compensation and the corresponding compensating current of phase-a. Similarly, Figs. 7(c) and (d) demonstrate the source

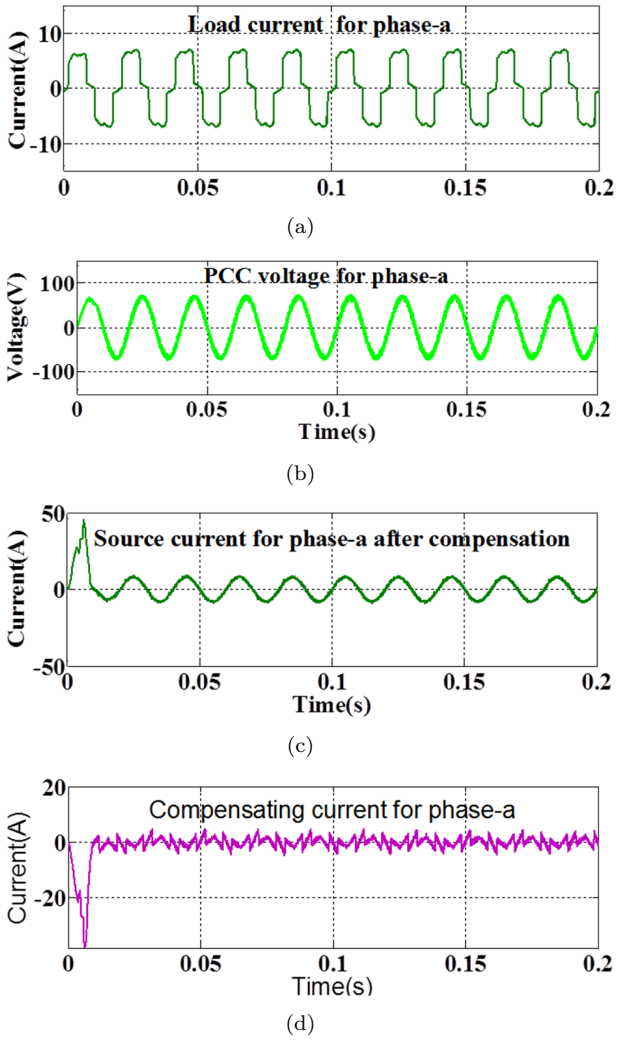


Fig.5: *Steady state response of DSTATCOM with ISCAP-PDC (P_{max}) structure; (a) load current for phase-a before compensation, (b) distorted PCC voltage for phase-a, (c) source current for phase-a after compensation, and (d) compensating current for phase-a.*

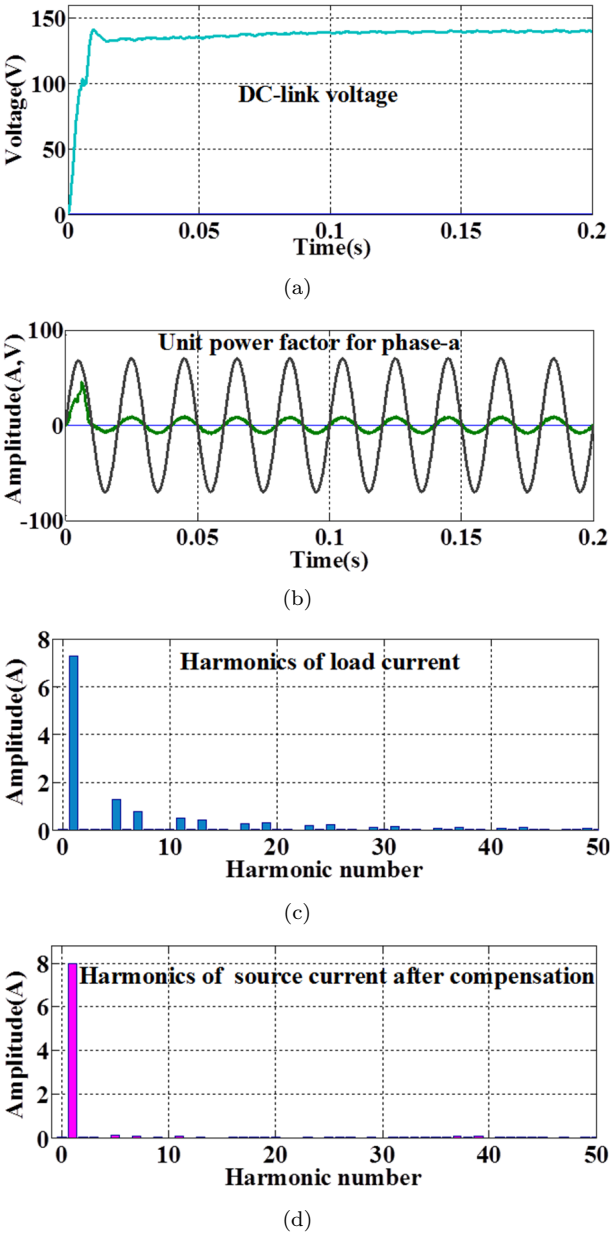
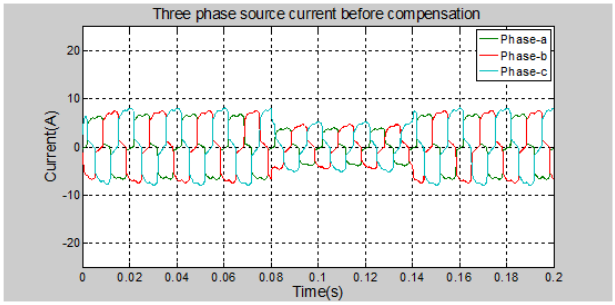


Fig.6: *Steady state response of DSTATCOM with ISCAP-PDC (P_{max}) structure; (a) dc-link voltage, (b) unit power factor for phase-a, (c) THD spectrum of load current, and (d) THD spectrum of source current after compensation.*

voltage as well as compensated source current to signify the unity power factor and THD of the load current. Correspondingly, Fig. 8 shows the source current transient state response of DSTATCOM with ISCAP-PDC (P_{max}) based control structure. Figs. 8(a) and (b) illustrate the compensated source current and dc-link voltage during transient state condition. Furthermore, Figs. 8(c) and (d) display real power (p) as well as reactive power (q) before and after compensation and THD of source current after compensation. Moreover, it is analyzed that the step change in load occurred with a time interval between 0.08 s and 0.14 s. However, it is observed from the result that, during this transient period the capacitor voltage quickly settles (≈0.0166 s) to its set-point. Hence, the compensation capability of DSTATCOM is enhanced. Moreover, the source current is found to be smoother and less distorted as shown in Fig. 8(a). The source current THD is observed to be 2.7062% in transient state condition.

5.2 Experimental Result

Opal-RT OP5142 experimental setup (Fig. 9(a)) is built in laboratory to validate the FPGA based design and study the efficacy in a real-time environment. The OP5142 provides a user friendly platform [18] for configuring FPGA devices depicted in Fig. 9(b). The System Generator for DSP tool



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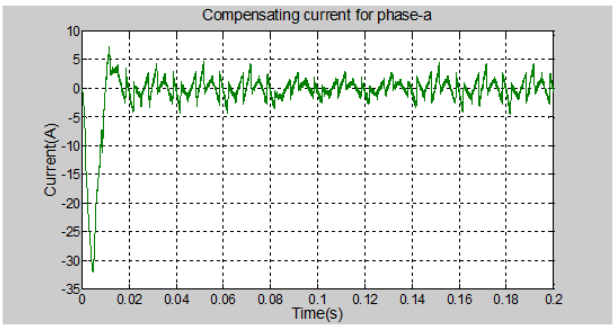

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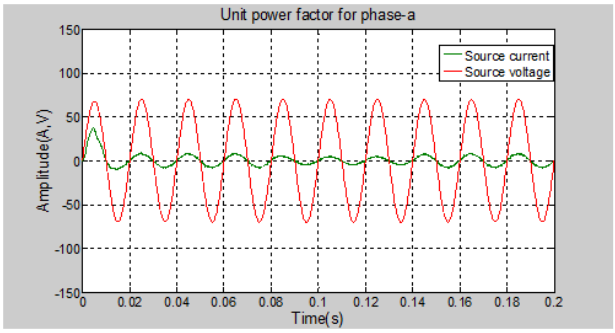

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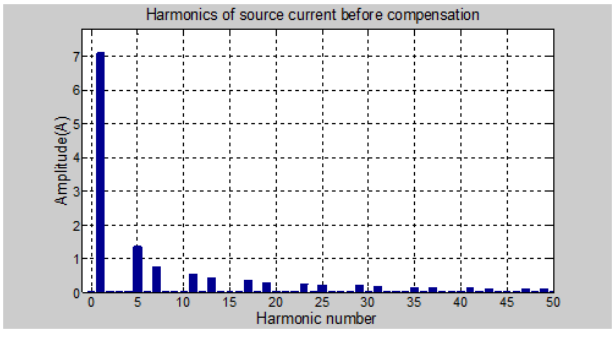
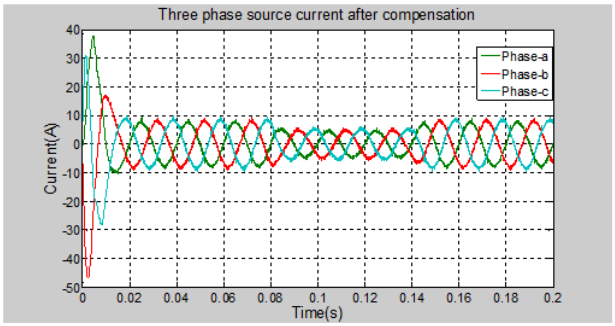


(d)

Fig.7: *Load current transient state response of DSTATCOM with ISCAP-PDC (P_{max}) structure; (a) three phase Load current before compensation, (b) compensating current for phase-a, (c) unit power factor for phase-a, and (d) THD spectrum of load current before compensation.*



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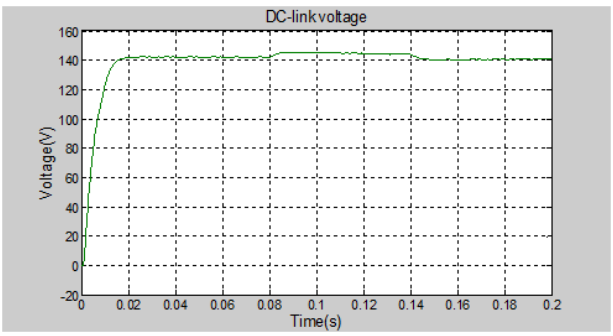

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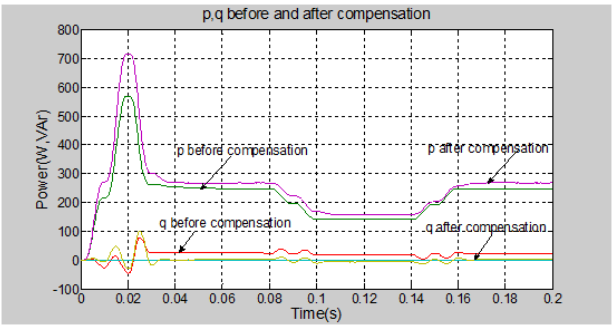
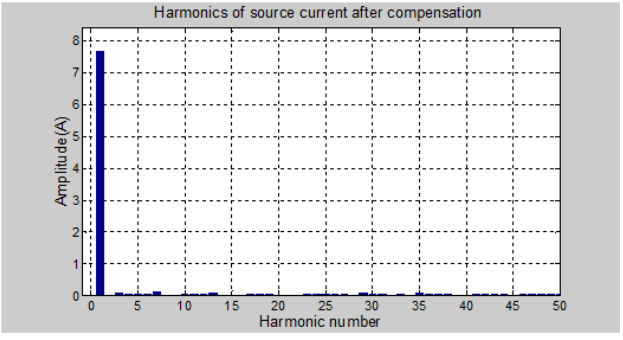
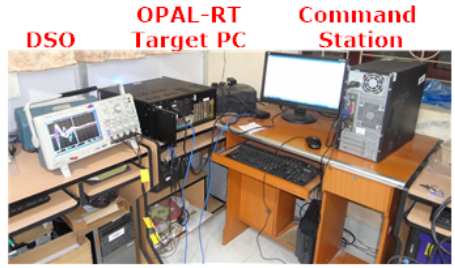


(c)

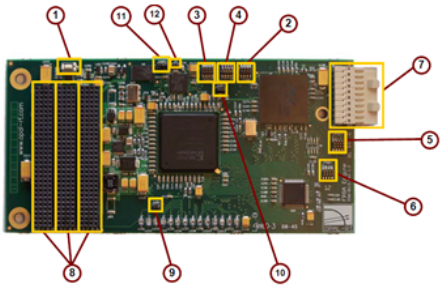


(d)

Fig.8: *Source current transient state response of DSTATCOM with ISCAP-PDC (P_{max}) structure; (a) three phase Load current after compensation, (b) dc-link voltage, (c) real and reactive power before and after compensation, and (d) THD spectrum of source current after compensation.*



(a)



(b)

SL. No	Name	Description
1	S1	FPGA Engine manual reset
2	JTAG1	FPGA JTAG interface
3	JTAG2	CPLD JTAG interface
4	JUMP4	JTAG Architecture selection
5	JTAG3	PCIe JTAG interface
6	JTAG4	SerDes JTAG interface
7	JP1	PCIe synchronization bus and power supply
8	J1/J2/J3	Backplane data,ID and I^2C interface
9	JUMP1	Identification EEPROM write protection
10	JUMP2	FPGA Configuration mode selection
11	JUMP3	Flash memory write protection
12	j4	Flash memory forced programmation voltage

(c)

Fig.9: *Opal-RT experimental setup; (a) RTDS hardware, (b) 5142 layout, and (c) OP5142 connector.*

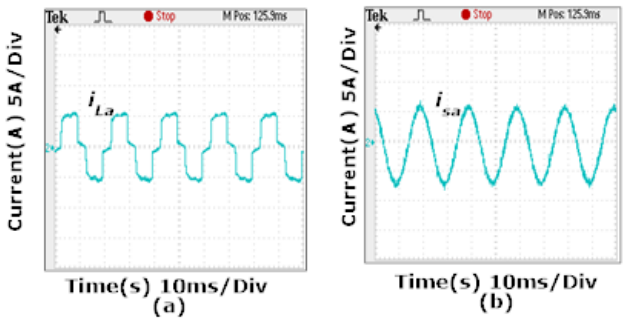


Fig.10: *Steady state response of DSTATCOM with ISCAP-PDC (P_{max}) structure (real-time); (a) load current for phase-a and (b) source current for phase-a after compensation.*

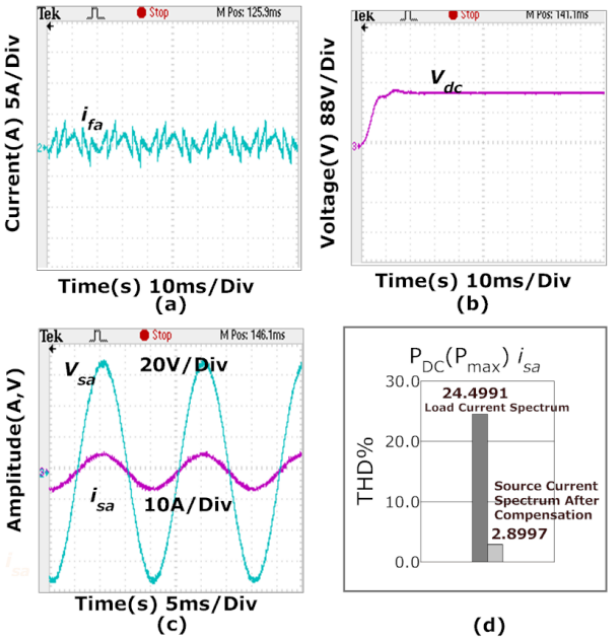


Fig.11: *Steady state response of DSTATCOM with ISCAP-PDC (P_{max}) structure (real-time); (a) compensating current for phase-a, (b) dc-link voltage, (c) unit power factor for phase-a, and (d) THD of source current before and after compensation.*

box from Xilinx along with RT-XSG from Opal-RT technologies can be integrated with Simulink to form a real-time reconfigurable platform for OP5142. This allows transferring Simulink sub-models to the FPGA processor for distributed processing. Through RT-XSG, Simulink specifies the models that will be executed by the reconfigurable platform.

The programming file is generated through 'Opal-RT FPGA Synthesis Manager' and the device is configured through 'Op ctrl reconfigurable I/O' block. The 'Opal-RT FPGA Synthesis Manager' block includes all the functionalities required to compile RT-XSG user model. This model is translated into a programming file suitable for the FPGA device in OP5142 [19]. The RT-LAB software environment facilitates the user to program the reconfigurable boards through simulation model using the configuration file generated by this block. Fig. 9(c) shows the OP5142 jumpers and connectors required for configuration mode selection and interface respectively.

The real time results obtained from Opal-RT are depicted in Figs. 10, 11 and 12 which demonstrate the

Table 3: *Performance metrics of ISCAP-PDC (P_{max}) system (steady state).*

Performance metrics	ISCAP-PDC (P_{max}) system in steady state					
	Before compensation			After compensation		
	Phase-a	Phase-b	Phase-c	Phase-a	Phase-b	Phase-c
THD(%) of source current	24.4991	22.6661	22.8166	2.8997	3.1827	3.0289
Active power p (W)	252.4	273.7	268.8	278.4	281.2	274.0
Reactive power q (Var)	30.6	23.6	46.0	1.6	8.0	7.3
Power factor (pf)	0.9927	0.9963	0.9857	1	0.9996	0.9996

Table 4: *Performance metrics of ISCAP-PDC (P_{max}) system (transient state).*

Performance metrics	ISCAP-PDC (P_{max}) system in transient state					
	Before compensation			After compensation		
	Phase-a	Phase-b	Phase-c	Phase-a	Phase-b	Phase-c
THD(%) of source current	24.4991	22.6661	22.8166	4.1354	4.5652	3.8959
Active power p (W)	252.36	273.7	266.8	278	283	275
Reactive power q (Var)	30.6	23.6	46.0	5.5	12.5	9.5
Power factor (pf)	0.9927	0.9963	0.9857	0.9998	0.9990	0.9994

details of load current, source current, compensating current, dc-link voltage, unit power factor and source current after compensation for structure ISCAP-PDC (P_{max}) during both steady and transient state condition. The steady state response of DSTATCOM with ISCAP-PDC (P_{max}) control structure is shown in Fig. 10. Fig. 10(a) shows the load current for phase-a and Fig. 10(b) shows the source current for phase-a after compensation.

Fig. 11(a) shows the compensating current for phase-a. It is observed from the Fig. 11(b) that the proposed controller can provide better stabilization to the dc-link voltage. Moreover, the equivalent rise time and settling time of the dc-link voltage are 0.0145 s and 0.0262 s with minimum overshoot of 1.6773%, which shows that the tracking performance of the proposed controller is better for compensation of harmonics and reactive power. It is observed that the source voltage and source current after compensation have phase error equal to zero, that means the system has achieved unity power factor as depicted in Fig. 11(c). Additionally, Fig. 11(d) shows the result of THD spectrum for phase-a load current and source current after compensation. The THD for three phase load current and source current after compensation are calculated separately. The values of THDs for load current are observed to be 24.4991%, 22.6661% and 22.8166% and for the corresponding source current THDs are observed to be 2.8997%, 3.1827% and 3.0289%. The performance matrices of the proposed ISCAP-PDC (P_{max}) structure based all-on-chip controller are demonstrated in Table 3.

Fig. 12 presents the real-time transient results of three phase load current, compensated source current, compensating current, dc-link voltage, phase relationship between source voltage and source current and THD result for load and compensated source current in the proposed ISCAP-PDC (P_{max}) based DSTATCOM system. It is analyzed that the waveforms for load current, compensated source current, compensating current, dc-link voltage and unity power factor are almost same as the simulation results as expressed in Figs. 7 and 8. The performance metrics of this result are demonstrated in Table 4. The values of THDs for three phase load current are observed to be 24.4991%, 22.6661% and 22.8166% and likewise, the THDs for the corresponding three phase source current are perceived to be 4.1354%, 4.5652% and 3.8959%. Additionally, active and reactive power along with power factor before and after compensation are also demonstrated in the Table 4.

5.3 VHDL Test Bench Result

Fig. 13 shows the VHDL Test Bench, switching pulse of the top module in full zoom and device utilization summary for ISCAP-PDC (P_{max}) structure. Signals prefixed with 'gi' and 'go' are identified as gateway input and gateway output signals of the FPGA based all-on-chip controller respectively. Fig. 13(a) displays the test bench waveform of the switching signal for DSTATCOM and the enlarged versions of all six switching signals are represented in Fig. 13(b). The design is incorporated using VHDL in the ISE10.1 tool from Xilinx along with Modelsim 13.bPE from Mentor Graphics and is implemented on a Xilinx SPARTAN-3 XC3S5000 chip. Fig. 13(c) exhibits the resource utilization summary which indicates the area occupied by the FPGA device.

6. CONCLUSION

This paper facilitates the development and implementation of a FPGA-based novel digital controller

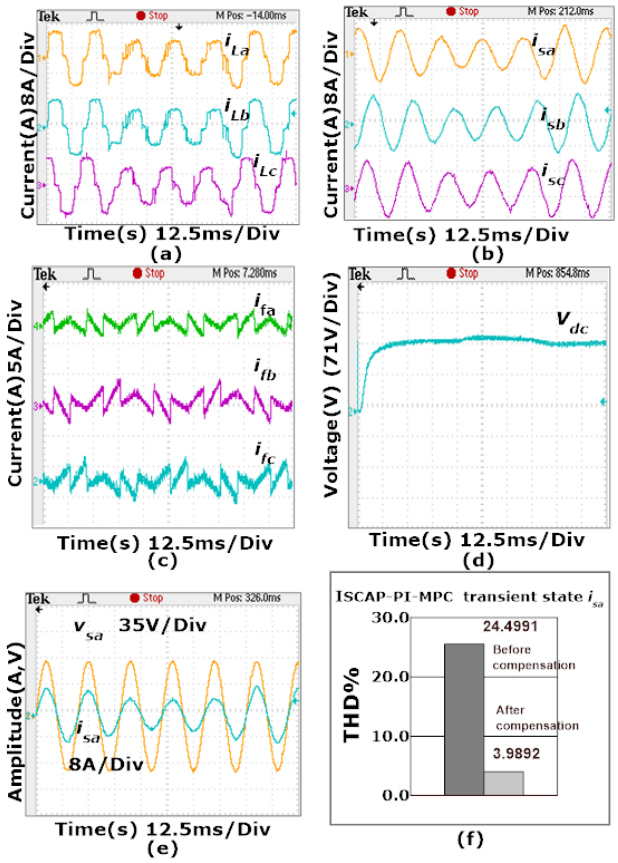
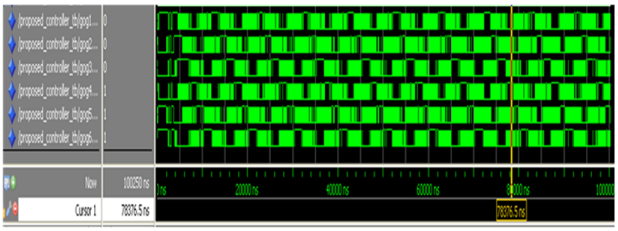
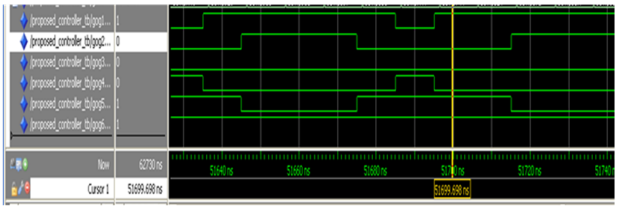


Fig.12: *Transient state response of of DSTATCOM with ISCAP-PDC (P_{max}) structure (real-time); (a) three-phase load current before compensation, (b) three-phase source current after compensation, (c) compensating current for phase a, b and c, (d) dc-link voltage, (e) phase relationship between source voltage and source current after compensation, and (f) load current and source current THD before and after compensation.*

for DSTATCOM which is faster and provides a greater degree of feasibility as well as flexibility than a microcontroller and DSP based processor. After verification through OP5600 HIL platform, it is implemented on a Xilinx XC3S5000 chip successfully. The performances of the proposed controller are demonstrated through VHDL test bench, simulation and real-time results with consideration of total harmonic distortion and power factor correction in steady state as well as transient condition. The ISCAP-PDC (P_{max}) structure supported via FPGA built digital controller gives rise to THD% results such as 2.8997, 3.1827, 3.0289 for phase a, b, and c, respectively. The aforementioned outcomes show that an all-on-chip digital controller for ISCAP-PDC (P_{max}) is able to compensate the harmonics generated by non-linear load and affords sinusoidal source current within allowable range of IEEE 519 standard.



(a)



(b)

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	11728	33280	35%
Number of Slice Flip Flops	5657	66560	8%
Number of 4 input LUTs	19339	66560	29%
Number of bonded IOBs	103	489	21%
Number of MULT18X18s	59	104	56%
Number of GCLKs	1	8	12%

(c)

Fig.13: *VHDL test-bench and RTL schematic of ISCAP-PDC (P_{max}) all-on-chip controller; (a) VHDL test bench waveform of switching signal, (b) switching signal for DSTATCOM in full zoom, and (c) device utilization summary.*

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Gokulananda Sahu received the B.E. degree in Electronics from Dr. Babasaheb Ambedkar Marathwada Universiy, India and the M.Tech and Ph.D. degrees in Electronics and Communication Engineering from the National Institute of Technology, Rourkela, India, in 2010 and 2017, respectively. He is currently an Associate Professor in Bhubaneswar College of Engineering, Bhubaneswar, Odisha, India. He has 20 years of teaching and research experience. His research interest includes power quality, industrial electronics, VLSI design, embedded system and FPGA based system design.

Rajesh Kumar Patjoshi received the B.E. degree in Electronics and Telecommunication Engineering from the Amaravati University, India and the M.Tech and Ph.D. degrees in Electronics and Communication Engineering from the National Institute of Technology, Rourkela, India, in 2010 and 2015, respectively. He is currently an Associate Professor in the Department of Electronics and communication Engineering, National Institute of Science and Technology, Berhampur, India. His research interests include power quality enhancement towards grid integrated renewable energy source and microgrid system, network control system, embedded systems, VLSI design for artificial intelligence, Low power and RF VLSI design.

Rakhee Panigrahi received the B.E. degree in Electrical Engineering from the Veer Surendra Sai University of Technology Burla, Odisha, India and the M.Tech and Ph.D. degrees in Electrical Engineering from the National Institute of Technology, Rourkela, India, in 2009 and 2015, respectively. She is currently an Assistant Professor in the Department of Electrical Engineering, Biju Patnaik University of Technology, Parala Maharaja Engineering College, Berhampur, India. Her research interests include advanced control approach, estimation techniques with application to power quality, renewable energy and grid integrated microgrid system.