

# Trimming Lithography: An Alternative Technology for Sub-Resolution and Sub-Wavelength Patterning

Nithi Atthi<sup>1</sup>, Areerat Sriklad<sup>2</sup>, Wutthinan Jeamsaksiri<sup>3</sup>, Charndet Hruanun<sup>4</sup>, Amporn Poyai<sup>5</sup>, and Rardchawadee Silapunt<sup>6</sup>, Non-members

## ABSTRACT

Lithography is one of the key technologies for scaling down a size of integrated circuits thus increasing the performance of an electronic device. Currently, there are many lithographic techniques that are potentially capable to produce a nanometer feature size but the continuing development for a commercial use is still limited by extremely high investment especially on exposure equipment and mask. This paper introduces an alternative patterning technique called Trimming lithography as one of the strong candidates for future lithography, for producing sub-resolution and subexposure wavelength features. The pattern size can be downscaled by carefully adjusting the trim distance that is much higher than an original design linewidth. It is shown that the photoresist (PR) feature size can be scaled down with the acceptable profile to approximately  $0.18 \mu\text{m}$  from the original  $0.8 \mu\text{m}$  mask pattern with the  $0.5 \mu\text{m}$  resolution of the exposure tool. However, the pattern density of the line/space pattern becomes lower than that of the typical lithography. Different pattern qualities between dense and isolated patterns are probably explained by a diffraction occurring during a transmission of light through the mask slit.

**Keywords:** Lithography, Moore's Law, Next-generation Lithography, Pattern Shrinkage, Sub-resolution Patterning, Trimming Lithography

## 1. INTRODUCTION

The size of the integrated circuits (ICs) pattern has been shrunk down at the rate of 30% for every three years and the numbers of transistors in a chip has been approximately double every 18 months during the past 50 years. This pattern scaling trend is called Moore's law [1]. The international technology roadmap of semiconductor (ITRS) predicted that

the smallest feature size, which is used for gate electrode, of complementary metal-oxide-semiconductor (CMOS) products would continue to shrink down to below 40 nm node for production line within year 2011 [2]. The advantages of scaling down the pattern size for ICs are chip size reduction, more transistors per IC, lighter, faster operation, more intelligent, lower power consumption, and lower cost per chip. This tiny device is a key component of modern electronic appliances such as high definition flat panel display (HD-FPD), high capacity hard disk drives (HDD), and etc [2]. It is unquestionably that the key success for scaling down the pattern size is the performance of the lithography tool and technique. The most extensively used technique is the optical lithography (OL) that has long been the powerful workhorse for micro-scale IC manufacturing. Theoretically, the resolution ( $R$ ) of the OL is increased by decreasing the wavelength of the light source ( $\lambda$ ), adjusting the lens diameter and improve the lens arrangement to increase the numerical aperture ( $NA$ ), and improving the process performance ( $K_1$ ) as stated in (1) [3],

$$R = K_1 \lambda / NA, \quad (1)$$

where  $R$  = exposure tool's resolution (nm),  
 $K_1$  = lithography process constant,  
 $\lambda$  = wavelength of the light source (nm),  
 and  $NA$  = numerical aperture of the lens system.

Normally,  $K_1$  can be increased by using various Resolution enhancement technologies (RETs) such as (1) Phase shifted mask (PSM), (2) Optical proximity correction (OPC), (3) Off-axis illumination (OAI), (4) Hyper- $NA$  immersion scanning system, with a (5) Chemical amplified resist (CARs) [3-4]. However, the investment cost of OL is unbelievably high, e.g., EUR-10M for a 32 nm immersion scanner and EUR-0.1M for 65 nm node one mask plate [5]. In contrast, the other nonoptical lithography techniques have also been developed such as e-beam lithography (EBL) [1], X-ray projection lithography (XPL) [2], and nano-imprint lithography (NIL) [5]. However, the application and development of these techniques are impeded by their low throughput, small area fabrication, and high cost and timeconsumption for the

Manuscript received on April 10, 2012 ; revised on October 18, 2012.

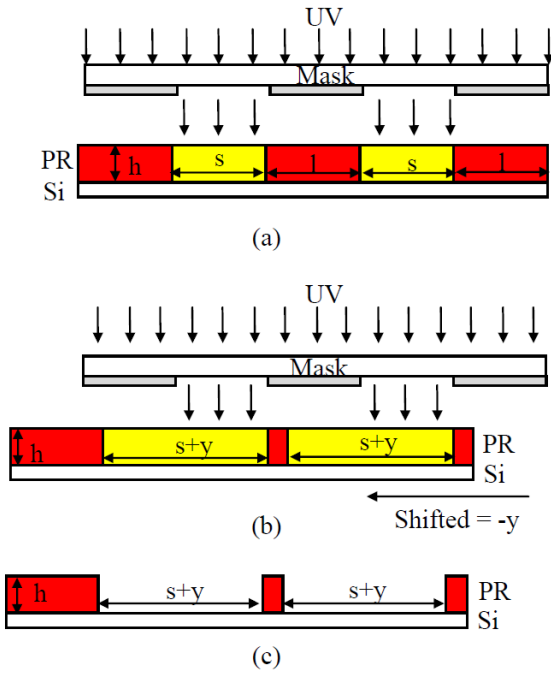
<sup>1,3,4,5</sup> The authors are with Thai Microelectronics Center (TMEC), National Electronics and Computer Technology Center (NECTEC), Thailand., E-mail: nithi.atthi@nectec.or.th

<sup>2,6</sup> The authors are with Department of Electronic and Telecommunication Engineering, King Mongkut's University of Technology Thonburi, Thailand., E-mail: rardchawadee.sil@kmutt.ac.th

process development. To overcome these limitations, the novel lithography technique for scaling the pattern size called Trimming lithography is introduced [6].

The concept of Trimming lithography primarily involves the synchronization of the exposure dose with the exposure position (a clear area on the mask or a scanning position of the direct patterning). The PR pattern size can be reduced with 2-step patterning as shown in Fig. 1. The first full exposure is performed to produce a pattern size  $l$ . Then, the wafer substrate is shifted to the left for a distance  $y$ , and the PR is fully exposed again. After a single development, the PR pattern on the wafer is scaled down to  $l - y$  and the space between the patterns is increased to  $s + y$ .

The objective of this research is to determine the potential of Trimming lithography for shrinking the PR pattern size, which in some cases, below the resolution of the exposure tool and then determine the effects of the trimming distance on the pattern quality.



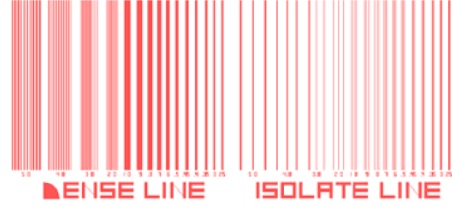
**Fig.1:** Trimming lithography concept: (a) 1<sup>st</sup> exposure, (b) 2<sup>nd</sup> exposure with mask shifting, (c) trimmed PR pattern after a single development.

## 2. EXPERIMENTAL SETUP

### 2.1 Pattern design and mask preparation

In this experiment, two types of test structures are designed; (1) dense line and space (L/S) whose pattern size is equal to the pattern space and (2) isolated line. The designed pattern sizes are 5.0, 4.0, 3.0, 2.0, 1.0, 0.9, 0.8, 0.7, 0.6, 0.5, 0.45, 0.40, 0.35, 0.30, and 0.25  $\mu\text{m}$  as shown in Fig. 2. The layout data is converted in the inverted mode with 5x magnification

from the original design and the pattern is written by the Heidelberg Direct Write Laser (DWL) on the  $6 \times 6 \times 0.25$  inch<sup>3</sup> (6025) mask.



**Fig.2:** The layout of the test structures.

### 2.2 Process window evaluation for the 0.5 $\mu\text{m}$ L/S pattern using the Energy-Focus matrix

This experiment is carried out using the Nikon NSR2005i8A 5x demagnification stepper with the UV wavelength  $\lambda = 365$  nm,  $NA = 0.54$ , and  $R = 0.50$   $\mu\text{m}$ . The 0.5  $\mu\text{m}$  L/S pattern is selected for the evaluation as its size is a borderline for image resolving defined by the stepper resolution. First, a six inch diameter silicon wafer substrate is spin-coated with the Sumitomo PFI34-A positive PR and then pre-baked in the hotplate at 90° C for 3 min. The PR film thickness is 1.09  $\mu\text{m}$  with the thickness deviation of 3.0 % across the wafer. The pattern is transferred to the wafer by varying the exposure shutter time of the stepper from 60 to 580 msec with an increment step of 20 msec. The focus distance ( $F$ ) is also varied from -1.6 to 1.6  $\mu\text{m}$  with the step of 0.2  $\mu\text{m}$ . Note that the mercury arc lamp power during the experiment is 350.81 mW/cm<sup>2</sup>. This means that the exposure dose is varied from 21.1 to 203.5 mJ/cm<sup>2</sup>. The sample is next post-exposure baked (PEB) at 110° C for 60 sec to reduce the standing wave on the PR sidewall and puddle developed in a single step using the Tokuyama SD-W developer for two conditions; 60 and 75 sec. The pattern quality of the 0.5  $\mu\text{m}$  L/S pattern is sorted using the 150x optical microscope (OM) with Thai Microelectronics Center (TMEC)'s standard procedure. The effects of  $F$  on the developed profile of the processed samples are studied by varying  $F$  from -0.4 to +1.8  $\mu\text{m}$  with a 0.2  $\mu\text{m}$  step at the constant exposure dose of 120 mJ/cm<sup>2</sup> and the single step development for 60 sec. The estimated sidewall angle ( $\theta_s$ ) is measured from the top view critical dimension (CD) using the Hitachi S-4700 scanning electron microscope (SEM) and calculated by (1). Note that, this calculation assumes the PR film thickness ( $h$ ) of 1.09  $\mu\text{m}$  and the PR pattern has a trapezoid shape [7] with a uniform slope.

$$\theta_s = \tan^{-1}[(CD_T - CD_B)/2] \quad (2)$$

where  $\theta_s$  = PR sidewall angle (degree),  
 $CD_T$  = top pattern linewidth ( $\mu\text{m}$ ),

and  $CD_B$  = bottom pattern linewidth ( $\mu\text{m}$ ).

### 2.3 Study of the effects of 0.5 $\mu\text{m}$ trimming on the pattern quality

In this experiment, the pattern is trimmed by shifting the wafer for  $+0.5 \mu\text{m}$  from the original position. The wafer is first aligned with the center of the mask, referred as the origin (0, 0), for the 1<sup>st</sup> exposure step as shown in Fig. 1(a). Then the 2<sup>nd</sup> exposure step is performed by shifting the wafer to the position (-0.5, 0) as shown in Fig. 1(b), meaning that the target pattern is  $0.5 \mu\text{m}$  smaller than that of the design. The exposure dose ( $E$ ) and  $F$  are kept at  $120 \text{ mJ}/\text{cm}^2$  and  $-0.2 \mu\text{m}$  respectively, throughout the experiment. Then the sample is developed in a single step for 75 sec. The pattern quality is characterized by the SEM.

### 2.4 Study of the effects of the trimming distance on the pattern quality

In this experiment, a silicon wafer is spin-coated with the Sumitomo PFI34-A positive PR and then prebaked in the hotplate at  $90^\circ\text{C}$  for 3 min. The target PR film thickness is  $1.09 \mu\text{m}$  with 3.0% deviation. The 1st exposure step is done by aligning the wafer with the center of the mask, referred as the origin (0, 0), as shown in Fig. 1(a). The 2<sup>nd</sup> exposure step is subsequently performed by using the same mask plate but this time the wafer is shifted from 0.4 to  $0.9 \mu\text{m}$  with an increment step of  $0.1 \mu\text{m}$  as shown in Fig. 1(b). The exposure doses ( $E$ ) during the 1<sup>st</sup> and 2<sup>nd</sup> exposures are similar and fixed at  $120 \text{ mJ}/\text{cm}^2$  while the focus ( $F$ ) is fixed at  $-0.2 \mu\text{m}$ . This means that the 1<sup>st</sup> exposure PR pattern is trimmed by the range of 0.4 to  $0.9 \mu\text{m}$  as shown in Fig. 1(c) and the ideal minimum feature size after trimming is then equal to 50 nm. The calculation results are shown in Table 1. The sample is then postexposure baked (PEB) at  $110^\circ\text{C}$  for 60 sec and developed with the Tokuyama SD-W developer for 60 sec. The pattern linewidth and sidewall angle ( $\theta_s$ ) are characterized by the SEM.

## 3. RESULTS AND DISCUSSIONS

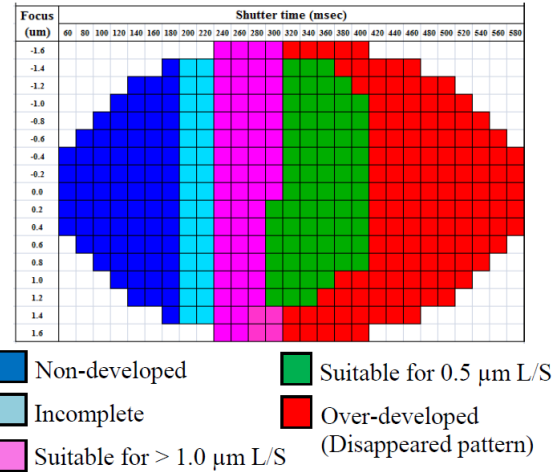
### 3.1 Process window for the 0.5 $\mu\text{m}$ L/S pattern

By using the development time at 60 sec, the good exposure dose to clear for the  $0.5 \mu\text{m}$  L/S pattern size or larger is found at  $E = 300$  to  $400 \text{ msec}$  ( $105$  to  $140 \text{ mJ}/\text{cm}^2$ ) and  $F = -1.4$  to  $1.2 \mu\text{m}$ , as shown in green area in Fig. 3. When the development time is increased to 75 sec, the range is changed to  $E = 240$  to  $580 \text{ msec}$  ( $84$  to  $203 \text{ mJ}/\text{cm}^2$ ) and  $F = -1.6$  to  $1.0 \mu\text{m}$ , as shown in green area in Fig. 4. However, both results indicate that the OM inspection is not practically suitable for distinguishing different sidewall profiles from the focus distance since the resolu-

**Table 1:** The calculated pattern linewidth difference between designed linewidth ( $l$ ) and trim distance ( $y$ ).

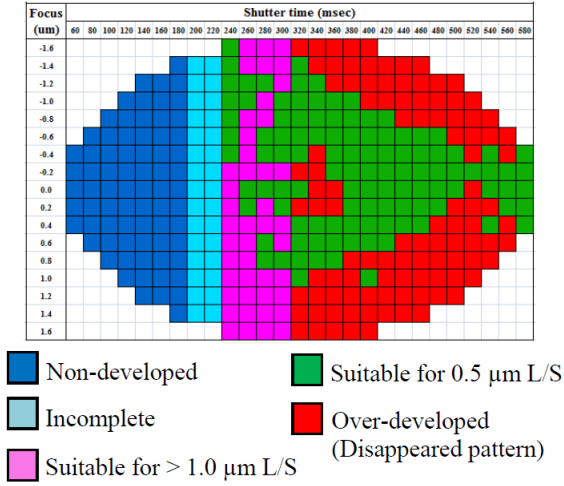
Design CD ( $\mu\text{m}$ )	Target pattern linewidth ( $\mu\text{m}$ )		
	Nominal CD	Maximum CD after 0.4 $\mu\text{m}$ trimming	Maximum CD after 0.9 $\mu\text{m}$ trimming
5.0	5.0	4.60	4.10
4.0	4.0	3.60	3.10
3.0	3.0	2.60	2.10
2.0	2.0	1.60	0.10
1.0	1.0	0.60	No pattern
0.9	0.9	0.50	No pattern
0.8	0.8	0.40	No pattern
0.7	0.7	0.30	No pattern
0.6	0.6	0.20	No pattern
0.5	0.5	0.10	No pattern
0.45	0.45	0.05	No pattern
0.40	0.40	No pattern	No pattern
0.35	0.35	No pattern	No pattern
0.30	0.30	No pattern	No pattern
0.25	0.25	No pattern	No pattern

tion is too low and the characterization of the sidewall profile from the top view is difficult.



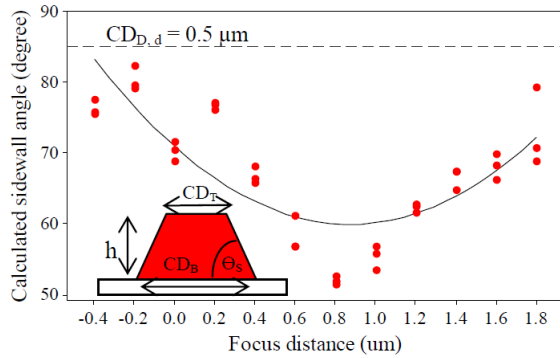
**Fig.3:** The contour  $E$ - $F$  map of the pattern quality check with 60 sec development time.

The larger CDB (at 0% threshold, outer CD) than CDT (at 100% threshold, inner CD) that appears when  $F$  is varied from  $-0.4 \mu\text{m}$  to  $+1.8 \mu\text{m}$  at  $E = 120 \text{ mJ}/\text{cm}^2$ , suggests a strong dependence of the sidewall profile calculated by (2) on the focus distance. The calculated Os in the smiley plot in Fig. 5 depicts that the two extreme focus distances ( $-0.2$  and  $+1.8 \mu\text{m}$ ) are both able to produce the pattern with the average Os greater than 80 degrees but the  $-0.2 \mu\text{m}$  focus distance is preferable because its Os has smaller deviation. Based on the TMECSs process condition for  $0.5 \mu\text{m}$  where  $E$  is  $120 \text{ mJ}/\text{cm}^2$  and  $F$  is  $-0.2 \mu\text{m}$ , the actual linewidths for the pattern sizes greater than  $1 \mu\text{m}$  exhibit a good linearity when compared to the design linewidth as shown in Fig. 6 and all other pattern sizes above  $0.4 \mu\text{m}$  can still be maneuvered



**Fig.4:** The contour E-F map of the pattern quality check with 75 sec development time.

within upper and lower specification limits (USL and LSL)  $\pm 10\%$  of the design pattern size as shown in Fig. 7. Note that the actual linewidths are measured at 50% threshold.



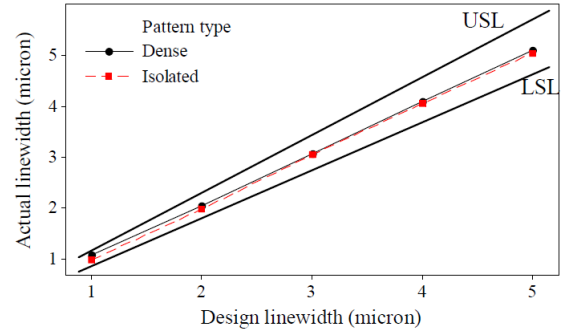
**Fig.5:** Calculated sidewall angle on the 0.5  $\mu\text{m}$  L/S dense pattern by varying the focus distance from -0.4  $\mu\text{m}$  to +1.8  $\mu\text{m}$  ( $E = 120 \text{ mJ/cm}^2$ )

The linear regression equations for dense and isolated patterns with the sizes between 0.5 to 5.0  $\mu\text{m}$  are shown in (3) and (4), respectively. Both equations have the adjusted  $R^2$  of 100%, indicating high correlation between actual linewidth and design linewidth for both patterns.

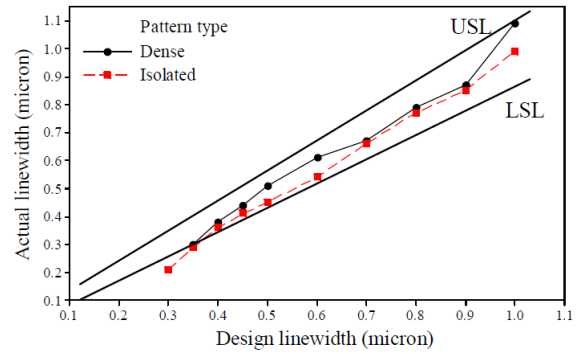
$$CD_D = 1.026CD_{D,d} - 0.01982 \quad (3)$$

$$CD_I = 1.026CD_{I,d} - 0.06174 \quad (4)$$

when  $CD_D$  is actual dense pattern linewidth ( $\mu\text{m}$ ),  
 $CD_{D,d}$  is design dense pattern linewidth ( $\mu\text{m}$ ),  
 $CD_I$  is actual isolated pattern linewidth ( $\mu\text{m}$ ),  
and  $CD_{I,d}$  is design isolated pattern linewidth ( $\mu\text{m}$ ).



**Fig.6:** The relation between actual linewidth and design linewidth (CD is varied from 1.0 to 5.0  $\mu\text{m}$ ).

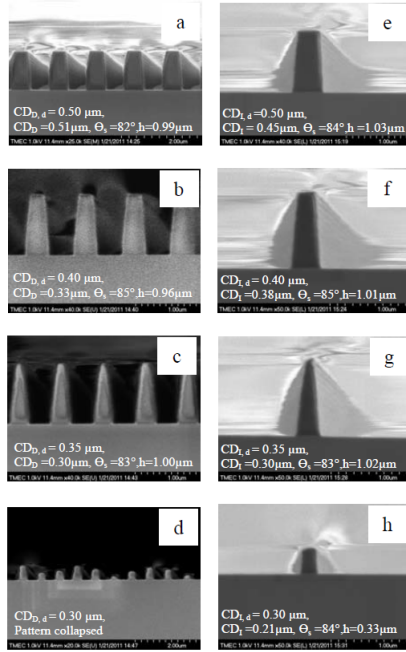


**Fig.7:** The relation between actual linewidth and design linewidth (CD is varied from 0.25 to 1.0  $\mu\text{m}$ ).

The SEM images of the dense pattern in Fig. 8(a) shows that the process condition found earlier can produce a well-formed 0.5  $\mu\text{m}$  pattern. The pattern shape, however, is degraded as the pattern size goes below  $R$  ( $CD < 0.5 \mu\text{m}$ ) and very poor sidewall angle is observed when the pattern size is continuously decreased to near  $\lambda$  ( $CD \sim 365 \text{ nm}$ ) as shown in Fig. 8(b-c), respectively. Apparently, as the pattern size enters a sub-wavelength region ( $CD < 365 \text{ nm}$ ), the developed PR pattern is collapsed; the physical profile is unsustainable and the thickness or PR pattern height ( $h$ ) is non-uniform, as shown in Fig. 8(d). This phenomenon is also observed on the isolated pattern shown in Fig. 8(e-h). The main reason for this collapse is due to the size of the mask pattern that is obviously smaller than the resolution and wavelength of the exposure tool. This results in much higher angle diffraction of the UV light that is incident on and overexposes particularly, the top part of the PR film and finally leads to a significant thickness loss.

### 3.2 Effects of 0.5 $\mu\text{m}$ trimming on the quality of various designed pattern sizes

It appears from both SEM images in Fig. 9(b-c) that PR profiles are well-formed after 0.5  $\mu\text{m}$  trimming. This can actually validate the potential of the Trimming lithography for the smaller than 0.30  $\mu\text{m}$

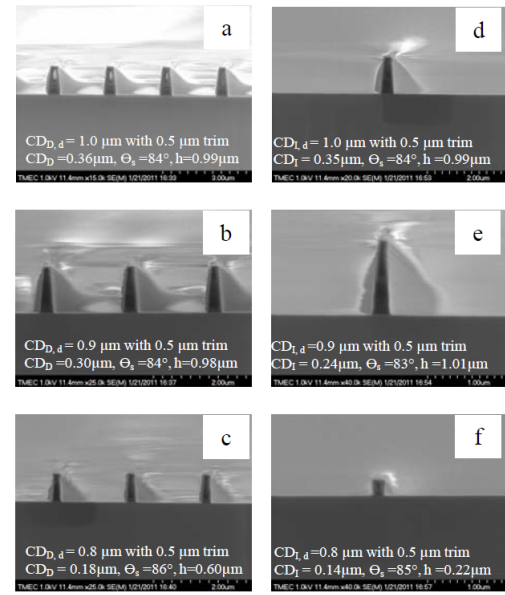


**Fig.8:** SEM images of (a-d) dense pattern and (e-h) isolated pattern, with CD varied from 0.30 to 0.50  $\mu m$  (captured with different magnifications).

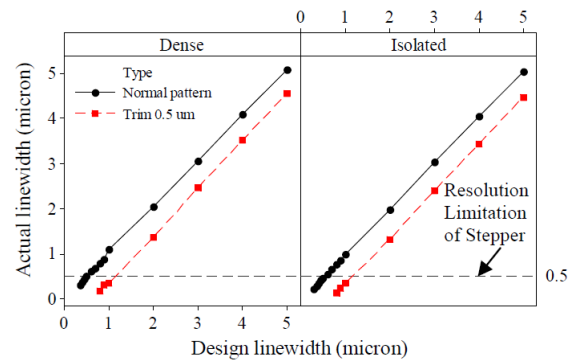
linewidth dense L/S pattern application with no visual of pattern collapsing (compared with the pattern in Fig. 8(c-d)). On the similar process, the isolated pattern with the sizes of 0.24 and 0.14  $\mu m$  can well be produced as shown in Fig. 9(e-f), respectively. Nevertheless, with this approach, the pattern density of both L/S pattern and isolated pattern will inevitably be decreased. The result in Fig. 10 shows that the linewidth increasing rate of the actual CD after 0.5  $\mu m$  trimming is relatively similar to that of the normal pattern without trimming. Moreover, all CD values after trimming are smaller than those of the normal mask pattern and the design linewidth. This means that the concept of trimming lithography to reduce the pattern size from the designed mask pattern is verified. The sidewall angles, shown in Fig. 11, increase with the decrease in pattern size for both dense and isolated patterns. From this experiment, it is found that the trimming exposure energy has a little effect on the final PR film thickness except when the trimmed pattern size becomes smaller than the exposure wavelength, where the PR film thickness is rapidly decreased as shown in Fig. 12. The PR thickness loss observed in both cases is, possibly caused by some diffraction of the UV light.

### 3.3 Effects of trimming distance to the pattern quality

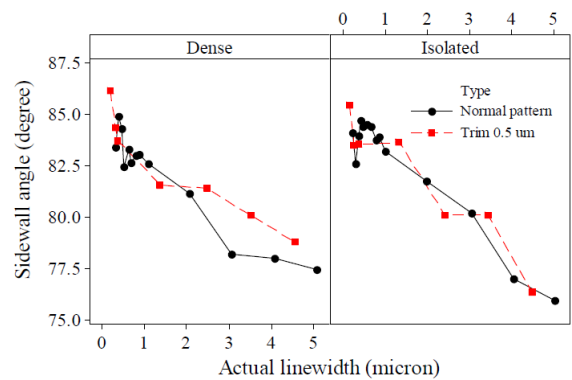
Fig. 13 shows the relation between the actual linewidth vs. The design linewidth at different trimming distances. It is found that the normal pat-



**Fig.9:** SEM images of (a-c) 0.5  $\mu m$  trim dense patterns, (d-f) 0.5  $\mu m$  trim Isolate pattern (captured with different magnifications).

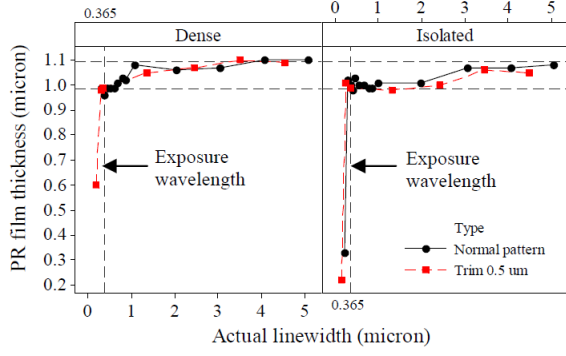


**Fig.10:** The relation between actual linewidth and design linewidth with and without 0.5  $\mu m$  trimmed.



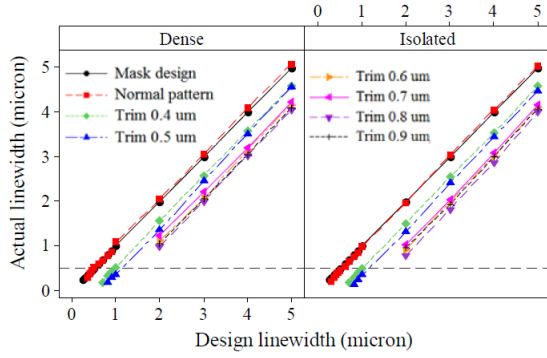
**Fig.11:** The relation between sidewall angle and actual linewidth with and without 0.5  $\mu m$  trimming.





**Fig.12:** The relation between PR remaining thickness and actual linewidth with and without  $0.5 \mu\text{m}$  trimming.

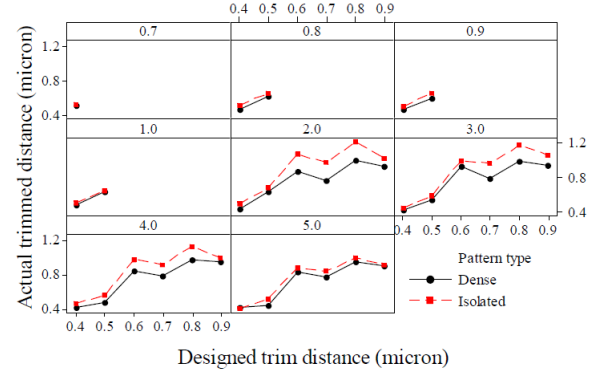
tern linewidth is relatively close to the mask design linewidth for both dense L/S and isolated patterns and the trimmed pattern linewidth decreases proportionally to the design.



**Fig.13:** The plots between actual linewidth and design linewidth ( $CDD, d$  and  $CDI, d$  are varied from  $0.25$  to  $5.0 \mu\text{m}$  and trimmed from  $0.4$  to  $0.9 \mu\text{m}$ ).

The plots in Fig. 14 show the relation between the actual trimmed distance, extracted from the actual linewidth, and the designed trimming distance. Based on a visual inspection, the pattern sizes below  $0.7 \mu\text{m}$  can no longer be reduced by this experimental range, thus they are omitted here. It is further seen that the patterns between  $0.7$  and  $1.0 \mu\text{m}$  disappear for both dense L/S and isolated patterns as the trimming distance exceeds  $0.5 \mu\text{m}$ . This is possibly explained by referring to the earlier result shown in Fig. 9(f) that when the trimmed pattern size enters the exposure sub-wavelength and the diffraction of the UV light becomes a factor, the PR will obviously experience a thickness loss. This experimental result provides an additional indication that the severe PR loss will tend to occur when the trimming distance exceeds approximately 50% of the designed pattern linewidth and the PR will mostly disappear after the development. From these results, it can be implied that the trimming distance for a sub-micron

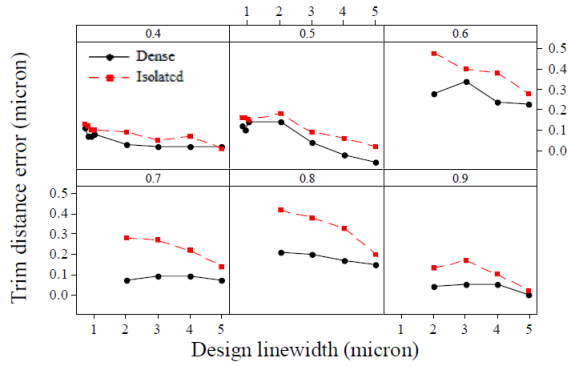
design pattern should be relatively smaller than its half-linewidth.



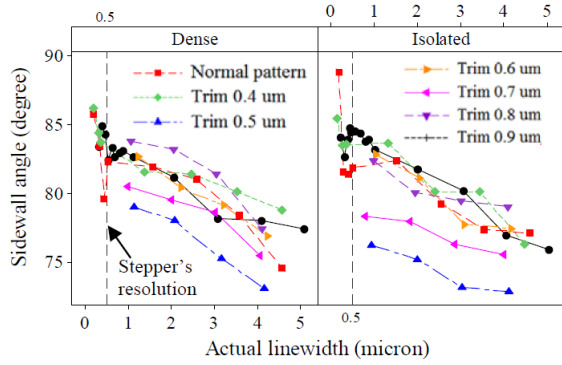
**Fig.14:** The plots between actual trimmed distance and designed trim distance ( $CD_{D,d}$  and  $CD_{I,d}$  are varied from  $0.25$  to  $5.0 \mu\text{m}$ ).

The plots in Fig. 14 also show that the actual trimmed distance of the isolated pattern is in overall higher than that of the dense L/S pattern. This is probably due to different diffraction characteristics between L/S dense and isolated patterns through the mask slit where the exposure area on the isolated pattern is theoretically larger than that of the L/S dense pattern. In addition, these diffraction characteristics do not depend on the exposure dose. The result in Fig. 15 shows the relation between the trim distance error and the design pattern linewidth. The trim distance error is somewhat greater as the design size decreases and the trim distance error is higher for the isolated pattern. This can be explained by the difference of the light diffraction between L/S dense and isolated patterns as mentioned above [7]. The sidewall angle after trimming with the sub-micron pattern is in average greater than  $75^\circ$ . However, when the actual linewidth decreases to a sub-resolution of the stepper ( $< 0.5 \mu\text{m}$ ), the sidewall angle reaches as steep as  $85^\circ$  as seen from Fig. 16.

Moreover, the relation between the final PR film thickness and the actual linewidth in Fig. 17 shows that the trimmed pattern with the size above the exposure wavelength ( $> 365 \text{ nm}$ ) can still maintain the PR film thickness loss within 10% of the initial film thickness. However, the PR film suffers a severe loss when the trimmed pattern size enters a sub-exposure wavelength region ( $< 365 \text{ nm}$ ), similar to the result observed earlier in Fig. 9(c) and 9(f). It is to point out that the slope of a developed pattern is in general non-uniform and a smaller slope at the upper area due to higher exposure and more contact with the developer is expected. Therefore in the case where the pattern size enters subresolution and sub-exposure wavelengths, the higher portion due to higher angle diffraction of the UV light will remarkably affect the PR film in the upper area which will easily remove it after the development. On the other hand, the lower

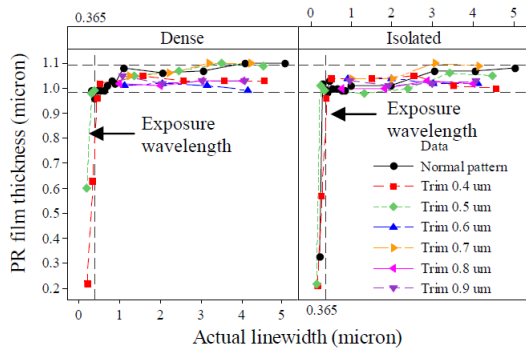


**Fig.15:** 15: The plots between trim distance error and design linewidth ( $CD_{D,d}$  and  $CD_{I,d}$  are varied from 0.25 to 5.0  $\mu\text{m}$  and trimmed from 0.4 to 0.9  $\mu\text{m}$ ).



**Fig.16:** The plots between sidewall angle and actual linewidth ( $CD_{D,d}$  and  $CD_{I,d}$  are varied from 0.25 to 5.0  $\mu\text{m}$  and trimmed from 0.4 to 0.9  $\mu\text{m}$ ).

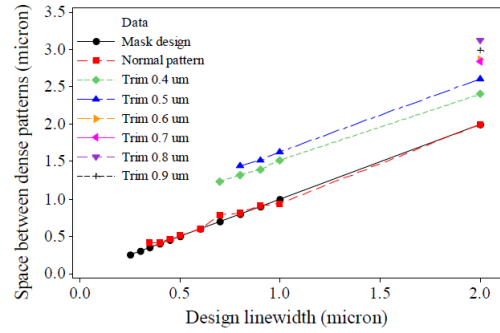
area with the larger slope is not much affected it thus stands and the overall sidewall angle of these developed features become higher than those with larger patterns.



**Fig.17:** The plots between PR film thickness after development and actual ( $CD_{D,d}$  and  $CD_{I,d}$  are varied from 0.25 to 5.0  $\mu\text{m}$  and trimmed from 0.4 to 0.9  $\mu\text{m}$ ).

It is clearly illustrated in Fig. 13 that the trimmed

dense L/S pattern linewidth actually decreases as the trimming distance increases. The opposite phenomenon for the space between patterns is observed as shown in Fig. 18. This implies that the trimmed pattern density is indeed smaller than that of the pattern prepared by the conventional lithography. The alternative solution for pattern density improvement is to integrate the Trimming lithography with the double patterning technique [8].



**Fig.18:** The plots of spacing between dense pattern and linewidth ( $CD_{D,d}$  and  $CD_{I,d}$  are varied from 0.25 to 5.0  $\mu\text{m}$  and trimmed from 0.4 to 0.9  $\mu\text{m}$ ).

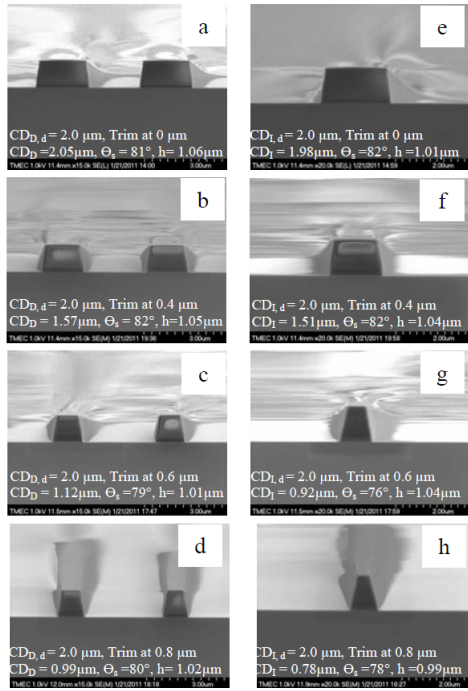
The 2  $\mu\text{m}$  designed pattern is applied next to observe the effects of the trimming distance to the pattern quality. SEM images in Fig. 19 exhibit a monotonic decrease of the trimmed linewidth with the trimming distance. From the SEM inspection of the profile after trimming, it is found that the trimmed pattern with the linewidth equal to the stepper resolution as shown in Fig. 20 is well -formed.

Moreover, the profile of trimmed patterns with the subresolution and sub-exposure wavelength sizes appear to be better than the patterns developed from those obtained from the traditional process, as shown in Fig. 21 and Fig. 22, respectively.

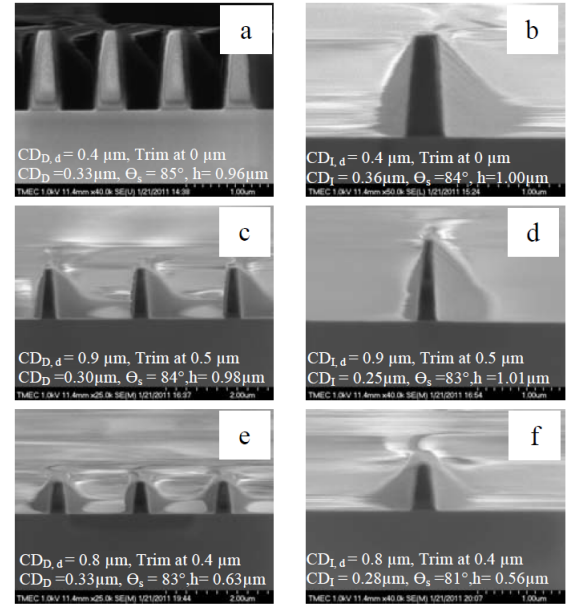
In particular, Fig. 22(e) shows that the dense pattern can be trimmed down to 0.18  $\mu\text{m}$  from the original 0.8  $\mu\text{m}$  and 0.5  $\mu\text{m}$  trim distance with the acceptable profile. The better appearance of the trimmed pattern profile is probably due to the unidirectional trimming. Since the lensSs system is configured such that the light path is straight and directed normal to the PR surface, the upper area of the PR film is therefore typically exposed at a higher degree than the lower area, finally resulting in the trapezoid developed feature [7]. Once the trimming takes place by shifting a wafer for a certain distance, the PR film in the lower area becomes more exposed, making the final slope steeper and the pattern is thus in a better shape.

#### 4. CONCLUSION

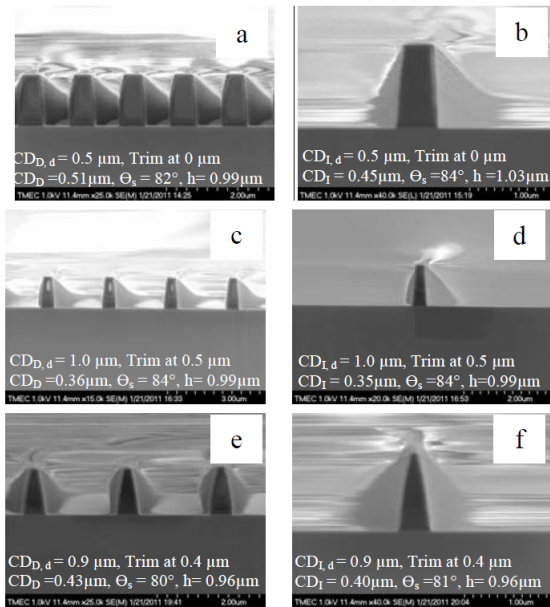
Trimming lithography is a powerful technique to produce a sub-resolution and sub-wavelength pattern



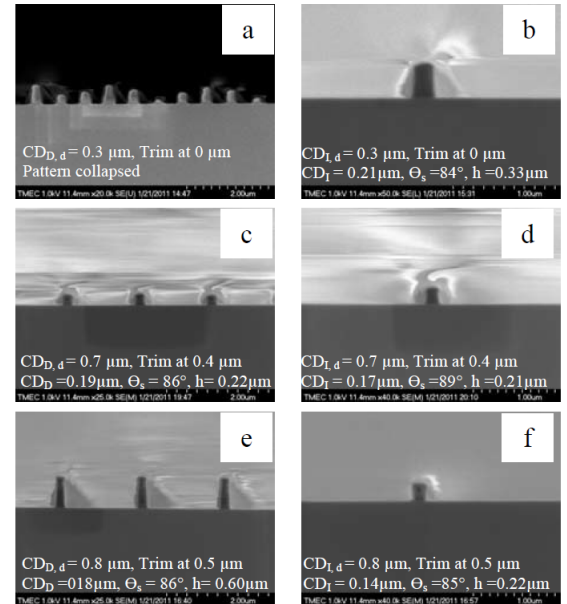
**Fig.19:** SEM images of (a-d) dense pattern, (e-h) isolate pattern with 2  $\mu\text{m}$  design linewidth and trimmed at 0, 0.4, 0.6, and 0.8  $\mu\text{m}$ , respectively.



**Fig.21:** SEM images of dense L/S and isolated patterns with the target size smaller than 0.5  $\mu\text{m}$  (sub-resolution); (a-b) 0.4  $\mu\text{m}$  without trimming, (c-d) 0.9  $\mu\text{m}$  with a 0.5  $\mu\text{m}$  trim, and (e-f) 0.8  $\mu\text{m}$  with a 0.4  $\mu\text{m}$  trim.



**Fig.20:** SEM images of dense L/S and isolated patterns with the target size equal to the stepper resolution (0.5  $\mu\text{m}$ ); (a-b) 0.5  $\mu\text{m}$  without trimming, (c-d) 1.0  $\mu\text{m}$  with a 0.5  $\mu\text{m}$  trim, and (e-f) 0.9  $\mu\text{m}$  with a 0.5  $\mu\text{m}$  trim.



**Fig.22:** SEM images of dense L/S and isolated patterns with the target size smaller than 365 nm (sub-wavelength); (a-b) 0.3  $\mu\text{m}$  without trimming, (c-d) 0.7  $\mu\text{m}$  with a 0.4  $\mu\text{m}$  trim, and (e-f) 0.8  $\mu\text{m}$  with a 0.5  $\mu\text{m}$  trim.



by using the traditional binary intensity mask. It can effectively scale down the dense pattern size to  $0.18\ \mu\text{m}$ , which is a sub-wavelength pattern by using a  $0.8\ \mu\text{m}$  mask pattern with a  $0.5\ \mu\text{m}$  trim distance. However, the trimmed pattern density obviously decreases in all cases. The pattern density improvement using Trimming lithography as well as the effects of PR film thickness, and the line edge roughness will be furthered studied in the future.

## 5. ACKNOWLEDGEMENT

The authors would like to thanks COAX group Corp. Ltd. for the SEM analysis, and thanks to all TMECSs staffs who supported this research work.

## References

- [1] R.F. Pease and S.Y. Chou, "Lithography and other patterning techniques for future electronics," *Proc. of the IEEE*, vol. 96, no. 2, pp. 248–270, February 2008.
- [2] ITRS Reports. (2011, July). ITRS 2010 Update. [Online]. Available: <http://www.itrs.net/reports.html>
- [3] B.J. Lin, "Optical lithography's present and future challenges," *C. R. Physique*, vol. 7, pp. 858–874, 2006.
- [4] K. Ronse, "Optical lithography's historical perspective," *C. R. Physique*, vol. 7, pp. 844–857, 2006.
- [5] L. Guo, "Nanoimprint lithography: methods and material requirements," *Adv. Mater.*, vol. 19, pp. 495–513, 2007.
- [6] R. S. Ghaida, G. Torres, and P. Gupta, "Single-Mask Double-Patterning Lithography," *Proc. of SPIE*, vol. 7488, pp. 74882J-1–74882J-11, 2009.
- [7] C. A. Mack, *Field guide to optical lithography*, SPIE field guides, vol. FG06, John E. Greivenkamp publisher, Series Editor, 2006.
- [8] B. Hwang, J. Han, M-C. Kimt, S. Jung, N. Lim, S. Jin, Y. Vim, D. Kwak, J. Park, J. Choi, and K. Kim, "Comparison of double patterning technologies in NAND flash memory with sub-30nm node," *IEEE*, ISBN 978-1-4244-4353-6, 2009.



**Nithi Atthi** received his B.Eng. degree in materials engineering and M.S. degree in industrials engineering (Engineering management) from Kasetsart University, Bangkok, Thailand, in 2004 and 2008, respectively. He has been a researcher at National Electronics and Computer Technology Center (NECTEC), Thailand since 2004. His research interests are Photolithography Process, Photomask Fabrication, Ultra-

Hydrophobic Surface, Hard-Disk Drive Manufacturing, Process Optimization, and High-K Dielectric Materials for CMOS Process. He has published 86 international conference and journal papers.



**Arreerat Sriklad** received her B. Eng. degree in Electronics and Telecommunication from Pathumwan Institute of Technology, Bangkok Thailand, in 2007. She received her M.S. degree in Electrical engineering from King Mongkut's University of Technology Thonburi in 2011. Her research interest is in photolithography process.



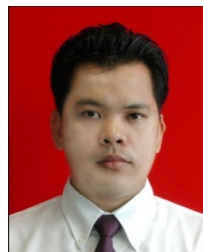
sensors and ENFETs.

**Wutthinan Jeamsaksiri** received a Master degree and a Ph.D. in Electrical and Electronics Engineering degrees from Imperial college, London in 1996 and 2002, respectively. He is now working at Thai Microelectronics Center, NECTEC, NSTDA Thailand since 2005. His research interest is in Si micro-sensors compatible with CMOS process. The sensors of interest are pressure sensors, ISFET based sensors including pH



Electronic and Computer Technology Center (NECTEC), Thailand.

**Charndet Hruanun** received the B.Sc degree in Biology from Ramkhamhaeng University in 1988 and M.Sc degree in Biotechnology from King Mongkut's University of Technology Thonburi in 1994. His research is emphasized on fabrication and characterization of semiconductor device, microfabrication technology on integrated circuit. He is currently working at Thai Microelectronic Center (TMEC) as part of National



**Amporn Poyai** was born in 1969 in Pathum-thani, Thailand. He received the Bachelor of Science (B.Sc.) degree in physics in 1991 from Silpakorn University, the Master of Engineering (Electrical Engineering) (M.Eng. (E.E.)) degree in 1994 from King Mongkut's Institute of Technology Ladkrabang (KMITL), both in Thailand. In 1998 and 2002, respectively, he obtained the Master and Ph.D. in electrical engineering from Katholieke Universiteit Leuven (KU Leuven) in Belgium. In 1994, he joined National Electronics and Computer Technology Center (NECTEC) of Thailand, where he has been involved in the nation microelectronics project. Since 1997, he has got scholarship from Thai government supported through the National Science and Technology Development Agency (NSTDA) of Thailand. In 1997, he joined the Interuniversitaire Micro-Electronica Centrum (IMEC) in Belgium to do his master and doctoral research under the direction of Prof. C. Claeys. His research covers the field of device physics and defect engineering. From December 2002, he is with Thai Microelectronics Center (TMEC) under NECTEC's project. Presently, he is a director of TMEC.



**Rardchawadee Silapunt** received her B.Eng. degree in electrical engineering from Chulalongkorn University, Bangkok, Thailand, in 1996, M.S. and Ph.D. degrees in electrical engineering from University of Wisconsin-Madison in 1998 and 2004, respectively. She is currently a lecturer at King Mongkut's University of Technology Thonburi in Thailand. Her current research interests

are Thin Film Processing, Electromagnetic Phenomena, Microwave Heaters, and Microwave Communications.