A Novel Single Phase AC-AC Converter with Power Factor Control

Suwat Kitcharoenwat[1],
Mongkol Konghirun[2], and **Anawach Sangswang**[3], Non-members

ABSTRACT

This paper presents a novel single-phase ac-ac converter topology that is capable of creating voltage output to buck or boost mode. The structure of topology uses minimal switches controlled with the two-section overlap in each cycle of the ac input. The proposed topology is simple, low-cost, and contains minimum number of device. The control strategy can regulate a wide output voltage range with low harmonic distortion and improve the power factor. The closed-loop control is divided into two parts. The first part is the voltage control of dual dc-link capacitors, and the second part controls the ac output voltage. In the part of voltage control at the dc-link capacitors, the switches operate in the boost mode. The ac input current is controlled by PID control with the aim for power factor correction. The output voltage is regulated by the PID control where the sinusoidal pulse-width modulation (sPWM) technique is chosen. Simulation and experimental results confirmed the output voltage regulation, the control of the charging dual dc-link voltage capacitors, the responses to the input voltage and load changes.

Keywords: AC-AC Converter, Continuous Current Mode (CCM), Power Factor, Single-phase AC-AC Converter, Buck-boost Capability

1. INTRODUCTION

An ac-ac converter has widely been used in industry to replace auto-transformers because of the ability for better control. The ac voltage is converted to another ac voltage through a variety of topologies such as full-bridge, and half-bridge converters with the dc-link [1]-[4], ac chopper [5], ac-ac resonant converter [6] or ac-ac converter using Z source network [7]-[8]. The full-bridge and half-bridge structures are among the popular choices in the UPS applications (1-phase or 3-phase applications) [1]-[2]. These topologies consist of three parts namely, rectifier, dc bus controller and output voltage drivers, generally separated from the control of the switches. An ac chopper topology is a buck converter that controls the output voltage by adjusting the PWM duty cycle. Even though the PWM control is not complex, the zero-crossing of the output voltage may cause a great distortion and its operation is limited to the boost mode.

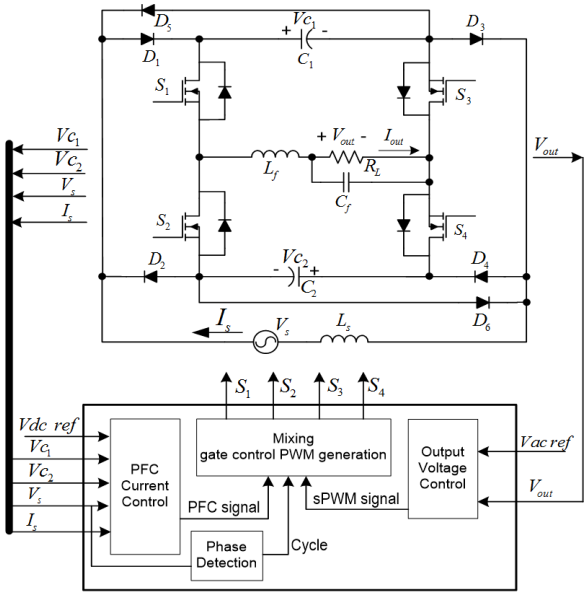

Fig.1: *The proposed system ac-ac converter.*

The resonant converter topology converts an ac signal to another form of ac signal through the resonance of the stored energy in the inductors and capacitors.

Recent work on the ac-ac converter uses an impedance network consisting of inductors and capacitors as energy storages combined into Z source topology [8]. The converter is operated by adjusting the PWM duty cycle to control the output voltage while operating with input power factor close to unity. The major disadvantage lies in the transient response.

This paper presents a new ac-ac converter topology with the capability of operation in both buck and boost modes. The converter circuit configuration is shown in Fig.1. The converter uses four switches to

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[1] The author is with Department of Computer Engineering, King Mongkut's University of Technology Thonburi, Faculty of Engineering,Tungkru, Bangkok, 10140, Thailand., E-mail: sw_rojn@yahoo.com

[2,3] The authors are with Department of Electrical Engineering, King Mongkut's University of Technology Thonburi,Faculty of Engineering,Tungkru, Bangkok, 10140, Thailand., E-mail: mongkol.kon@kmutt.ac.th and anawach.san@kmutt.ac.th

control the output voltage and the input current. The output voltage is generated by using sPWM technique to generate pulses from dual dc-link capacitors. The operation of the switches controls the output voltage and input current to the desired values. The gate control signals are created from two close-loop controls, the output voltage and the input current.

2. PROPOSED SYSTEM

The proposed ac-ac converter topology in Fig.1, consists of four switches S_1 - S_4, two dc-link capacitors C_1 and C_2, an inductor L_S, and six diodes D_1 - D_6. A wide range of adjustable ac output voltage can be generated where the frequency may differ from the input signal. The input current is controlled to charge the dual voltage dc-link capacitors where the power factor remains close to unity. The first part of operations, the switches control the charging of dc-link capacitors C_1 and C_2 in each cycle of the input voltage. The peak voltage is higher than the peak voltage of input signal. The structure of topology consists of two pairs of series, switches S_1 and S_2 and switches S_3 and S_4, operating in the boost manner. The dc-link voltage across C_1 is charged during the positive cycle of the input voltage and the dc-link voltage across C_2 is charged in the negative cycle.

The second part of operations is output signal generation by using bipolar sPWM technique. The positive voltage pulses are obtained from the dc-link voltage across C_1 and negative voltage pulse are obtained from the dc-link voltage across C_2.

2.1 Rectifier/Boost Converter Operation

This section aimed to control the dc-link voltages across capacitors C_1 and C_2 by rectifying the input voltage. The dc voltage level is boosted to the desired level while the power factor is maintained close to unity. Fig. 2 shows the equivalent circuit of the boost converter. When the input voltage is positive, the inductor L_S is charged through both switches S_1 and S_2. After the switches S_1 or S_2 are turned off, the energy storage in the inductor L_S is discharged to the dc-link capacitor C1. Similarly in Fig. 3, during the negative half cycle, the inductor L_S is charged through the switches S_3 and S_4, and discharged to the dc-link capacitor C2 by turning off switches S3 or S4. The voltage across the inductor L_S can be expressed as

$$V_{Ls} = L_s \frac{dI_s}{dt} = V_s \tag{1}$$

where

$$V_s = V_m \cdot \sin(\omega t), 0 < \omega t < 2\pi \tag{2}$$

When the inductor L_S current discharges in positive cycle and negative cycle of the input voltage, the voltage across the inductor L_S is

$$V_{Ls} = L_s \frac{dI_s}{dt} = V_s - V_c \tag{3}$$

where

$$V_s = V_m \cdot \sin(\omega t), 0 < \omega t < 2\pi \tag{4}$$

2.2 DC/AC Inverter Operation

The output voltage control uses the bipolar sPWM technique by turning on switches S_1 and S_2 to apply the positive voltage from the dc-link capacitor C_1 to the output, and turning on the switches S_3 and S_4 to apply the negative voltage from dc-link capacitor C_2 to the output.

The operations of the sPWM are shown in Fig.4 where the circuit configuration switches alternately. It can be seen that the pairs of switches S_1, S_2 and switches S_3, S_4 are operated in the positive input signal, the switches S_1 and S_3 will be turned on simultaneously to charge the current L_S.

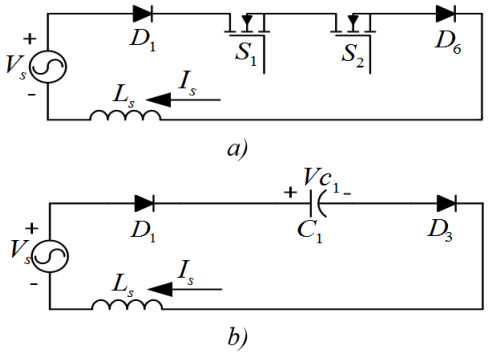

Fig.2: *Positive cycle a) charging and b) discharging inductor current.*

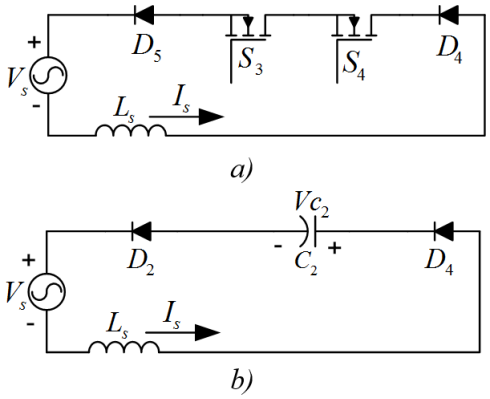

Fig.3: *Negative cycle a) charging and b) discharging inductor current.*

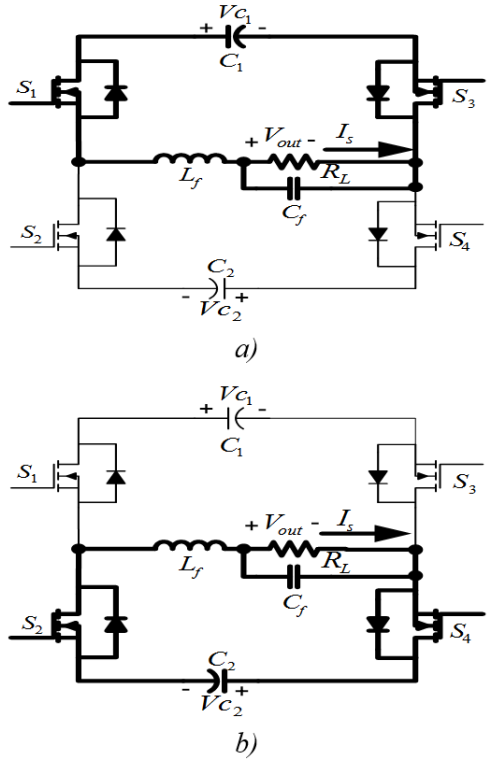

Fig.4: *Circuit configurations under a) positive and b) negative pulses of bipolar sPWM operation.*

3. CONTROL STRATEGY

The control of the circuit is separated into two parts. The first part is the input current control for power factor correction and the dual dc-link voltage control. The reference signal in this part is derived from the ac input voltage signal while the PID controller updates the PFC drive signal. The block diagram of this part is shown in Fig.5.

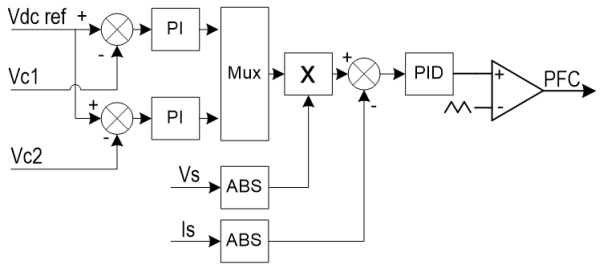

Fig.5: *Block diagram for PFC current control.*

The second block diagram is the output voltage control by using the bipolar sPWM. In this part, the sinusoidal waveform is used as the reference signal. The output voltage is fed back to the process through the PID controller to update the sPWM signal. The block diagram of this part is shown in Fig.6.

In the mixing gate control signals block, there are two mixing controls, sPWM signals and PFC signal

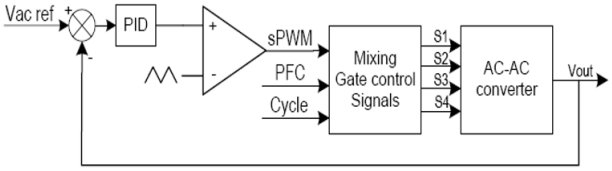

Fig.6: *Block diagram for output voltage control.*

(ac input current control). The mixing of gate control signals can be obtained as follows,

$$S_1 = sPWM\ OR\ (PFCANDCycle) \quad (5)$$
$$S_2 = \overline{sPWM}\ OR\ (PFCANDCycle) \quad (6)$$
$$S_3 = sPWM\ OR\ (PFCAND\overline{Cycle}) \quad (7)$$
$$S_4 = \overline{sPWM}\ OR\ (PFCAND\overline{Cycle}) \quad (8)$$

The implementation of the control algorithm for the input current and output voltage is shown in the flowchart in Fig.7. The control starts by reading all feedback signals, filtering and phase detection of the input signal. The input current control computes the period of PFC PWM signal through the dc-link voltage. The output voltage control is generated by comparing the sensed output signal with the reference signal, generated by the controller and synchronized with input voltage. Finally, the output signals, sPWM, PFC PWM and phase cycle signals are updated and send to the external gate signal mixing circuit.

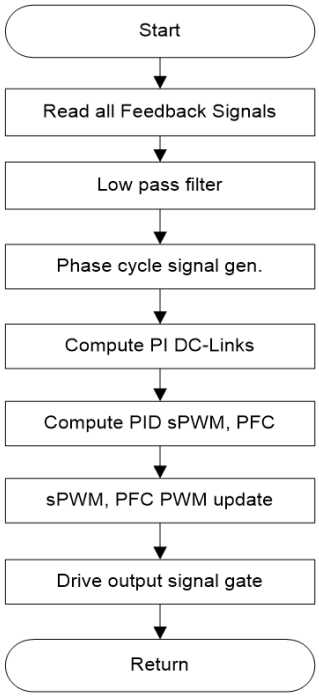

Fig.7: *Control algorithm of input current and output voltage.*

4. SIMULATION RESULTS

The proposed topology has been validated through a computer simulation study. The following circuit parameters in Fig. 1 are used: f_s=20 kHz, C_1=C_2=6,000μF, L_s=10mH, R_L= 100, 50Ω, L_f= 600μH, C_f=10μF, V_s=220Vrms 50Hz. The input current is controlled to charge the dc-link capacitors C_1 and C_2 to the level of 400V. Note that the dc-link voltage contains a small ripple. The simulated dc-link waveforms are shown in Fig. 8.

Figs.9 and 10 show the simulation results of output voltage control at 120 Vrms in buck mode with the load at 40W and 96W, respectively. Note that the reference signal for the input current control is derived from the input voltage signal. Similarly, Figs. 11 and 12 show the output voltage control in boost mode at 270Vrms with the load at 140W and 270W, respectively. Figs.13 and Fig 14 show the output voltage control where the input voltage is equal to the output voltage at 220Vrms with load of 100W and 200W, respectively.

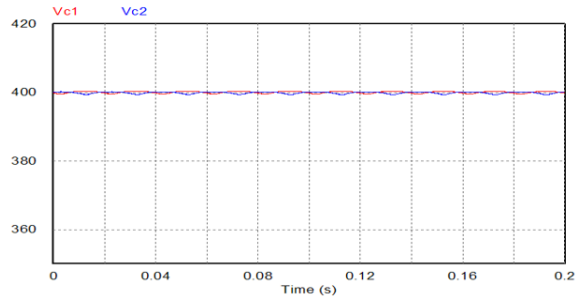

Fig.8: *Simulation results for the dc bus voltage Vc1 and Vc2.*

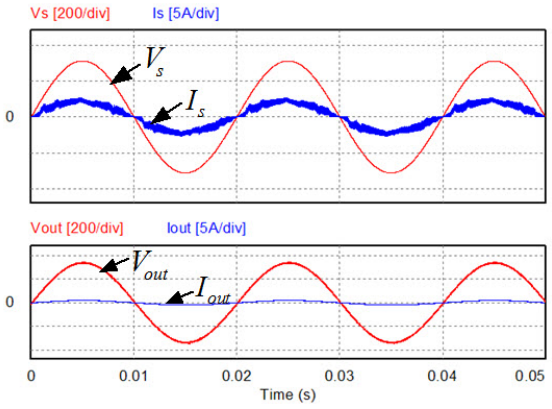

Fig.9: *Input current control (upper traces) and output voltage control (lower traces) at 120Vrms with 40W load in buck mode.*

According to these simulation results in Figs. 9 through 14, total harmonic distortion of input ac current (THDi) and power factor are summarized in Table 1. As seen, the THDi and power factor have been

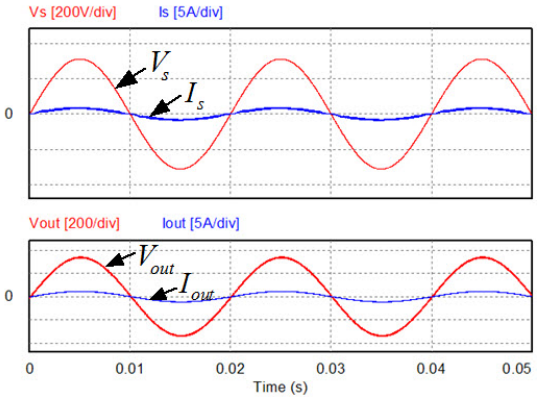

Fig.10: *Input current control (upper traces) and output voltage control (lower traces) at 120Vrms with 96W load in buck mode.*

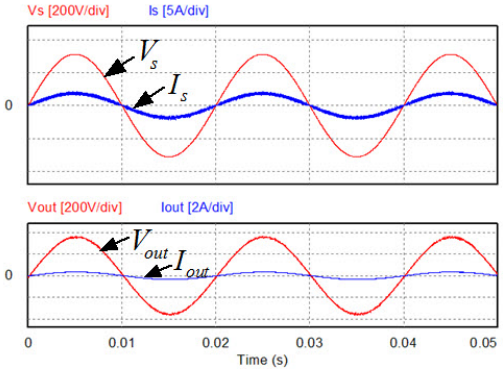

Fig.11: *Input current control (upper traces) and output voltage control (lower traces) at 270Vrms with load 140W in buck mode.*

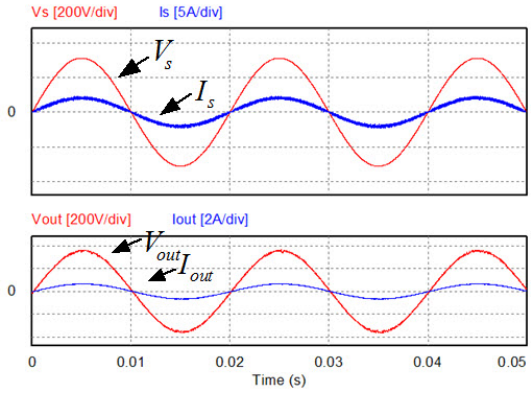

Fig.12: *Input current control (upper traces) and output voltage control (lower traces) at 270Vrms with load 270W in buck mode.*

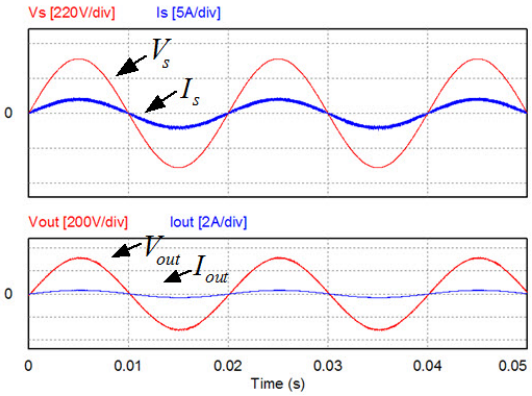

Fig.13: *Input current control (upper traces) and output voltage control (lower traces) at 220Vrms with load 100W.*

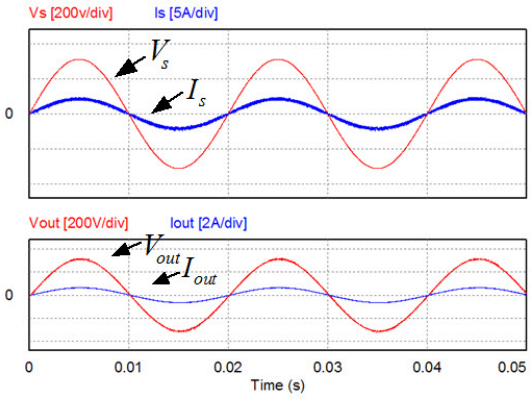

Fig.14: *Input current control (upper traces) and output voltage control (lower traces) at 220Vrms with load 200W.*

calculated to show the performance of proposed PFC.

Table 1: *Simulation results for total harmonic distortion of input ac current and power factor.*

	Fig.9	Fig.10	Fig.11	Fig.12	Fig.13	Fig.14
THDi(%)	0.188	0.104	0.085	0.076	0.080	0.079
PF(lagging)	0.980	0.994	0.996	0.997	0.997	0.996

5. EXPERIMENTAL RESULTS

A novel single phase ac-ac converter has been implemented. A hardware prototype used a 32-bit fixed-point microcontroller. The feedback signals are sent to the microcontroller by using a 12-bit analog-to-digital converter. The single-chip microcontroller receives the feedback signals to process and generate the gate signals to drive the single phase ac-ac converter. The switching frequency of the gate signal is at f_s= 20 kHz. The dead time is set to 1 μs.

The laboratory prototype is designed for 500W with 220V, 50Hz input voltage. The switching devices used GREEGOO G50-12CS1 IGBTs and the gate drive devices used SHARP PC923L0NSZ0F. The dc-link voltage is regulated at 400V. The output voltage range is from 0V to 282V. The power semiconductor switches are IGBTs operating with a carrier frequency of 20 kHz. The key component parameters are shown in Table 2.

Table 2: *System Parameters.*

Parameters	Value	Parameters	Value
L_S	600μH	V_S	220V/50Hz
C_1	6,000μF	V_{out}	0-282V/50Hz
C_2	6,000μF	Vc_1	400V
C_f	3μF	Vc_2	400V
L_f	600μH	f_s	20kHz

Figs.15 and 16 show experimental results for the ac input current and ac output voltage control in buck mode. The ac voltage output is controlled at 120 Vrms and supplied to a resistive load. The input current is operated in the continuous conduction mode (CCM). The ac output voltage is controlled to synchronize with ac input. Figs.17 and 18 show the experimental results of the boost mode operation. The output voltage is regulated at 270Vrms and supplied to the resistive load. Figs.19 and 20 show the experimental results of output voltage control where the input voltage is equal to the output voltage at 220Vrms with load of 100W and 200W, respectively.

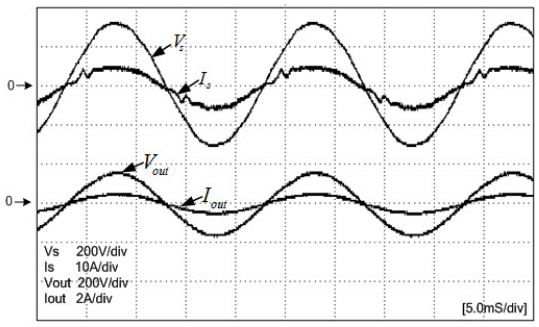

Fig.15: *Experimental results for input current control and output voltage control at 120Vrms with load 40W in buck mode.*

Similarly, both THDi and power factor from experimental results in Figs. 15 through 20 are measured and shown in Table 3. Referring to THDi in simulation results in Table 1, the THDi in experimental results in Table 3 are higher. Because the ideal inductor L_S is used in simulations, while the actual inductor made by toroid core with iron power material has hysteresis and resistive losses. The magnetically nonlinear operation due to core saturation also requires the higher bandwidth of current control from the PID controller.

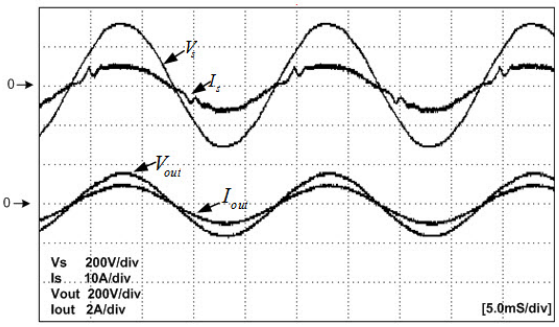

Fig.16: *Experimental results for input current control and output voltage control at 120Vrms with load 96W in buck mode.*

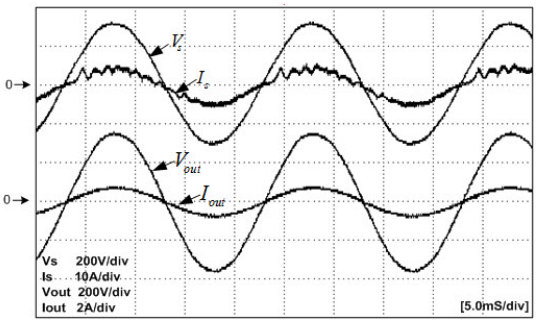

Fig.17: *Experimental results for input current control and output voltage control at 270Vrms with load 140W in boost mode.*

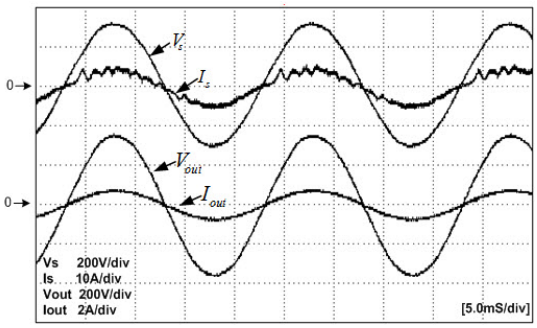

Fig.18: *Experimental results for input current control and output voltage control at 270Vrms with load 270W in boost mode.*

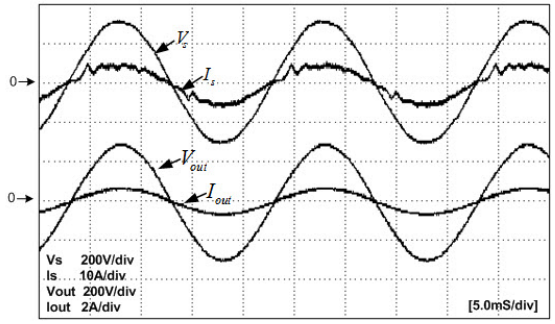

Fig.19: *Experimental results for input current control and output voltage control at 220Vrms with load 100W in normal mode.*

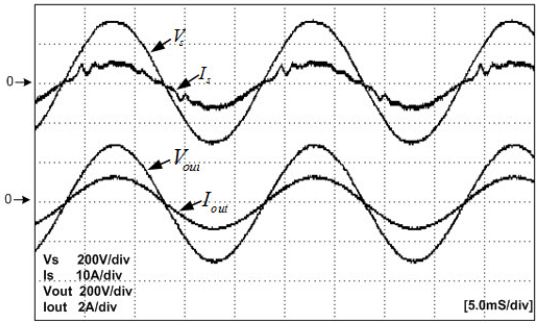

Fig.20: *Experimental results for input current control and output voltage control at 220Vrms with load 200W in normal mode.*

Table 3: *SExperimental results for total harmonic distortion of input ac current and power factor.*

	Fig.15	Fig.16	Fig.17	Fig.18	Fig.19	Fig.20
THDi(%)	9.3	9.2	12.1	11.1	11.2	11.6
PF(lagging)	0.988	0.990	0.978	0.987	0.985	0.988

6. CONCLUSION

This paper proposes a new type of ac-ac converter for improving the performance of converter through the input current and the output voltage. The topology requires less number of power switches. It can be operated in both input current and output voltage controls. The proposed topology has sinusoidal input line current with unity power factor and high quality output voltage under various load values. The proposed topology requires only four switches and operates by the mixing gate signals from two close-loop controls. The simulation and experimental results confirm the validity of the proposed topology under different output voltage levels and load values.

7. ACKNOWLEDGEMENT

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Suwat Kitcharoenwat was born in Songkhla, Thailand. He received the B.Eng. degree from the Rajamangala Institute of Technology Thanyaburi, Pathum thani, in 2000 and the M.S. degrees from King Mongkut's University of Technology Thonburi (KMUTT), Bangkok, Thailand, in 2007.He is currently working toward the Ph.D. degree in electrical and computer engineering. His research interests include electronic converters, and switch-mode power supplies.

Mongkol Konghirun received a B.Eng in Electrical Engineering from King Mongkut's University of Technology Thonburi, Thailand in 1995. And he received M.Sc. and Ph.D. degrees in Electrical Engineering from the Ohio State University, USA in 1999 and 2003, respectively. Presently, he is an Assistant Professor at department of Electrical Engineering, King Mongkut's University of Technology Thonburi. His research interests include electric motor drives and renewable energy.

Anawach Sangswang was born in Bangkok, Thailand. He received the B.Eng. degree from the King Mongkut's University of Technology Thonburi (KMUTT), Bangkok, in 1995 and the M.S. and Ph.D. degrees from Drexel University, Philadelphia, Pennsylvania, USA, in 1999 and 2003, respectively. He is currently an Assistant Professor with the Department of Electrical Engineering, KMUTT. His research interests include stochastic modeling, digital control of power electronic converters, and power system stability.