2.4-GHz Band Ultra-Low-Voltage LC-VCO IC in 130-nm CMOS

Xin Yang*, **Kangyang Xu***, **Wei Wang***,
Yorikatsu Uchida*, and **Toshihiko Yoshimasu***[1], Non-members

ABSTRACT

An ultra-low-voltage LC-VCO IC has been demonstrated using 130nm CMOS technology. The LC-VCO IC includes a cross-coupled NMOS pair, a single symmetric inductor, AMOS varactors with capacitor ac coupling and a buffer amplifier. The LC-VCO IC is designed, fabricated and fully evaluated on wafer. The VCO IC exhibits measured frequency tuning range of 17.4% and phase noise of -137 dBc/Hz at 1 MHz offset from the 2.2 GHz carrier at a supply voltage of only 0.5 V.

Keywords: LC-VCO, Ultra-Low-Power, Low Phase Noise.

1. INTRODUCTION

The CMOS process is renowned for the capability of high integration and cost effectiveness in mass production. When the CMOS technology has evolved into the deep submicron scale such as 45nm, the device current-gain cut-off frequency (f_T) has exceeded 200 GHz. The fabrication cost, however, drastically increases. In microwave analog circuits design, high dynamic range with low DC power consumption and low cost is essential. Thus, 130nm CMOS technology is a good candidate, because it has (1) f_T over 60 GHz, (2) a breakdown voltage of 1.5 V, (3) lower cost than 45-90 nm CMOS technologies.

The operation voltage target is only 0.5 V, which is the output voltage of solar cells. With the RF transceiver ICs able to operate under 0.5 V voltage supply, handsets could be powered by solar cells.

Previously, several VCOs are reported to improve their performance such as low phase noise [1], linear Kvco [2] and ultra-wide band operation [3]. In this paper, an ultra-low operation voltage and low phase noise LC-VCO IC design is presented in 130nm CMOS technology

Manuscript received on January 2, 2014 ; revised on February 2, 2014.

*The authors are with The Graduate School of Information, Production and Systems, Waseda University , Japan, E-mail: yoshimasu@waseda.jp[1]

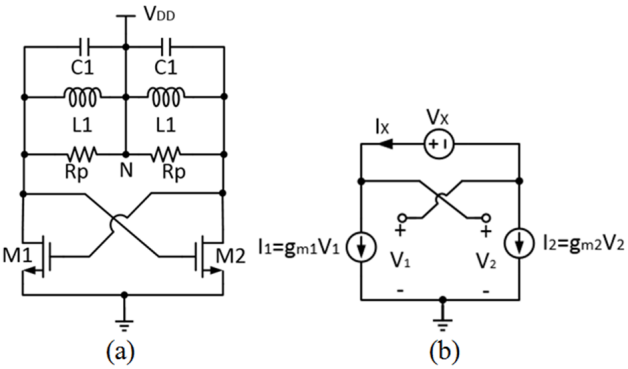

Fig. 1: *(a) Conventional Cross-coupled LC Oscillator, (b) Small Signal Model of Cross-coupled Pair.*

2. DEVICE MODELING AND IMPROVEMENT

2.1 Theory Analysis

Low-voltage VCO design is challenging for many reasons. Besides the transistor's low voltage operation, one of the major difficulties is the resonator design. Fig. 1(a) shows the conventional structure of the LC oscillator. It's noted that, for small differential ac signal, V_N does not change even if it is not connected to V_{DD}. So this oscillator structure can be seen as a lossy resonator ($2L_1$, $C_1/2$, and $2R_p$) tied to the port of an active circuit (M1 and M2), where R_p represents the equivalent parasitic resistance of the inductor and capacitor [4].

It can be seen from the small signal model of the cross-coupled pair as shown in Fig. 1(b), for $g_{m1} = g_{m2} = g_m$, that:

$$\frac{V_X}{I_X} = -\frac{1}{g_{m1}} - \frac{1}{g_{m2}} = -\frac{2}{g_m} \tag{1}$$

For oscillation to occur, the negative resistance must cancel the loss of the tank:

$$-\frac{2}{g_m} + R_p \leq 0 \tag{2}$$

As shown in Fig. 2, NMOS's transconductance (gm) performance is simulated with Vgs and Vds swept from 0 V to 1.5 V. And transistor size is chosen to 10 μm finger width with 12 fingers and 130 nm

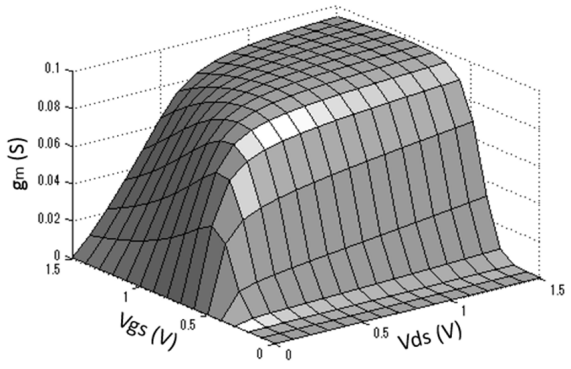

Fig.2: *NMOS Transistor's Transconductance.*

gate length. When Vgs=1 V and Vds=1.5 V, transistor's transconductance reaches the maximum value (g_m=96 mS). However, with Vgs=Vds=0.5 V operation, gm is decreased to 55 mS, which is only 57.3% of the maximum value. It can be seen that transistor's transconductance is not large enough in the low voltage operation.

Hence, to satisfy the oscillation startup condition, decreasing the parasitic resistance of the LC resonant circuit (improving Q-factor of inductor and capacitor) is very important for the ultra-low-voltage LC-VCO design.

2.2 Inductor Improvement

Y-parameter matrix is common for the two-port network parameter description, where Y_11 represents the admittance seen looking into port 1 when port 2 is shorted. So Q-factor of the inductor (two-port network) can be defined by [5]:

$$Q = \frac{Im(1/Y_{11})}{Re(1/Y_{11})} \tag{3}$$

To improve the LC resonant circuit performance, a single symmetric inductor is employed rather than two asymmetric spiral inductors. In addition to saving area, a differential geometry (driven by differential signals) also exhibits a higher Q and a broader range of operating frequency [6].

Fig. 4 shows the layout of two asymmetric spiral inductors structure. The size of each inductor is chosen to 2.5 turns with 15 μm wide top metal, and inner radius is 56 μm. Total size is 680 μm by 380 μm.

Fig. 5 shows the layout of single symmetric inductor structure. The size is chosen to 3 turns with 15 μm wide top metal, and inner radius is 90 μm. Total size is 440 μm by 420 μm.

A comparison of the simulated inductive part of input impedance and Q-factor between a single symmetric inductor and two asymmetric inductors are shown in Fig. 6 and 7. At typical 2.4 GHz operational frequency, with nearly the same inductive part of input impedance (3.2 nH), two asymmetric inductors exhibit a simulated Q-factor of 9.6, while the single symmetric inductor exhibits a simulated Q-factor of 15.4, which is 60% higher.

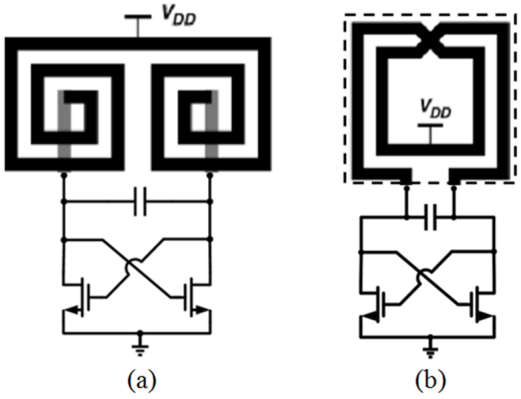

Fig.3: *(a) Oscillator with Two Asymmetric Inductors, (b) Oscillator with Single Symmetric Inductor.*

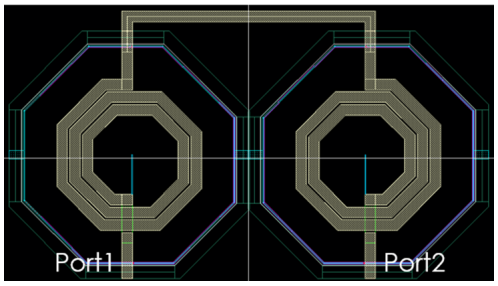

Fig.4: *Layout of Two Asymmetric Inductors.*

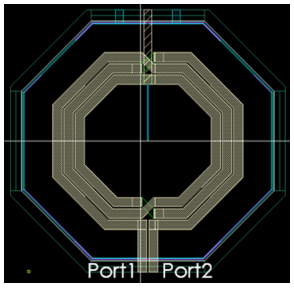

Fig.5: *Layout of Single Symmetric Inductor.*

Table 1 shows the characteristic comparison of two asymmetric spiral inductors and a single symmetric inductor. It can be clearly seen that the single symmetric inductor structure is effective to save the area and improve the Q-factor (decrease the parasitic resistance).

2.3 AMOS Varactor Improvement

A varactor is a voltage-dependent capacitor. Two critical attributes of varactor are concentrated: (1) the capacitance range, especially the ratio of the maximum and minimum capacitances that the varactor can provide, (2) the Q factor of the varactor.

A large varactor with high C_{max}/C_{min} ratio can

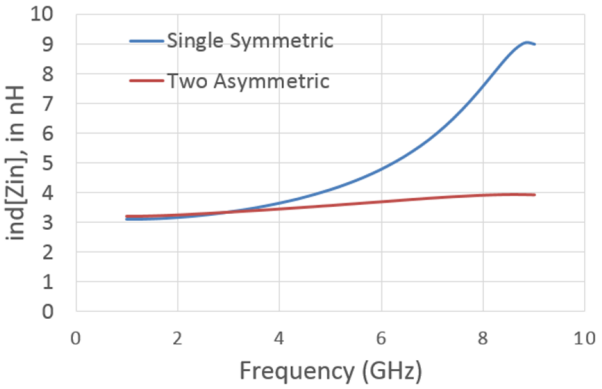

Fig.6: *Simulated Inductive Parts of the Input Impedance of Single Symmetric and Two Asymmetric Inductors.*

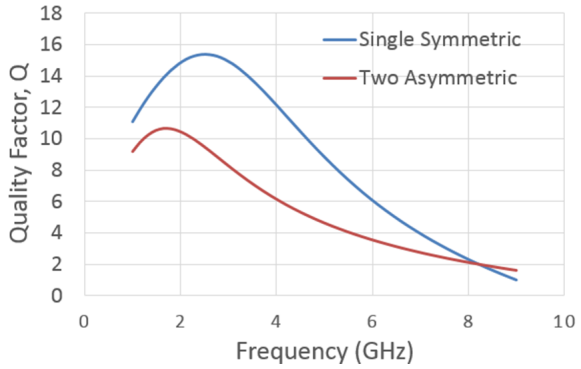

Fig.7: *Simulated Q-factors of Two Asymmetric Inductors and a Single Symmetric.*

Table 1: *Characteristic Comparison.*

Characteristic	Two Asymmetric	Single Symmetric	Improve
Area	680μm by 380μm	440μm by 420μm	-28%
L(nH) @2.4 GHz	3.24	3.29	1%
Q @2.4 GHz	9.6	15.4	60%

exhibit a wider frequency tuning range [7], because:

$$Tuning = \frac{C_{v,max} + C_{fix}}{C_{v,min} + C_{fix}} \quad (4)$$

Where C_V is the varactor capacitance and C_{fix} is the fixed parasitic capacitance.

To startup oscillation at 2.2 GHz with 3.2 nH inductor, the AMOS varactor size is optimized to 2 μm width and 1.6 μm length per finger, 60 fingers per group and 2 groups. The simulated C-V and Q-V characteristics at 2.4 GHz operational frequency is shown in Fig. 8. The varactor has a C_{max}/C_{min} about 4.5 over a tuning voltage of $\pm$1 V.

For resonant circuit design, capacitor ac coupling topology shown in Fig. 9 is used to allow positive and negetive voltages across the varactors. This topology

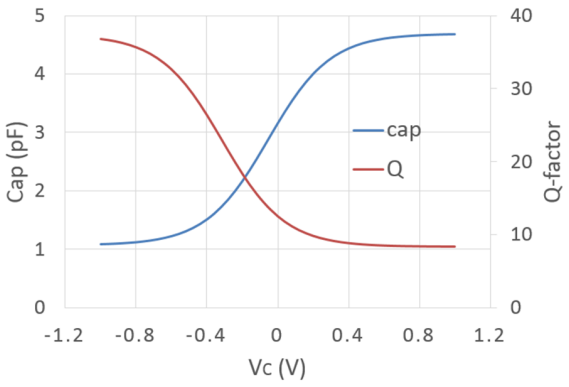

Fig.8: *Simulated C-V and Q-V Characteristics of AMOS varactor at 2.4 GHz.*

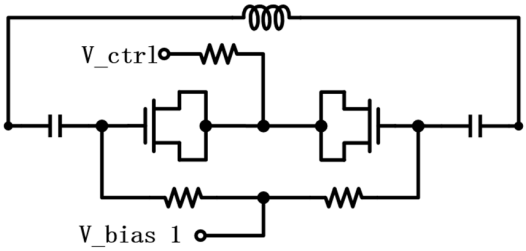

Fig.9: *AMOS Varactor Ac-coupling Structure.*

can increase the frequency tuning range and cover greater process variation. But the size of coupling capacitors must be large enough otherwise this fixed capacitance in series with the varactor will reduce tuning range of the varactor [8].

Obviously, DC gate to source bias voltage across the AMOS varactor is:

$$Vgs = V\_bias1 - V\_ctrl \quad (5)$$

Since the VCO design is for 0.5 V voltage supply system, V_ctrl has a changing range from 0 to 0.5 V. As shown in Fig. 10, if V_bias1 is set to 0 V, Vgs changing range is -0.5-0 V; Varactor capacitance changes not so linearly form 1.3 to 3.1 pF, but Q-factor is high (12.5-30). If V_bias1 is set to Vdd/2 (0.25 V), Vgs changing range is -0.25-0.25 V; Varactor capacitance changes linearly from 2 to 4.1 pF, but Q-factor is lower (9.6-20). It means that there is a trade-off between the capacitance changing range, linearity and Q-factor.

It is noted that while lager capacitance results in a better theoretical frequency tuning range, the actual tuning range can be degraded due to the Q-factor limitation [5].

Fig.11 shows the simulated frequency tuning range with different V_bias1 value in the actual cross-coupled VCO design. The VCO has a tuning range of 17.9% (2.3-2.74 GHz) with V_bias1=0.25 V, and 18.7% (2.47-3 GHz) with V_bias1=0.5 V. Because of

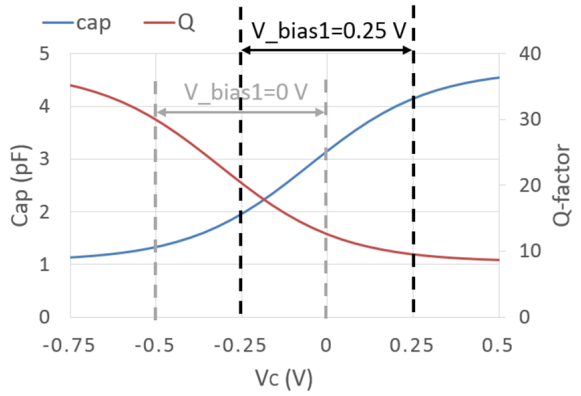

Fig.10: *Capacitance and Q-factor changing range of AMOS varactor with different V_bias1.*

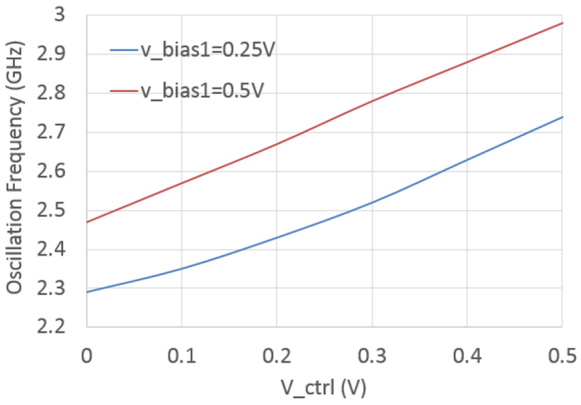

Fig.11: *Simulated Oscillation Frequency versus Tuning Voltage with 0.25V and 0.5V Varactor Bias.*

the system design target, V_bias1 is set to 0.25 V in the VCO IC design.

Considering the cross section of AMOS varactor shown in Fig. 12 [9], the equivalent circuit with physically meaningful lumped elements is proposed in Fig. 13(a), which can be simplified to the model shown in Fig. 13(b). And the substrate-related components R_{well}, R_{sub}, C_{sub1} and C_{sub2} can be simplified to:

$$\begin{aligned} Z_c =& R_{well} + \frac{1}{j\omega C_{sub1}} + R_{sub} || \frac{1}{j\omega C_{sub2}} \\ =& R_{well} + \frac{R_{sub}}{1 + (\omega R_{sub} C_{sub2}^2)} \\ & - j[\frac{1}{\omega C_{sub1}} + \frac{\omega C_{sub2} R_{sub}^2}{1 + (\omega R_{sub} C_{sub2})^2}] \end{aligned} \quad (6)$$

Based on the simpilified AMOS model shown in Fig. 13(b), common source connection and common gate connection of the two AMOS varactors shown in Fig. 14(a) and 14(b) are discussed and compared.

For the two AMOS varactors common gate connection shown in Fig. 14(a), the parasitic impedance Zc will increase varactors capacitance and decrease varactors Q-factor. So the frequency tuning range of

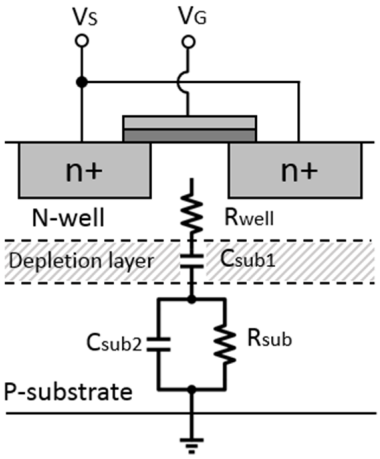

Fig.12: *Cross Section of AMOS Varctor.*

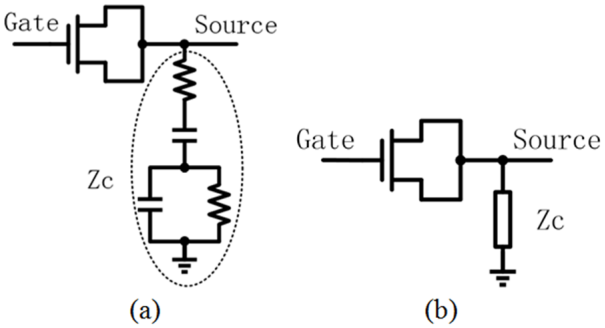

Fig.13: *(a): Equivalent Circuit of AMOS Varactor,(b) Simplified Model of AMOS Varactor.*

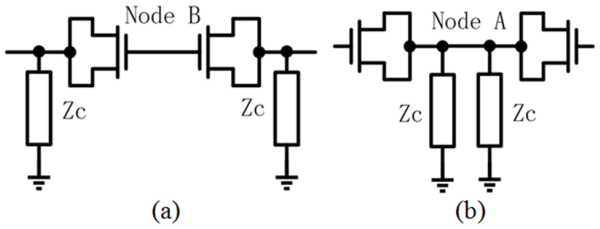

Fig.14: *Equivalent Circuit of Varactors (a) Common Gate Connection, (b) Common Source Connection.*

VCO design will be decreased by Zc.

However, for the common source connection shown in Fig. 14(b), node A (common source point) serves as the virtual ground. So Zc is short to ground and the AMOS varactor substrate parasitic effect will not influence VCO's performance. Fig. 15 shows the simulated frequency tuning range with different AMOS varactors connection method. For common gate connection, frequency tuning range is 17.3% (2.27-2.70 GHz). And for common source connection, frequency tuning range is 17.5% (2.29-2.73 GHz). It can be seen that the common source connection exhibits a better performance.

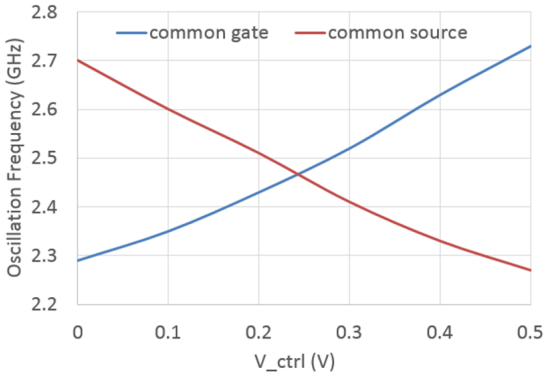

Fig.15: *Simulated Oscillation Frequency Performance.*

As a conclusion, ac coupling and common source connection topology can effectively improve AMOS varactors capacitance tuning range and Q-factor, which is useful for the LC resonant circuit design, especially for the low voltage LC-VCO design.

2.4 Circuit Design

Based on the Inductor and AMOS varactors improvement, the schematic of LC cross-coupled VCO circuit is proposed as shown in Fig. 16. The operation voltage (Vcc) is 0.5 V.

The standard 130-nm CMOS process offers an NMOS device with 400 mV threshold voltage, which exhibits fT of 66 GHz and f_{MAX} of 53 GHz with Vgs=Vds=0.5 V DC bias voltage. The size of cross-coupled NMOS transistor is optimized to 10 μm finger width with 12 fingers (120 μm total gate width) and 130 nm gate length for the negative resistance generation.

A transistor gate bias circuit is inserted with resistors. V_bias2 can change DC gate to source bias voltage to make the cross-coupled NMOS transistor operate mostly in saturation region during on-state, minimizing load Q-factor degradation [10].

The LC resonant circuit consists of (1) a single symmetric inductor that is simulated to be 3.2 nH with Q-factor of 15.4 at 2.4 GHz operational frequency, (2) AMOS varactors which have a capacitance tuning range from 2 to 4.1 pF over a tuning voltage of ±0.25 V, with capacitor ac coupling and common source connection structure. V_bias1 is set to 0.25 V (Vcc/2), and V_ctrl is changed from 0 V to 0.5 V to control the oscillation frequency tuning.

A source follower amplifier is connected at the output ports as the buffer amplifier to drive the power meter with 50 Ω input impedance.

Fig.17 shows the simulated performance of VCO's oscillation frequency tuning. The frequency tuning range is 17.5% (2.3-2.74 GHz).

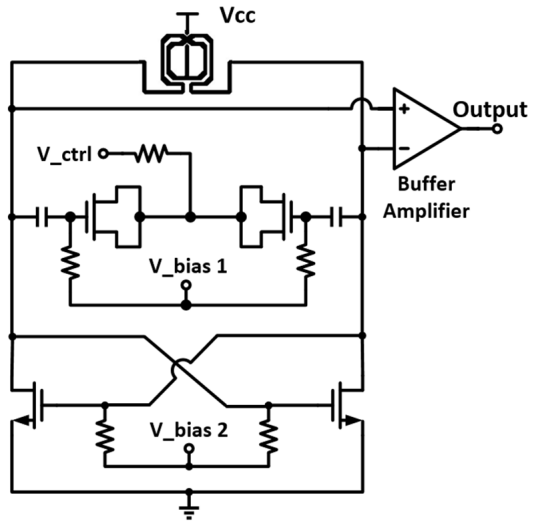

Fig.16: *Schematic of the LC-VCO Core Circuit.*

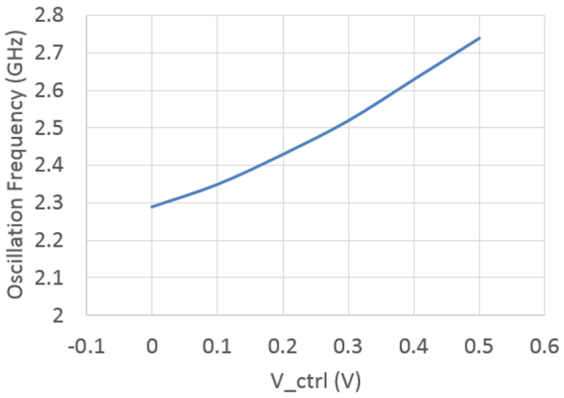

Fig.17: *Simulated Performance of Oscillation Frequency.*

3. FABRICATION AND MEASUREMENT

Fig. 18 illustrates a photograph of the fabricated VCO IC. The chip size is 0.70 mm by 0.75 mm, while the VCO core size (without pad) is only 0.45 mm by 0.7 mm. The VCO IC measurements are carried out with on-wafer probes. The dependence of the measured frequency tuning range (solid line) and the output power (dotted line) on the control voltage (V_ctrl) is depicted in Fig. 19. The supply voltage (Vcc) is 0.5 V and the DC current consumption of the VCO core circuit is 5.89 mA. The VCO IC exhibits a frequency tuning range from 2.17 to 2.59 GHz and an output power of around 1.0 dBm. The tuning range of 17.4 % is achieved by control voltage of only 0.5 V. The measured Kvco is from 740 to 900 MHz/V. Thus, Kvco ratio is 1.216 which is extremely linear comparing with previous linear VCO [2].

Fig. 20 shows measured phase noise of the VCO IC at an operation voltage of 0.5 V. The VCO IC exhibits a phase noise of -137 dBc/Hz at 1 MHz offset from the 2.2 GHz carrier. The well-known figure of merit

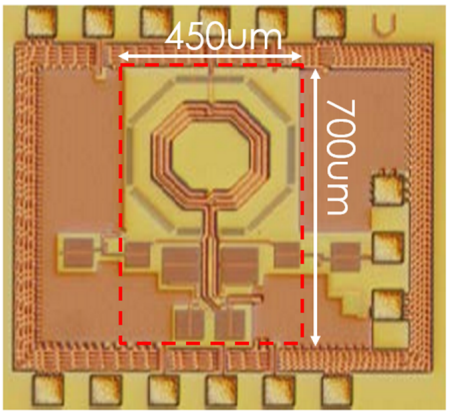

Fig.18: *Photograph of the fabricated LC-VCO IC.*

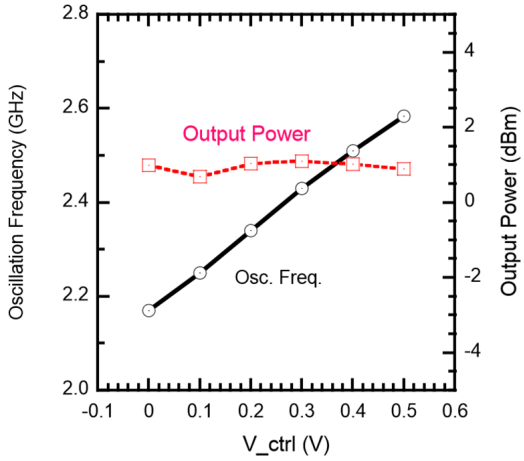

Fig.19: *Measured performance of oscillation frequency (solid line) and output power (dotted line).*

(FoM), which is defined by phase noise, oscillation frequency, offset frequency and DC power dissipation (ex. [11]), is

$$\begin{aligned} \mathrm{FOM} &= Phase\ Noise - 20\log\frac{\omega_0}{\triangle\omega} + 10\log\frac{P}{1mW} \\ &\approx -196dBc/Hz \end{aligned} \quad (7)$$

Table 2 summarizes the performance of the VCO IC with recently reported VCO ICs. The VCO IC presented in this paper has exhibited excellent FoM with ultra-low voltage.

4. CONCLUSION

This paper introduces the LC resonant circuit improving method for the VCO design, which consists of 1) a single symmetric inductor instead of two asymmetric inductors; 2) AMOS varactors using ac coupling and common source connection topology. And a 2.4 GHz band low voltage and low phase noise LC-VCO IC has been demonstrated in 130 nm CMOS technology. The VCO IC exhibits measured frequency tuning range of 17.4% and phase noise of -137dBc/Hz at 1 MHz offset from the 2.2 GHz carrier at an operation voltage of only 0.5 V.

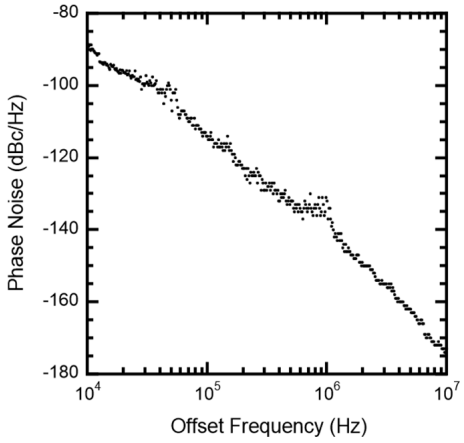

Fig.20: *Measured phase noise of the LC-VCO IC.*

Table 2: *Performance Summary and Comparison.*

	This Work	[12]	[13]
Technology	130 nm CMOS	65 nm CMOS	65 nm CMOS
Supply voltage	0.5 V	1.8 V	1.2 V
Frequency	2.17-2.59 GHz	2.62-3.3 GHz	4.1-6.5 GHz
FoM	-196.1 dBc/Hz	-183 dBc/Hz	-186.6 dBc/Hz

ACKNOWLEDGEMENT

This work is supported by Japan Society for the Promotion of Science (JSPS) KAKENHI Grant-in-Aid for Scientific Research (B) Number 23360162.

This work is supported by VLSI Design and Education Center(VDEC), the University of Tokyo in collaboration with Cadence Design Systems Inc, Mentor Graphics Inc, and Agilent Technologies Japan Ltd.

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Xin Yang (S'11) was born in Guangzhou, China, in 1989. Participating the 3+2 joint training project, he received the B.S. degree from Southeast University, Nanjing, China, and M.S. degree of Waseda University, Kitakyushu, Japan, in 2013, respectively. Currently, he is working towards Ph.D. degree at the Graduate School of Information, Production and Systems, Waseda University, Kitakyushu, Japan. His research interests include the microwave and millimeter-wave integrated circuits. Mr. Yang received the Best Student Paper Award of IMWS2012, and CSC scholarship from Chinese government from 2013 to 2016.

Kangyang Xu was born in Nanjing, China, in 1991. He received the B.S. degree from Southeast University, Nanjing, China. Currently, he is participating the 3+2 joint training project of M.S. degree with the Graduate School of Information, Production and Systems, Waseda University, Kitakyushu, Japan. His research interests include the microwave and millimeter-wave integrated circuits.

Wei Wang received the B.S degrees from the University of Electronic Science and Technology of China(UESTC), Chengdu, China, in 2012. Now he is a master student at Graduate school of Information, Production and system of Waseda, Kitakyushu, Japan. His research interests include the RF/millimeter-wave Integrated Circuit, 80GHz CMOS power amplifier for wireless system.

Toshihiko Yoshimasu (M'92) received the B.S. and Ph.D. degrees in Electrical Engineering from Kobe University, Kobe, in 1981 and 1999, respectively. In 1981, he joined Central Research Laboratories of Sharp Corporation, Tenri, Japan. From 1981 to 1984, he was engaged in research and development on high-power Si MOSFETs. From 1985 to 1999, he was engaged in research and development on GaAs-based microwave devices and associated monolithic circuits, including low-noise amplifiers, power amplifiers, switches, filters, oscillators and frequency converters. From 2000 to 2003, he was involved in the research and development of Si CMOS RF ICs for wireless communications. Since April 2003, he has been a Professor of the Graduate School of Information, Production and Systems, Waseda University, Kitakyushu-shi, Japan. His major interests include microwave and millimeter-wave ICs with Si CMOS, SiGe BiCMOS, GaAs-based HBT, and pHEMT technologies. Dr. Yoshimasu is a senior member of the Institute of Electronics, Information and Communication Engineers (IEICE), and a member of the Institute of Electrical and Electronics Engineers (IEEE).