The Simplified Control of Three-Phase Four-Leg Shunt Active Power Filter for Harmonics Mitigation, Load Balancing and Reactive Power Compensation

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ABSTRACT

In this paper, the simplified control of three-phase four-leg shunt active power filter for harmonics mitigation, load balancing and reactive power compensation is proposed. In order to calculate the harmonics, current imbalance and reactive power, the load currents are detected and transformed to $dq0$ variables. By using the low-pass filter, the fundamental active power current can be separated from the d-axis current. Therefore, the commanded active power filter currents are consist of d-axis harmonic currents, q-axis and 0-axis currents. These components are regulated by the PI controller with feedforward utility voltage via the four-leg space vector inverter. Moreover, the design guidelines of space vector phase-locked loop (PLL), current controllers and DC-bus voltage controller are also presented. Validity of the proposed control schemes is confirmed by the simulation.

Keywords: four-leg active power filter; load balancing; reactive power compensation.

1. INTRODUCTION

With the increasing use of nonlinear equipments in power system, power quality is becoming a critical issue these years. That nonlinear equipment has caused some serious problems in power quality such as low power factor and significant harmonics. The active power filter (APF) is an effective solution to alleviate such problems [1]-[6].

In many commercial and industrial installations, power is distributed through a three-phase four-wire system. This type of system has unique problems. If nonlinear single-phase and/or three-phase loads are present, or the three-phase load is unbalanced, line currents are unbalanced and neutral currents flow. These neutral currents contain both fundamental and harmonic components. In extreme cases, the neutral currents are potentially damaging to both the connected neutral conductor and the transformer. The three-phase three-wire active power filters cannot adequately reduce or eliminate line harmonics in this situation. To mitigate these problems, three-phase four-wire active power filters have been proposed [7]-[8].

Three-phase voltage-source converters normally have two ways of providing a neutral connection for three-phase four-wire systems :

1. using split dc link capacitors and tying the neutral point to the mid-point of the dc link capacitors;
2. using a four-leg converter topology and tying the neutral point to the mid-point of the fourth neutral leg.

With the split-capacitor approach the three-phase converter essentially becomes three single-phase half-bridge converters; thus, it suffers from an insufficient utilization of the dc link voltage. In addition, large and expensive dc link capacitors are needed to maintain an acceptable voltage ripple level across the dc link capacitors in case of a large neutral current due to unbalanced and/or nonlinear load . There is a growing interest in four-leg converters for three-phase four-wire applications. Therefore, the four-wire active power filter with a four-leg inverter topology is used in this paper.

For the space vector PWM of the four-leg inverter, by considering all four pole voltages including that the neutral phase simultaneously in the determination of zero-sequence voltage, a new and natural standpoint for the carrier-based PWM have been proposed in [9]. This new viewpoint renders the full consistency between the PWM methods for the three- and four-leg inverters, is very simple in the implementation. Therefore, the new algorithm is used in this paper.

This paper presents the power quality improvement by using the active power filter . The function of the APF is to detect and compensate harmonics, current imbalance, and reactive power caused by loads. The $dq0$ variables of load currents are used for calculating the commanded APF currents. To reduce the PI gain of current controllers, the feedforward utility voltages are added in the commanded APF voltages. The new carrier-based PWM of the four-leg inverter [9] is used for generating the gate signal of the IGBTs.

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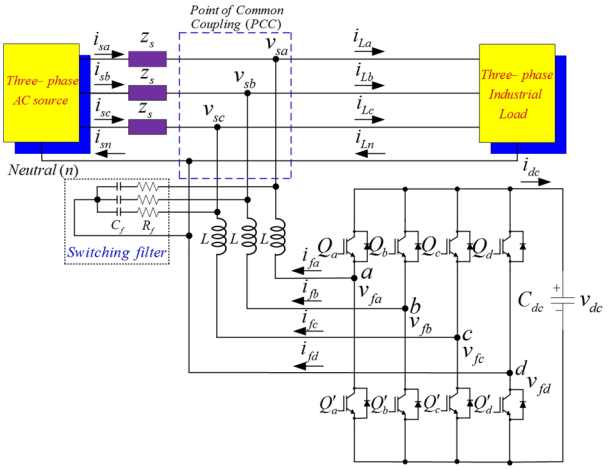

Fig.1: *Circuit configuration of the three-phase four-leg shunt active power filters.*

In order to receive the utility voltage information, such as amplitude and/or frequency, the space vector phase-locked loop is also introduced. Moreover, design guidelines of PLL, current controllers and DC-bus voltage controller are presented. Furthermore, an analysis, design-concept and simulation are detailed. Finally simulatation results, by the PSIM software, verify feasibility of the proposed control schemes.

2. THREE-PHASE FOUR-LEG ACTIVE POWER FILTER

The active power filter, shown in Fig. 1, is a three-phase four-wire voltage source PWM inverter. It is shunt-connected through three inductors to a three-phase unbalance industrial load with connected neutral, which produces current type harmonics and requires reactive power and zero-sequence load current. The three principal legs that are connected to each phase are controlled mainly for harmonics and reactive power compensation. The aim of the fourth added leg is to cancel the zero-sequence current in the utility. Under these considerations, the mains currents would become practically sinusoidal and in phase with the corresponding phase voltages.

2.1 Harmonics, current imbalance and reactive power calculation

In order to calculate the harmonics, current imbalance and reactive power, the load currents are detected and transformed to $\alpha\beta 0$ variables as shown in Fig. 2 and (1). Equation (2) is the currents transformation between stationary reference frame and synchronous reference frame. The $\hat{\theta}$ is the estimated value of utility voltage angle from the PLL.

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3/2} & -\sqrt{3/2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (1)$$

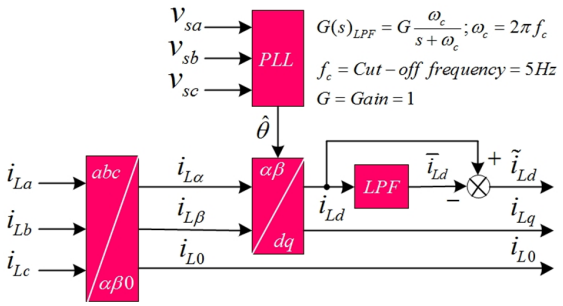

Fig.2: *Block diagram of currents calculation.*

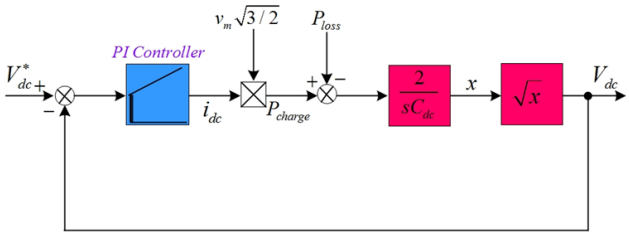

Fig.3: *The DC-bus voltage control loop.*

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \quad (2)$$

The active power current is the average value of d-axis current ($\bar{i}_{Ld}$) that can be separated from the d-axis current by using the low-pass filter (LPF). The i_{Lq} denotes harmonics and reactive power. The i_{L0} denotes harmonics and current imbalance. Therefore, the commanded APF currents are consist of d-axis harmonic currents ($\tilde{i}_{Ld}$), q-axis currents and 0-axis currents.

2.2 Design of DC-Bus voltage controller

The DC-bus voltage is expected to be constant in steady state, then a proportional integral (PI) can be used as the DC-bus voltage controller. The design guidelines of these controller are discussed in this subsection. The energy equation as shown in (3).

$$\begin{aligned} p_{charge} - p_{loss} = V_{dc}(t) i_{dc}(t) &= V_{dc}(t) C_{dc} \frac{dV_{dc}(t)}{dt} \\ &= \frac{1}{2} C_{dc} \frac{dV_{dc}^2(t)}{dt} \end{aligned} \quad (3)$$

Where $p_{charge}\left(= v_m\sqrt{3/2} i_{dc}\right)$ is the active power charge to inverter, v_m is the peak of phase voltage and p_{loss} is the inverter losses. The DC-bus voltage control loop is shown in Fig. 3.

For the linearization around operating point, the square-root function can be approximated by the first order Taylor series expansion as shown in (4).

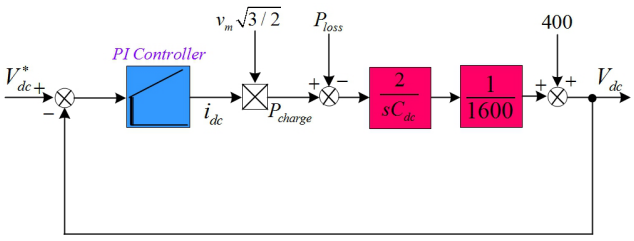

Fig.4: *The small-signal DC-bus voltage control loop.*

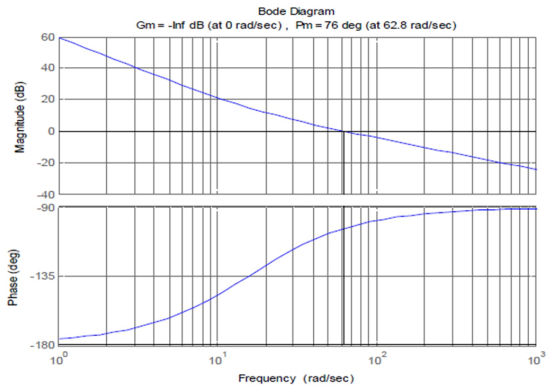

Fig.5: *Phase margin of the dc-bus control as designed.*

$$y(x) = \sqrt{x} = \sqrt{x_0 + \Delta x} \approx \sqrt{x_0} + \frac{d\sqrt{x}}{dt}\Big|_{x=x_0} \Delta x \approx \sqrt{x_0} + \frac{1}{2\sqrt{x_0}}(x - x_0) \quad (4)$$

At the operating point ($V_{dc} = V_{dc}^* = 800V$), the $x_0 = 800^2$ and substituting in (4), the approximated square-root function as shown in (5). Fig. 4 shows the small-signal of DC-bus voltage control loop [10].

$$y(x) \approx \sqrt{800^2} + \frac{1}{2\sqrt{800^2}}(x - 800^2) \approx 400 + \frac{x}{1600} \quad (5)$$

Where "*" denotes the commanded value.

Since the DC-bus voltage fluctuates in two times of fundamental frequency because of the power exchange between utility and APF. In this case, the cross-over frequency (ω_0) of the loop-transfer function should be reduced the twice fundamental frequency. At the ω_0 , the loop- transfer function could be expressed in (6).

$$|G(s)H(s)|_{s=j\omega_0} = \left|\left(k_p + \frac{k_i}{s}\right)\left(\frac{v_m\sqrt{3/2}}{s}\right)\left(\frac{2}{1600 * C_{dc}}\right)\right|_{s=j\omega_0} = 1 \quad (6)$$

For the adequate phase margin, the corner frequency ($\omega_{cn} = k_i/k_p$) of PI controller should be less than ω_0 .In this paper, ω_0 is selected equal to 10% of the twice frequency and ω_{cn} is selected equal to 25% of ω_0 . From these design,$\omega_0 = 62.8rad/s$ and$\omega_{cn} = 15.7rad/s$, the k_p and k_i are 0.51 and 8.06, respectively. Fig. 5 shows the phase margin (= 76°) at $\omega_0 = 62.8rad/s$ of the control as designed.

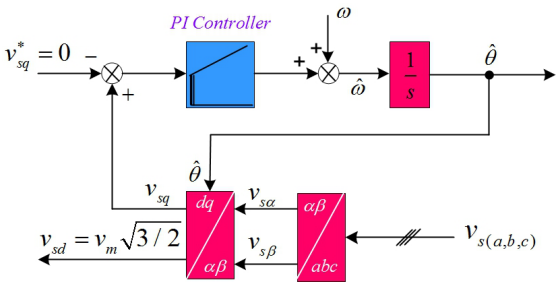

Fig.6: *The block diagram of space vector PLL.*

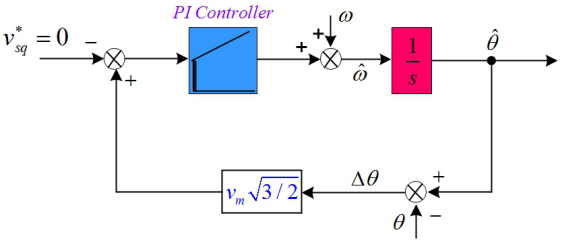

Fig.7: *The small-signal block diagram of space vector PLL.*

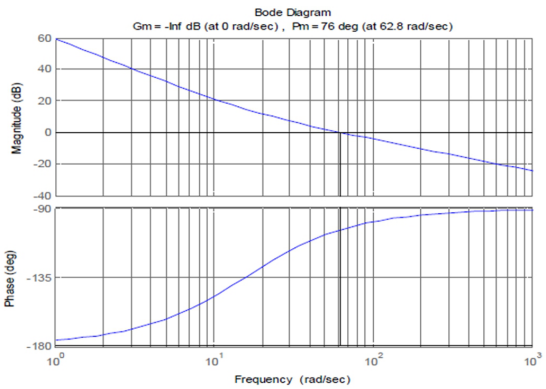

Fig.8: *Phase margin of the PLL control as designed.*

2.3 Design of Space vector PLL

In order to receive the utility voltage information, such as amplitude and/or frequency, the space vector phase-locked loop is introduced in this subsection. The phase voltages of the utility are detected and transformed to space vector quantity. On the synchronous reference frame, the v_{sq} equal to zero when the synchronous reference frame is synchronized with the utility voltage. Therefore, thev_{sq} is regulated to zero by the PI controller. Fig. 6 shows the block diagram of space vector PLL. In order to design the PI controller, the small-signal of the v_{sq} is analyzed. Whenv_{sq} is controlled by the PLL, a relation of v_{sq} is shown in (7).

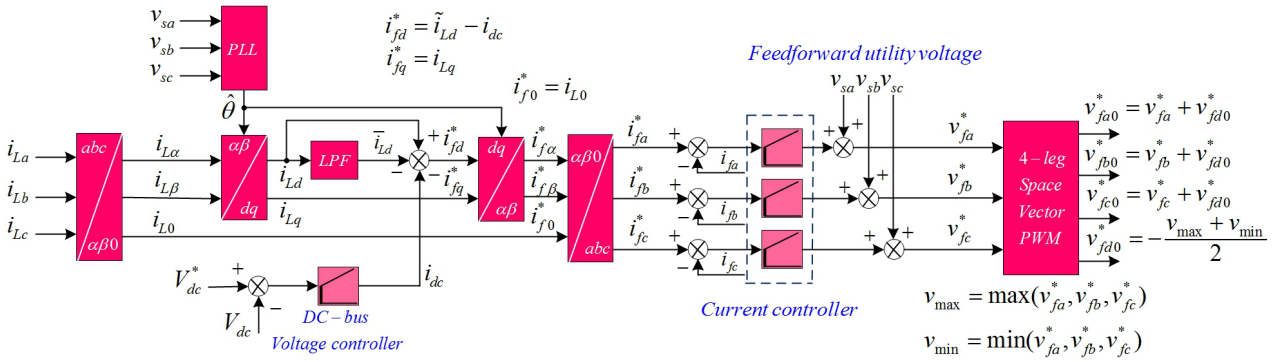

Fig. 9: *The overall control block diagram of three-phase four-leg shunt active power filters.*

$$\begin{aligned} v_{sq} &= -v_{s\alpha}\sin\hat{\theta} + v_{s\beta}\cos\hat{\theta} \\ &= -\sqrt{3/2}v_m\sin(\hat{\theta}-\theta) = -\sqrt{3/2}v_m\sin(\Delta\theta) \end{aligned} \tag{7}$$

Around the equilibrium operating conditions, the $\Delta\theta$ is very small, therefore, the $sin(\Delta\theta)$ is about $\Delta\theta$. The small-signal block diagram of space vector PLL as shown in Fig. 7.

From Fig. 7, it should be noted that the loop-transfer function is similar to the DC-bus voltage control loop, therefore, the PI controller as designed in the same manner. To reduce the twice frequency of the utility voltage, from the axis- transform, The ω_0 is selected equal to 10% of the twice frequency and ω_0 is selected equal to 25% of ω_0. From these design, $\omega_0 = 62.8rad/s$ and $\omega_{cn} = 15.7rad/s$, the k_p and k_i are 0.16 and 2.51, respectively. Fig. 8 shows the phase margin ($= 76°$) at $\omega_0 = 62.8rad/s$ of the control as designed.

2.4 Design of Current Controller

To completely compensate the harmonics, current imbalance and reactive power, the overall control block diagram of three-phase four-leg shunt active power filters as shown in Fig. 9. The commanded APF currents on the $\alpha\beta0$ and abc frame as shown in (8) and (9), respectively.

$$\begin{bmatrix} i^*_{f\alpha} \\ i^*_{f\beta} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i^*_{fd} \\ i^*_{fq} \end{bmatrix} \tag{8}$$

$$\begin{bmatrix} i^*_{fa} \\ i^*_{fb} \\ i^*_{fc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & 1/\sqrt{2} \\ -1/2 & \sqrt{3/2} & 1/\sqrt{2} \\ -1/2 & -\sqrt{3/2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i^*_{f\alpha} \\ i^*_{f\beta} \\ i^*_{f0} \end{bmatrix} \tag{9}$$

From the Fig. 1, the APF currents equation is shown in (10).

$$\frac{di_{f(a,b,c)}}{dt} = \frac{v_{f(a,b,c)} - v_{s(a,b,c)}}{L} \tag{10}$$

In order to control the APF currents and reduce the PI gain of current controllers, the feedback and feed-forward control are introduced and the commanded

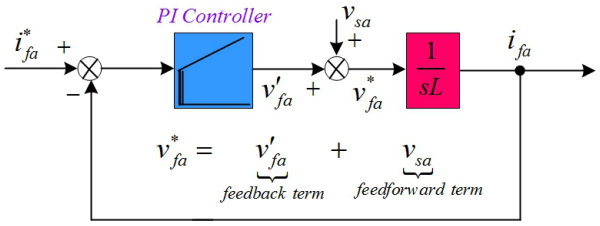

Fig. 10: *The a-phase current loop.*

APF voltage as shown in (11).

$$\begin{aligned} v^*_{fa} &= v'_{fa} + v_{sa},\ v^*_{fb} \\ &= v'_{fb} + v_{sb},\ v^*_{fc} = v'_{fc} + v_{sc}. \end{aligned} \tag{11}$$

Where v'_{fa}, v'_{fb} and v'_{fc} are the voltage from the current controllers a-phase, b-phase and c-phase, respectively. Fig. 10 shows the a-phase current loop.

To design the PI gains of the current controller, the high-gain of controller is required for the order of harmonics to be eliminated. In this paper, the cross-over frequency (ω_0) is selected equal to 62,800 rad/s and the corner frequency is selected equal to 1% of ω_0 . From these design,$\omega_0 = 62,800rad/s$ and $\omega_{cn} = 628rad/s$, the $k_p$and k_i are 62.8 and 39438, respectively. Fig. 11 shows the phase margin ($= 89.4°$) at $\omega_0 = 62,800rad/s$ of the control as designed.

2.5 Four-leg Space Vector PWM Inverters

For the space vector PWM of the four-leg inverter, by considering all four pole voltages including that the neutral phase simultaneously in the determination of zero-sequence voltage, a new and natural standpoint for the carrier-based PWM have been proposed in [9]. The commanded pole voltages are given by (12), and Fig. 12 is demonstrated of these waveforms.

$$\begin{aligned} v^*_{fa0} &= v^*_{fa} + v^*_{fd0},\ v^*_{fb0} = v^*_{fb} + v^*_{fd0} \\ v^*_{fc0} &= v^*_{fc} + v^*_{fd0},\ v^*_{fd0} = -\tfrac{v_{\max}+v_{\min}}{2} \end{aligned} \tag{12}$$

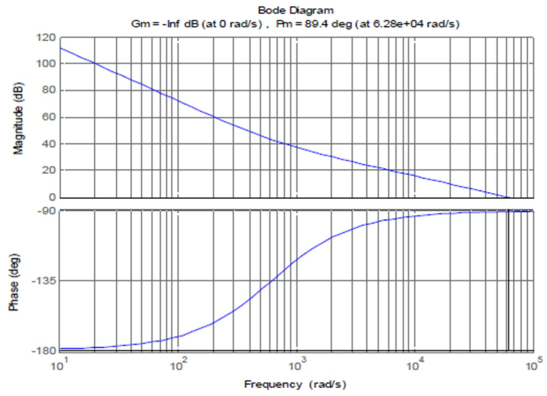

Fig.11: *Phase margin of the current control as designed.*

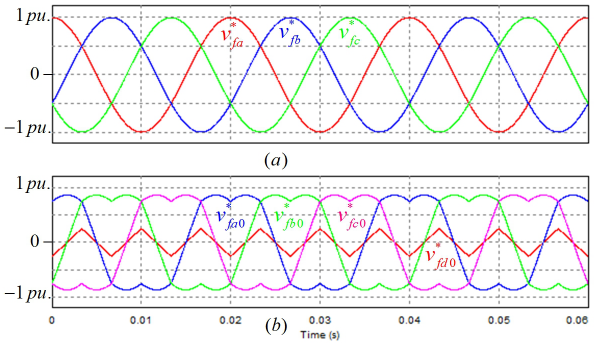

Fig.12: *Commanded phase voltages (a) and pole voltages (b).*

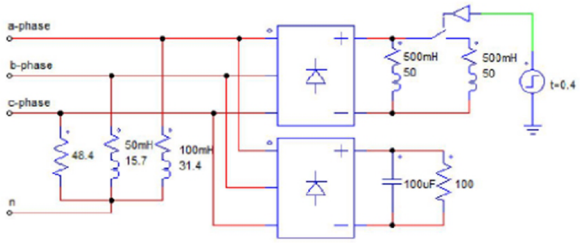

Fig.13: *The three-phase unbalance and harmonic loads.*

Where $v_{max} = max(v^*_{fa}, v^*_{fb}, v^*_{fc})$,
$v_{min} = min(v^*_{fa}, v^*_{fb}, v^*_{fc})$

3. SIMULATION RESULTS

To verify the feasibility of proposed control schemes, the simulation is presented in this section and the PSIM software is used for this simulation. The specifications and parameters of proposed APF as shown in the appendix. The three-phase heavily unbalance and harmonic loads as shown in Fig. 13 and the nonlinear step-load change is occurred at $t = 0.4$ second. The simulation results are shown in Fig. 14 - Fig. 19. From Fig. 14, the utility line currents are practically sine waves despite of the load currents are heavily unbalance and harmonic waveforms. Fig. 15 shows the neutral load currents, neutral utility current and DC-bus voltage. It should be noted that the DC-bus voltage has been regulated to the commanded value and the load balancing or neutral current has also been compensated under the nonlinear step-load change. Fig. 16 shows the effectiveness of reactive power compensation as proposed that the source power factor at the PCC has become practically unity. Fig. 17-19 show the harmonics spectrum of the utility and load currents. It should be noted that the total current harmonic distortion (THD_i) of a-phase, b-phase and c-phase utility currents are equally to 4.36%, 4.46% and 4.51%, respectively. Despite the a-phase, b-phase and c-phase load currents are equally to 35.41%, 31.20% and 34.25%, respectively. These results illustrate the effectiveness of harmonic compensation as proposed.

4. CONCLUSIONS

This paper presents the simplified three-phase four-leg shunt active power filter, The proposed APF may be used for current harmonic compensation, reactive power compensation, load balancing and neutral current compensation. Moreover, design guidelines of PLL, current controllers and DC-bus voltage controller are presented. Furthermore, an analysis, design-concept and simulation are detailed. Finally simulation results, by the PSIM software, verify feasibility of the proposed control schemes.

APPENDIX

Table 1: *SPECIFICATIONS AND PARAMETERS OF APF.*

Rated	3ϕ,380V,50Hz
Source impedance	R_s =0.5 Ω, L_s=0.5mH
Switching filter	R_f =120 Ω , C_f = 2.7 μF
Current filter	L=1mH
Switching frequency	20kHz
DC − bus capacitor	C_{dc}=4000μF
DC − bus voltage	V^*_{dc} = 800V
DC − bus voltage controller	$k_p = 0.51$, $k_i = 8.06$
PLL controller	$k_p = 0.16$, $k_i = 2.51$
Current controller	$k_p = 62.8$, $k_i = 39,428$

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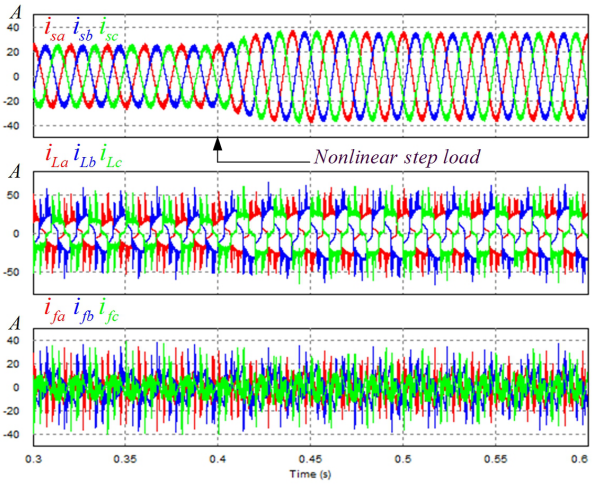

Fig.14: *The utility currents, load currents and APF currents.*

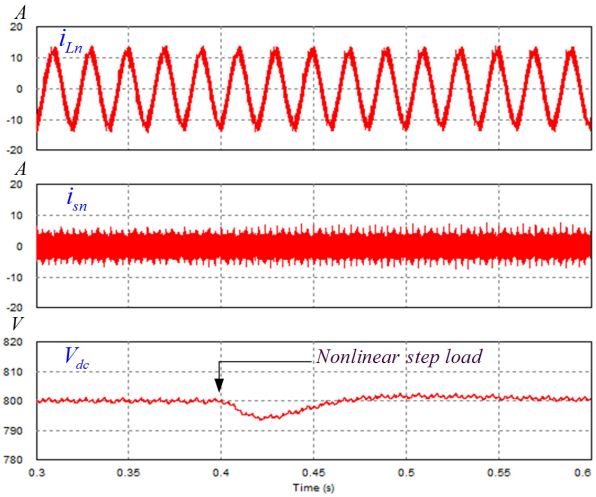

Fig.15: *The neutral load current, neutral utility current and DC-bus voltage.*

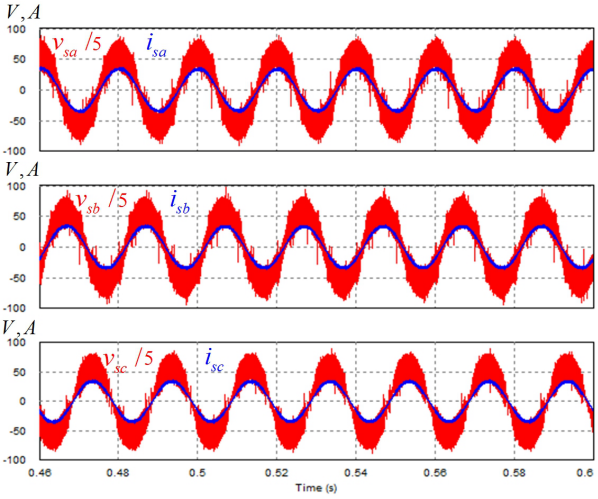

Fig.16: *The PCC voltages and currents.*

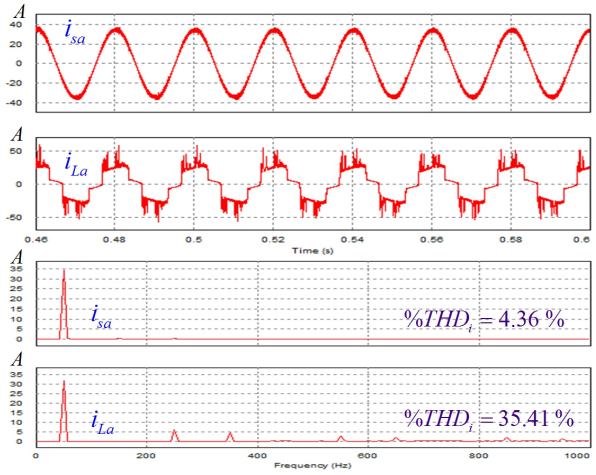

Fig.17: *The harmonics spectrum of a-phase utility current and load current.*

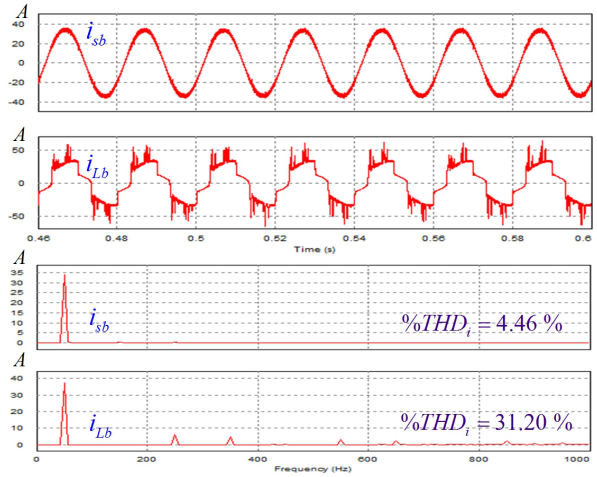

Fig.18: *The harmonics spectrum of b-phase utility current and load current.*

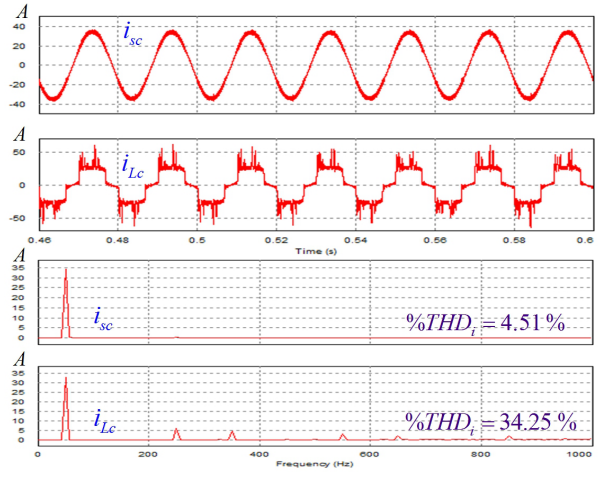

Fig.19: *The harmonics spectrum of c-phase utility current and load current.*

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