Impact of Strain on Fully Depleted Strained Gate Stack Double Gate MOSFET: A Simulation Study

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ABSTRACT

The fusion of strain engineering and multigate technology is implemented to design an advanced MOSFET model i.e. Fully Depleted Strained Gate Stack Double Gate (FD-S-GS-DG) in nanoscale regime. Both DC and Analog performances of FD-S-GS-DG are analyzed by varying the Ge mole fraction (X). The sensitivity of crucial device parameters like threshold voltage (V_{th}), subthreshold swing (SS), on-current (I_{on}), off state leakage current (I_{off}), on-off ratio (I_{on}/I_{off}), transconductance (g_m), output conductance (g_d), early voltage (V_{EA}), gain (A_V), transconductance generation factor (TGF) towards X are successfully evaluated and presented. From the obtained results by choosing appropriate value of X, we can significantly enhance the device performance.

Keywords: Gate stack (GS), Strain, Ge mole fraction (X), SCEs, Analog performance.

1. INTRODUCTION

The central component of semiconductor electronics is the integrated circuit (IC), which combines the basic elements of electronic circuits - such as transistors, diodes, capacitors, resistors and inductors on one semiconductor substrate. The two most important elements of silicon electronics are transistors and memory devices. For logic applications generally MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) are used [1]-[4].

The semiconductor industry has showcased a spectacular exponential growth in the number of transistors per integrated circuit for several decades, as predicted by Moore′s law [2]. The future technology trend predicted by ITRS (International Technology Roadmap for Semiconductors) [4], physical dimensions and electrostatic limitations faced by conventional process and fabrication technologies will require the dimensional scaling of complementary metal-oxide-semiconductor (CMOS) devices within the next decade [5], [6]. To enable future technology scaling, new device structures for next-generation technology have been proposed. Some of the new technologies are Silicon On Insulator (SOI) [7], Strained Silicon (S-Si) at the channel [8]-[10], inclusion of high-k dielectric materials in gate oxide [11]-[13] and Multi gate MOSFETs [14]-[16]. Many of these devices have been shown to have favorable device properties and new device characteristics, and require new fabrication techniques. These nanoscale devices have significant potential to revolutionize the fabrication and integration of electronic systems and scale beyond the perceived scaling limitations of traditional CMOS.

The salient objectives of this work is to design and simulate one optimum device i.e. Fully Depleted Strained Gate Stack DG (FD-S-GS-DG) MOSFET with optimized device parameters and analyze the sensitivity of important device performances including static and analog towards Ge mole fraction content (X) for both low power and high frequency applications.

2. DEVICE DESIGN AND SIMULATION

The schematic structure of FD-S-GS-DG MOSFET is shown in Fig. 1. In this structure the channel length (L) and Source/Drain length (L_S/L_D) is fixed as 40nm, the silicon thickness (t_{Si}) as 10nm and a uniform density of N_D as 10^{20} cm^{-3} is taken. The channel is doped with $(N_A) = 10^{16}$ cm^{-3}. Gate stack configuration is designed by considering SiO_2 layer thickness is fixed at 0.6nm and above this layer 0.5nm equivalent thickness of high-k layer, HfO_2 (k=24) is deposited, so that the EOT reaches 1.1nm. The work function of the gate material (Molybdenum) is considered at 4.6 eV. The Ge composition (X) in the layer SiGe is varied from 0 to 0.4 [17]-[19]. The strained silicon can be formed by following the steps: (i) epitaxial growth of SiGe layer on Si substrate (ii) ion implantation and high temperature annealing (iii) removal of surface layer and regrowth of Si/SiGe layer [20].

In the simulation, the inversion-layer Lombardi constant voltage and temperature (CVT) mobility model has been used. The Shockley-Read-Hall (SRH) generation and recombination parameters simulate the leakage currents. The model Fermi-Dirac uses a Rational Chebyshev approximation that gives results

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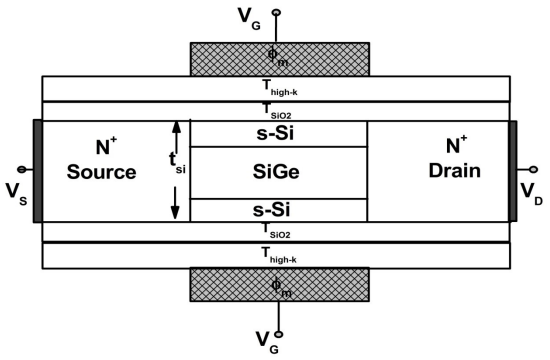


Fig. 1: *Schematic structure of FD-S-GS-Double Gate N-MOSFET.*

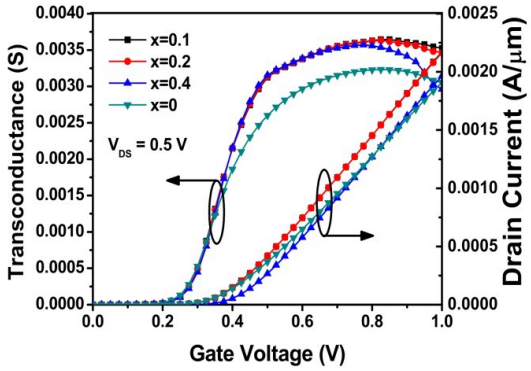
close to the exact values. The Auger recombination models for minority carrier recombination have been used [21].

3. RESULTS AND DISCUSSION

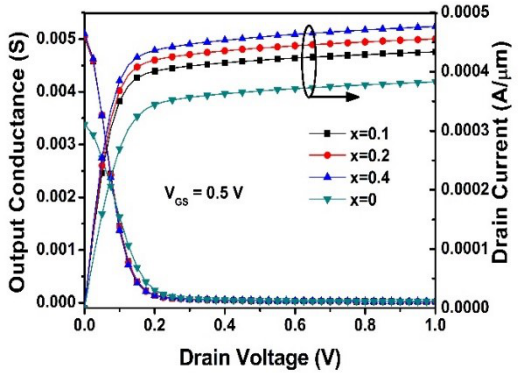
Fig. 2(a) shows the variation of drain current (I_D) and transconductance (g_m) with respect to gate voltage (V_{GS}) for various Ge concentrations (X). From the figure, as the Ge concentration is increased, drain current and transconductance is also increased because of the enhancement of carrier mobility caused by the strained silicon due to the lowering of in-plane effective mass and a reduction in intervalley scattering [22]. The output characteristic ($I_D - V_{DS}$) and output conductance (g_d) as a function of drain bias (V_{DS}) is plotted in Fig. 2(b). Here also, both the current and output conductance is more for strained silicon as compare to unstrained ($X = 0$) silicon due to the same mobility effect.

The simulated results for threshold voltage (V_{th}), subthreshold swing (SS), maximum value of on current (I_{on} (max)), off current (I_{off}), on-off ratio (I_{on}/I_{off}) are tabulated in Table 1. By comparing those values with Ge concentration (X) varying from 0 (unstrained) to 0.2 (strained), Ion is raised up to 13.4%, and I_{on}/I_{off} is improved by 1.75% with little compromise in I_{off}. The SS value increases as X value increases and reaches its maximum for X=0.4.

Fig. 3(a) shows the variation of the Early voltage (V_{EA}) with drain bias for various Ge mole fractions (X) at a gate voltage of 0.5 V. The V_{EA} is more for strained silicon as compare to unstrained silicon. It depicts highest value for X=0.1 and starts decreasing as x value increases. The intrinsic gain (A_V) of the device, which is a ratio of transconductance and output conductance for various Ge concentrations is plotted against gate voltage (V_{GS}) for V_{DS}=0.5 V is shown in Fig. 3(b). The intrinsic gain g_m/g_{ds} is a valuable figure of merit for operational transconductance amplifier. Similarly, from the figure, the gain is high for strained silicon from its counterpart unstrained silicon and reaches its maximum value for



(a)



(b)

Fig. 2: *(a) Drain current (I_D) and transconductance (g_m) variation with Gate voltage (V_{GS}) for different Ge concentration (X) (b) Drain current (I_{DS}) and output conductance (g_d) as a function of Drain voltage (V_{DS}) for different Ge concentration (X).*

X=0.1. It then starts decreasing as X value increases.

All the extracted values for analog performance are tabulated in Table 2. Similarly, as Ge concentration (X) varies from 0 (unstrained) to 0.2 (strained), transconductance (g_m) of the device increases by 12.40%, output conductance (g_d) is increased by 49.31%, early voltage (V_{EA}) is raised by 19.21%, gain of the device is increased by 3.6% and TGF is raised by 9.36%.

4. CONCLUSIONS

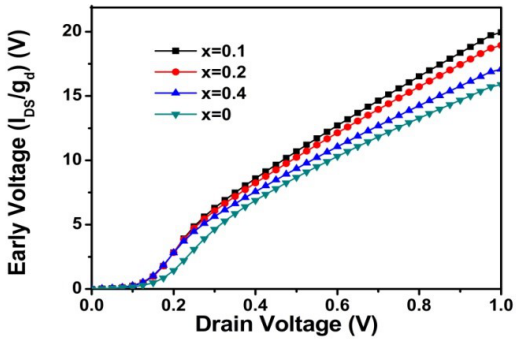
In this work, one optimum device, i.e. fully depleted strained gate stack double gate (FD-S-GS-DG) MOSFET is designed and simulated to study some aspect of its performance. Both DC and Analog performances are studied by varying the Ge mole fraction (X). The increase in strain, i.e., equivalent Ge content, enhances the performance of FD-S-GS-MOSFET in terms of electrostatic parameters as well in analog parameters because of an increase in the

Table 1: *Electrostatic parameters for different values of Ge Concentration.*

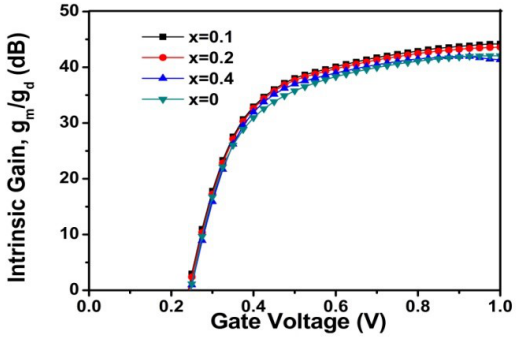
Ge Concentration (X)	V_{th} (V)	SS (mV/decade)	I_{on} (max) (mA)	I_{off} (A)	I_{on}/I_{off}
X=0	0.219	62.5057	1.910	3.05E-10	6.26E+09
X=0.1	0.213	62.6723	2.116	3.19E-10	6.12E+09
X=0.2	0.208	62.8793	2.166	3.40E-10	6.37E+09
X=0.4	0.202	63.2893	2.173	3.46E-10	6.28E+09

Table 2: *Analog parameters for different values of of Ge Concentration.*

Ge concentration (X)	g_m (max) (mA)	g_d (max) (mA)	V_{EA} (V)	Gain (dB)	TGF (V^{-1})
X=0	3.232	3.380	15.882	42.046	39.62
X=0.1	3.572	5.026	19.947	41.344	40.87
X=0.2	3.633	5.047	18.933	43.599	41.98
X=0.4	3.649	5.097	17.081	44.194	42.08



(a)



(b)

Fig.3: *(a) Early voltage (V_{EA}) variation with Drain voltage (V_{DS}) for different Ge concentration (X). (b) Intrinsic gain (A_V) as a function of Gate voltage (V_{GS}) for different Ge concentration (X).*

carrier mobility. Never the less, availability of few challenges are trivial even if a long list of advantages exist. According to our demonstrated results, there are undesirable side effects after certain amount of equivalent Ge content (i.e. X=0.4) such as an increase in SS value and a decrease in I_{on}, g_m, V_{EA} and gain (A_v) which may affect the device characteristics and performance significantly. Therefore, we conclude that strained silicon up to some extent of Ge mole fraction shows better results in device performances.

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