Design and implementation of a new multilevel push pull inverter topology

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ABSTRACT

The paper presents simulation and experimental results of a novel multilevel push pull inverter based multi-winding transformer. In the presented topology the most important advantage is that only one DC voltage source is used for generating the multilevel stepwise waveform in output voltage. Also, the number of switches in the suggested topology is reduced respect to conventional multilevel inverters. In the suggested inverter only one switch will be turn on in each interval and so the conduction losses of converter will decrease. The selective harmonic elimination (SHE) method is used for generating the gate pulses. Therefore the converter losses include switching losses and conducting losses, are reduced and so the efficiency of inverter is increased. Design procedure of transformer turn ratio is presented in this paper. The suggested topology is proposed to be a proper choice in low voltage, PV and dynamic voltage restorer (DVR) applications. The presented simulation and experimental results show the validity and effectiveness of proposed topology.

Keywords: Push pull inverter, Symmetric and asymmetric multilevel inverter, Selective harmonic elimination, Reduced switching device

1. INTRODUCTION

Recently expansions in the power electronic devices provide possibility of designing and implementing of novel power electronic inverters. Voltage Source Multilevel Inverter (MLI) is very suitable topology in high voltage range applications such as: power distribution, motor drive systems, power quality and power conditioning applications [1-5].

Many advantages of multilevel inverters in comparison with the two-level voltage converter can be listed as follow: Output voltage step is smaller, harmonic components are lower, electromagnetic compatibility and switching losses are better in multilevel converters. Also by increasing the number of levels in the converter, the output voltage has more steps generating a staircase waveform and so the harmonic distortion is reduced [6-7]. Some disadvantages of multilevel converters are: number of power electronic switches is increased, control scheme is complex, and tend to reduce the overall reliability and efficiency [8].

Diode-clamped, Flying capacitor, and cascaded H-bridge are the main fundamental multilevel topologies [9]. The Diode clamped multi-level inverter (DCMLI) and the Flying capacitor multilevel inverter (FCMLI) have complex control scheme because they require additional diodes and capacitors whereas the cascaded H-bridge (CHB) multilevel configuration is simple and its main advantage of it. However cascaded H-bridge converter requires a separate DC-link capacitor for each cell and therefore a control strategy is needed to regulate the voltage of DC link capacitors [9]. Today the available rating of the semiconductors is increased which is caused new topologies of multilevel converters by fewer numbers of semiconductors has been designed and implemented.

As mentioned in high voltage applications the cascaded H-bridge (CHB) topology is a good choice because this converter is the modular and the control of it is easy. But number of required separated voltage sources to supply each cell is high. To reduce it in high-voltage applications, cascade transformer-based multilevel converter has been presented [10-12]. Multilevel converters can be controlled by several modulation methods reported in [13-16]. Modulation methods based on switching frequency is classified into two categories, first group including high switching frequency methods such as: Space Vector Modulation (SVM), and Sinusoidal Pulse Width Modulation (SPWM). Second group including low switching frequency methods such as: Selective Harmonic Elimination (SHE), Minimization of the Total Harmonic Distortion (MTHD), and Space Vector Control (SVC) [17]. In the second group, switching frequency is low so switching losses is minimum also implementation of these converters is easy [18].

Commonly in SHE method, some algorithms such as: Resultant Theory, Newton-Raphson (N-R), Sequential Quadratic Programming (SQP), Homotopy algorithm, Genetic algorithm (GA), PSO and Harmony Search Algorithm (HSA) calculate switching angels as off-line. However among them resultant theory can find all solutions of the SHE equations, analytically [17].

In this paper a new topology of cascaded transformer multilevel family is proposed with one DC source and reduced number of switches which it pro-

Manuscript received on July 06, 2015 ; revised on August 28, 2015.

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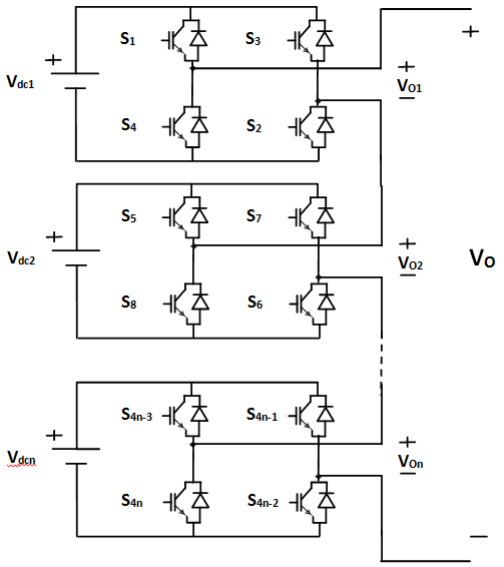

Fig.1: *Configuration of cascade multilevel converter.*

duces a large number of steps in output voltage. The main advantages of proposed topology beside reduce the number of power electronic devices and sources are low switching frequency of switches and easy implementation.

2. CASCADED H-BRIDGE MULTILEVEL CONVERTER

As mentioned, the cascade H-bridge converter is one of the more important multilevel converters which it is formed from series of multiple H-bridge units. In this converter a desired output voltage is generated from several separate DC sources. DC sources can be obtained from batteries, fuel cells, etc. Output phase voltage of a cascaded multilevel inverter is obtained by:

$$V_o = V_{o1} + V_{o2} + ... + V_{on} \tag{1}$$

Where, $V_{o1}, V_{o2}, ...V_{on}$ are the voltage of each H-bridge units as shown in Figure 1.

The maximum number of levels for phase voltage is given by equation (2) if the values of DC voltage sources are same:

$$\begin{aligned} m &= 2n + 1 \\ m &= \frac{l}{2} + 1 \end{aligned} \tag{2}$$

In this equation, n and m are the number of DC voltage sources and the maximum number of levels of phase voltage, respectively, and l is the number of switches.

However cascaded H-bridge multilevel converter needs to independent DC voltage sources in DC-links of bridges and it is main disadvantage of this topology which commonly cascade transformer-based multilevel converter has been presented to overcome it. This paper proposed a new transformer-based multilevel converter with fewer number of power electronic devices compared with conventional transformer-based multilevel converters.

3. PROPOSED TOPOLOGY

Figure 2 shows the proposed converter. It is clear from this figure which the proposed topology contained only one DC voltage source, multi-winding transformer, and unidirectional switches. Also to generate positive and negative output voltage level, proposed topology is separated into two symmetric parts. The switches S1, S2... Sn produce waveform with positive polarity by symmetrical steps and the complement switches S'1, S'2...S'n produce waveform with negative polarity.

With assumption the desired designing of transformer turn ratio, the maximum number of output phase voltage levels is given by:

$$m = l - 1 \tag{3}$$

Where, l and m are the number of switches and the maximum number of levels of phase voltage, respectively.

Operation of proposed topology for generating output voltage with symmetrical steps is based on multi-winding transformer turn ratio. If the all of primary side winding is energized, then output voltage will be having minimum level. In other words, by turning on upper switches sequentially and energizing the partially of primary side winding, the output voltage in secondary side is increased up to high level.

In proposed topology, to generate each level (positive or negative) always only one switch must be turned on. But in the conventional cascaded H-bridge multilevel converters with n DC voltage source, the number of on state switches is at least 2. Therefore the conductive losses and voltage drop in output voltage for proposed topology is very lower than cascaded H-bridge multilevel converter.

For limiting the di/dt in primary windings of transformer when output voltage's level has been changed from one level to other level, a short time overlaps (about μsec) must be applied to the gate signals of related switches. In other word, first next level switch turned on after a short time (μsec) the previous level switch turned off. For example, the gate signals of two switches are shown in Figure 3. Also, switches S_a, S_b are used to performed mentioned operation when output voltage's level has been changed from positive level to negative level and vice versa.

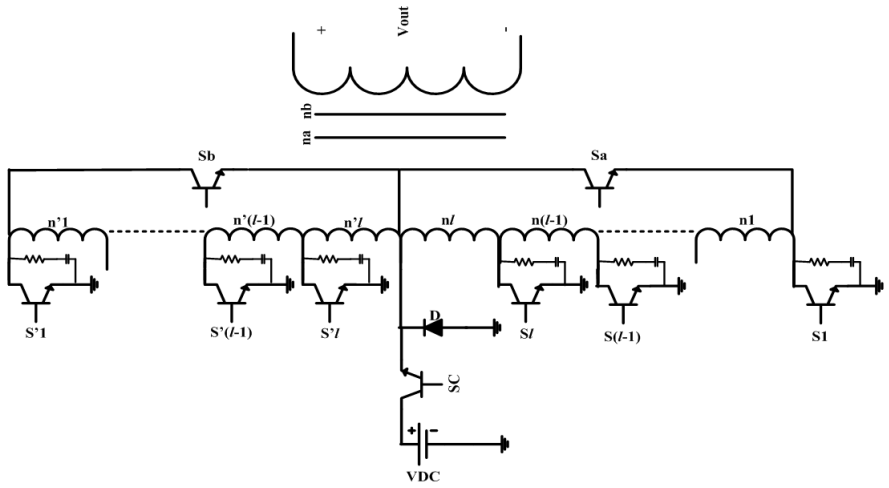

Fig.2: *Proposed multilevel converter.*

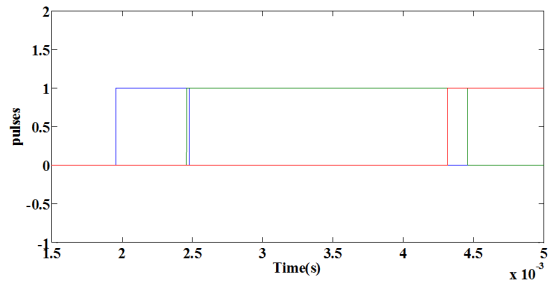

Fig.3: *Gate signals to show operation of switches.*

In this paper, a 9-level of proposed converter is surveyed and simulated to show performance of suggested converter. Figure 4 shows structure of 9-level proposed converter.

4. SETTING OF MULTI-WINDING TRANSFORMER TURN RATIO TO 9-LEVEL PROPOSED CONVERTER

To generate symmetrical steps in output voltage, transformer turns ratio are designed as follows:

To generate level +1 in output voltage, the switch S1 has to turn on and then all of transformer windings in primary side (n1, n2, n3, and n4) are energized, so:

$$\frac{n_b}{n_{a1}} = \frac{V_{out1}}{V_{dc}} \tag{4}$$

$$n_1 + n_2 + n_3 + n_4 = n_{a1} \tag{5}$$

Where n_b is secondary side turn ratio of transformer and is constant and n_{a1} is total value of primary side winding turn ratio. In this condition, the output voltage will be at the 1^{th} level. To generate level +2 in output voltage the switch S_2 has to turn on and other switches are turn off. Therefore the winding n2, n3, n4 in primary side are energized and so:

$$n_2 + n_3 + n_4 = n_{a2} \tag{6}$$

$$\frac{n_b}{n_{a2}} = \frac{V_{out2}}{V_{dc}} \tag{7}$$

Where n_{a2} is total value of primary's winding turn ratio in this condition.

Similarly, to generate level +3 and +4 in output voltage the switches S_3 and S_4 must be turned on respectively. For generating level +3 we have:

$$n_3 + n_4 = n_{a3} \tag{8}$$

$$\frac{n_b}{n_{a3}} = \frac{V_{out3}}{V_{dc}} \tag{9}$$

Where n_{a3} is total value of primary's winding turn ratio in this condition. Also, for generating level +4 will have:

$$n_4 = n_{a4} \tag{10}$$

$$\frac{n_b}{n_{a4}} = \frac{V_{out4}}{V_{dc}} \tag{11}$$

Where n_{a4} is total value of primary's winding turn ratio in this condition. Similarly, to generate negative levels of output voltage, complement switches S'_1, S'_2 S'_3, S'_4 turned on and create levels -1,-2,-3,-4 respectively.

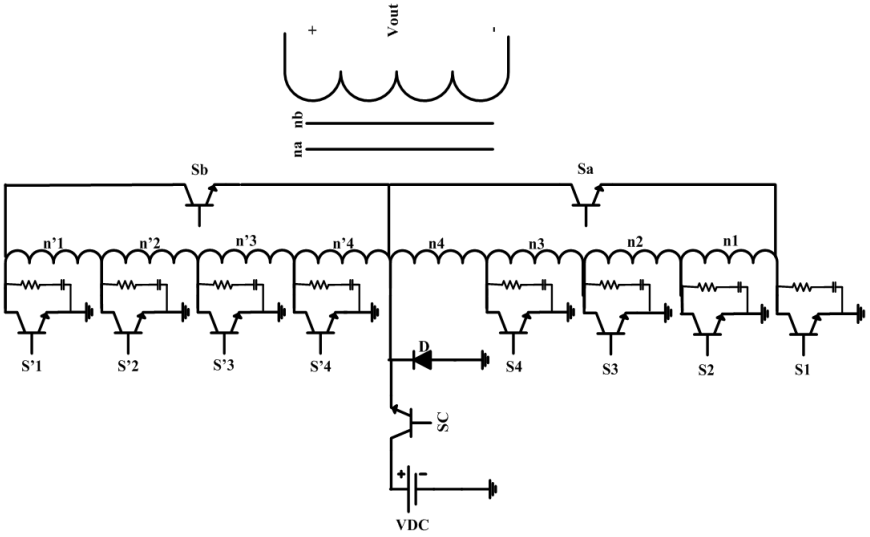

Fig.4: *Structure of 9-level proposed converter.*

5. SWITCHING ALGORITHM

Various modulation methods can be used for proposed multilevel converter. In this paper Selective Harmonic Elimination (SHE) strategy is selected to control proposed converter. In SHE method switching losses is minimum and implementation is easy.

Equation (12) can illustrate the Fourier series expansion for the output voltage waveform of the proposed converter:

$$V(\omega t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_{dc}}{n\pi}(\cos n\theta_1 + \cos n\theta_2 + \ldots + \cos n\theta_5)\sin n\omega t \quad (12)$$

Common methods in order to choosing the switching angles are: minimizing the total harmonic distortion (THD) or eliminating the lower frequency dominant harmonics. Using second method causes size of output filter for removing the higher frequencies components is reduced then this method is more popularity [17]. In this paper, the choice is to eliminate the lower frequency harmonics and consequently improving the THD of output voltage.

By determining desired switching angles in SHE method, desired amplitude of fundamental component is obtained and specific higher frequency components are removed. The multiples of third harmonics in each phase cancel in the line-to-line voltages then the mathematical statements of a 9-level converter (simulated in this paper) are given as follow:

$$\begin{aligned} \frac{4V_{dc}}{\pi}(\cos(\theta_1) + \cos(\theta_2) + \ldots + \cos(\theta_4)) &= V_1 \\ \cos(5\theta_1) + \cos(5\theta_2) + \ldots + \cos(5\theta_4) &= 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \ldots + \cos(7\theta_4) &= 0 \\ \cos(11\theta_1) + \cos(11\theta_2) + \ldots + \cos(11\theta_4) &= 0 \end{aligned} \quad (13)$$

One approach to solving nonlinear equation (13) and obtaining angles is to use an iterative method such as the Newton-Raphson method. Other approach is using of analytically methods such as resultant theory [17]. If the equation (13) solved correctly, in harmonic spectrum of 9-level output voltage there are not the 5^{th}, 7^{th} and 11^{th} order harmonic components [17-18].

In this paper desired amplitude of first harmonic has been generated with variable DC input, this means modulation index ($m = 4Vdc/\pi V1$) is constant. Then, in this work the best modulation index for minimum THD of 9-level voltage has been selected and related angels have been calculated to control proposed converter. By this operation, besides cancelling of the 5^{th}, 7^{th} and 11^{th} harmonics, THD of output voltage has a minimum value between other modulation indexes. [17].

For 9-level output voltage, between all modulation indexes, minimum THD of output voltage (5.45%), is pertained to m=0.685 where $\theta 1$=5.9°, $\theta 2$=35.24°, $\theta 3$=44.28° and $\theta 4$=77.72° leads to 5^{th}, 7^{th} and 11^{th} harmonics will be zero. Table.1 shows switching pattern for proposed converter to have a symmetrical output voltage without 5th, 7th and 11th harmonics.

6. LOSS STUDY

6.1 Power electronic losses

Commonly the losses of power electronic converters are divided into two groups, the conduction and switching losses. The conduction losses are caused by equivalent resistance and the on-state voltage drop of the semiconductor device and the switching losses are related to non-ideal operation of switches. Therefore the total power losses can be calculated as below:

$$P_{loss} = P_{cond} + P_{sw} \quad (14)$$

Table 1: *Switching pattern for proposed converter.*

STATE	ANGLE($\theta = \omega t$)	ON SWITCHES	OUTPUT LEVEL
1	$0 \leq \omega t \leq \theta_1 \& \pi - \theta_1 \leq \omega t \leq \pi + \theta_1$	-	0
2	$\theta_1 \leq \omega t \leq \theta_2 \& \pi - \theta_2 \leq \omega t \leq \pi - \theta_1$	S_1	+1
3	$\theta_2 \leq \omega t \leq \theta_3 \& \pi - \theta_3 \leq \omega t \leq \pi - \theta_2$	S_2	+2
4	$\theta_3 \leq \omega t \leq \theta_4 \& \pi - \theta_4 \leq \omega t \leq \pi - \theta_3$	S_3	+3
5	$\theta_4 \leq \omega t \leq \pi - \theta_4$	S_4	+4
6	$\pi + \theta_1 \leq \omega t \leq \pi + \theta_2 \& 2\pi - \theta_2 \leq \omega t \leq 2\pi - \theta_1$	S_1'	-1
7	$\pi + \theta_2 \leq \omega t \leq \pi + \theta_3 \& 2\pi - \theta_3 \leq \omega t \leq 2\pi - \theta_2$	S_2'	-2
8	$\pi + \theta_3 \leq \omega t \leq \pi + \theta_4 \& 2\pi - \theta_4 \leq \omega t \leq 2\pi - \theta_3$	S_3'	-3
9	$\pi + \theta_4 \leq \omega t \leq 2\pi - \theta_4$	S_4'	-4

In order to calculate the conduction losses, first of all, conduction losses of a typical power transistor and diode are calculated; then they are developed to the multilevel inverter. The average power losses of a power IGBT P_{cT} and diode P_{cD} can be written as (15), (16) respectively.

$$P_{cT} = \frac{D_T}{\pi} \int_0^{\pi} V_{CE} I_C d\theta \tag{15}$$

$$P_{cD} = \frac{D_D}{\pi} \int_0^{\pi} V_D I_D d\theta \tag{16}$$

Where are defined as follows:

$$V_{CE} = V_T + R_T I_T a \tag{17}$$

$$V_D = V_{fwd} + R_D I_{fwd} \tag{18}$$

To obtain the switching losses the linear approximation of voltage and current during turn-on and turn-off period is applied. Therefore energy losses during the turn-on and turn-off period of a switch can be formulated as follows:

$$E_{onT} = \int_0^{t_{on}} v(t)i(t)dt = \int_0^{t_{on}} \left(\frac{V_{swT}}{t_{on}}\right)\left(\frac{I'}{t_{on}}(t_{on} - t)\right) dt = \frac{V_{swT} I' t_{on}}{6} \tag{19}$$

$$E_{offT} = \int_0^{t_{off}} v(t)i(t)dt = \int_0^{t_{off}} \left(\frac{V_{swT}}{t_{off}}\right)\left(\frac{I}{t_{off}}(t_{off} - t)\right) dt = \frac{V_{swT} I t_{off}}{6} \tag{20}$$

Where, E_{offT} is the turn-off loss of the each switch, t_{off} is the turn-off time of the switch, I is the current through the switch before turning off, and V_{swT} is the off-state voltage on the switch. Also the turn-on time of the switch is t_{on}, I' is the current through the switch after turning on, and E_{onT} is the turn-on loss of the each switch.

The switching losses depend on the number of switching transitions, therefore not only they depend on power semiconductors characteristics but also they depend on the modulation method. Generally, the average switching power loss can be written as follows:

$$P_{sw} = 2f \left(\sum_{k=1}^{N_{sw}} \left(\sum_{i=1}^{N_{onk}} E_{onk,i} + \sum_{i=1}^{N_{offk}} E_{offk,i} \right) \right) \tag{21}$$

Where f is the fundamental frequency, N_{onk}, N_{offk} are the times of turning on and off the switch k during a half fundamental cycle. Also $E_{onk,i}$ is the energy loss of the switch k during the i^{th} turning on and $E_{offk,i}$ is the energy loss of the switch k during the i^{th} turning off.

6.2 Transformer losses

When input power is supplied to the primary of transformer, some portion of that power is used to compensate core losses in transformer and some portion of the input power is lost as copper (ohmic) loss and dissipated as heat in the primary and secondary windings, because these windings have some internal resistance in them.

Copper loss is RI2 loss, in primary side it is R1I12 and in secondary side it is R2I22 loss, where I1 & I2 are primary & secondary current of transformer and R1 & R2 are resistances of primary & secondary winding. As the both primary & secondary currents depend upon load of transformer, copper loss in transformer vary with load.

Hysteresis loss and eddy current loss both depend upon magnetic properties of the materials used to construct the core of transformer and its design. So these losses in transformer are fixed and do not depend upon the load current. So core losses in transformer which is alternatively known as iron loss in transformer can be considered as constant for all range of load. Hysteresis loss and eddy current loss in transformer is denote as:

$$W_h = K_h f B_m^{1.6} \tag{22}$$

$$W_e = K_e f^2 K_f B_m^2 \tag{23}$$

Where, Kh is Hysteresis constant, f is frequency, Ke is Eddy current constant, Kf is form constant.

7. SIMULATION RESULT

Computer simulation is performed using MATLAB/SIMULINK software in order to verifying the performance of the proposed converter. The main simulation parameters are listed in Table 2.

The 9-level propose converter is controlled by SHE method and operated with a fixed modulation index equal to 0.685 (m=0.685). In order to control output

Table 2: *Switching pattern for proposed converter.*

PARAMETERS	V_{DC}	FREQUENCY	LOAD
VALUE (UNIT)	30 (V)	50 (HZ)	30(Ω)-20 (MH)

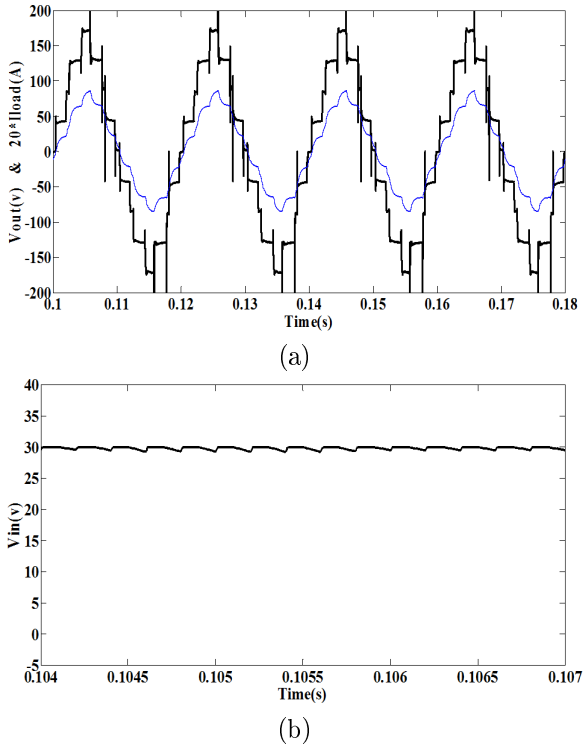

Fig.5: *Simulation results (a) output voltage (b) capacitor voltage at chopper output.*

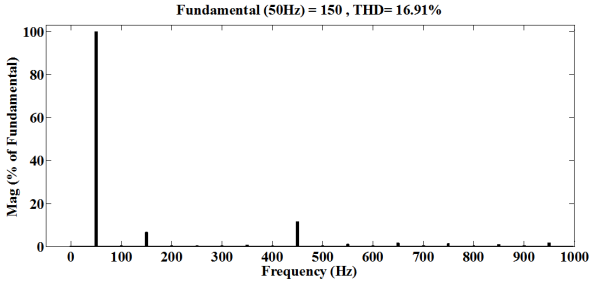

Fig.6: *Harmonic spectrum of output voltage.*

voltage, input DC voltage has been regulated using switch Sc. Figure 5 (a) shows output voltage and load current. Also output voltage of chopper is given in Figure 5 (b).

To show well-performance of proposed converter Figure 6 illustrated harmonic spectrum of output voltage. It is obvious that selected harmonics has been eliminated and THD of output voltage without any passive filter is low.

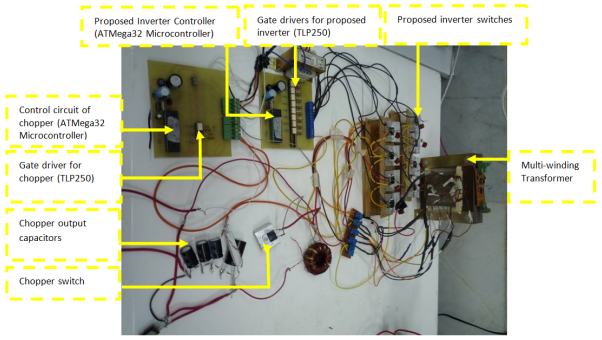

Fig.7: *Experimental prototype for the proposed nine level push pull inverter topology with chopper circuit in DC side.*

8. EXPERIMENTAL RESULT

In this paper a single-phase 9-level proposed converter has been implemented to validate the practicability of proposed topology that it is shown in Figure 7. The DC voltage is 12.5v, and the various R-L loads are connected to proposed converter.

The output voltages for various loads taken from the prototype converter without any output RLC filter is shown in Figure 8. The DC voltage in chopper output and ripple of this voltage has been illustrated in Figure 9 (a) and Figure 9 (b) respectively.

As mentioned, for limiting the di/dt in primary windings of transformer when output voltage's level has been changed from one level to other level, a short time overlaps (about μsec) must be applied to the gate signals of related switches, gate signal of switches has been shown in Figure 10.

The match between simulation and experimental results confirms the advantages and practicality of the proposed converter and its SHE control strategy.

9. CONCLUSIONS

This paper proposed a novel multilevel converter based on multi-winding transformer. The proposed configuration can reduce the number of switches and DC sources compared with conventional cascaded H-bridge multilevel converters. Also determination of transformers turn ratio for proposed converter has been introduced in this paper. The performance of the proposed multilevel converter has been verified by simulation and experimental results.

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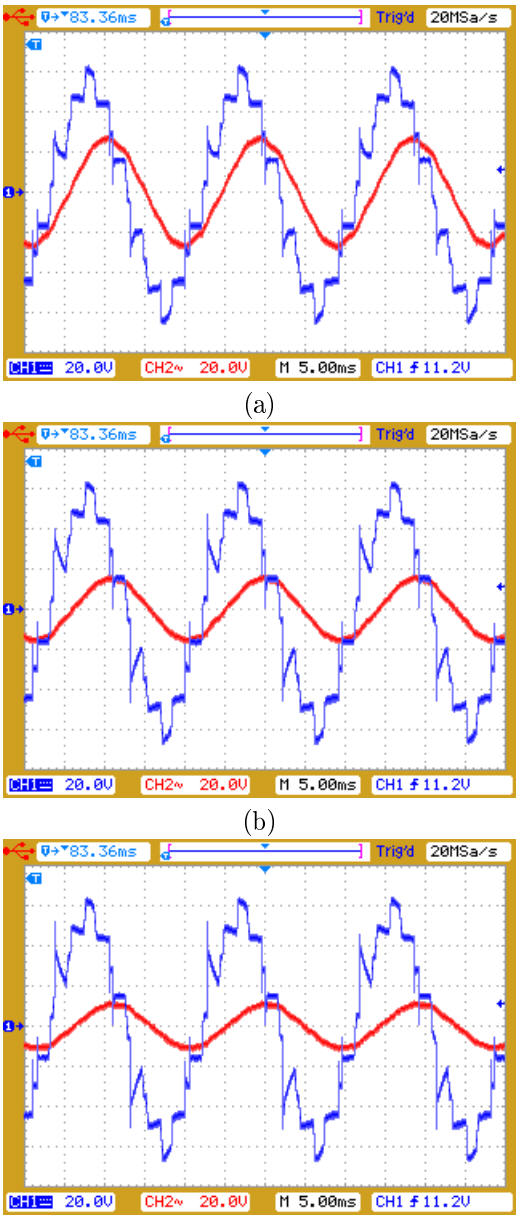
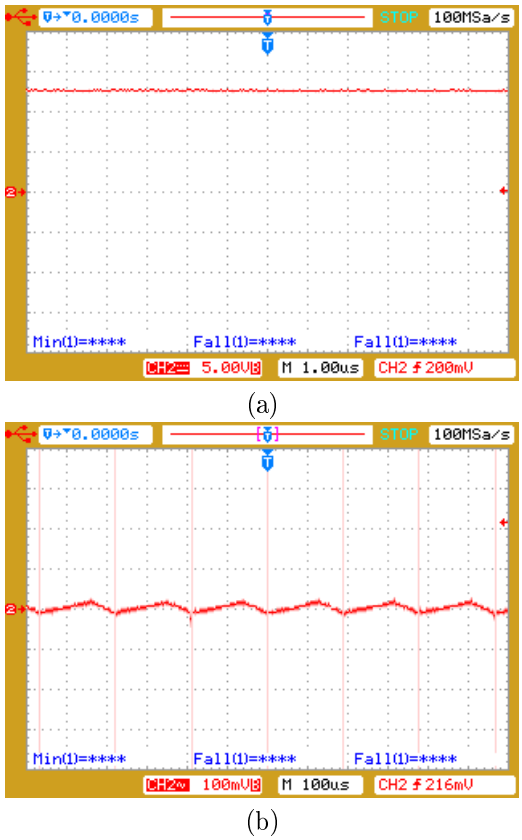


(a) (b) (c)

Fig.8: *Output voltage and load current (a)cosϕ = 0.9 (b)cosϕ = 0.8 (c) cosϕ = 0.65 .*



(a) (b)

Fig.9: *DC input voltage (a) DC voltage (b) ripple of input DC voltage.*

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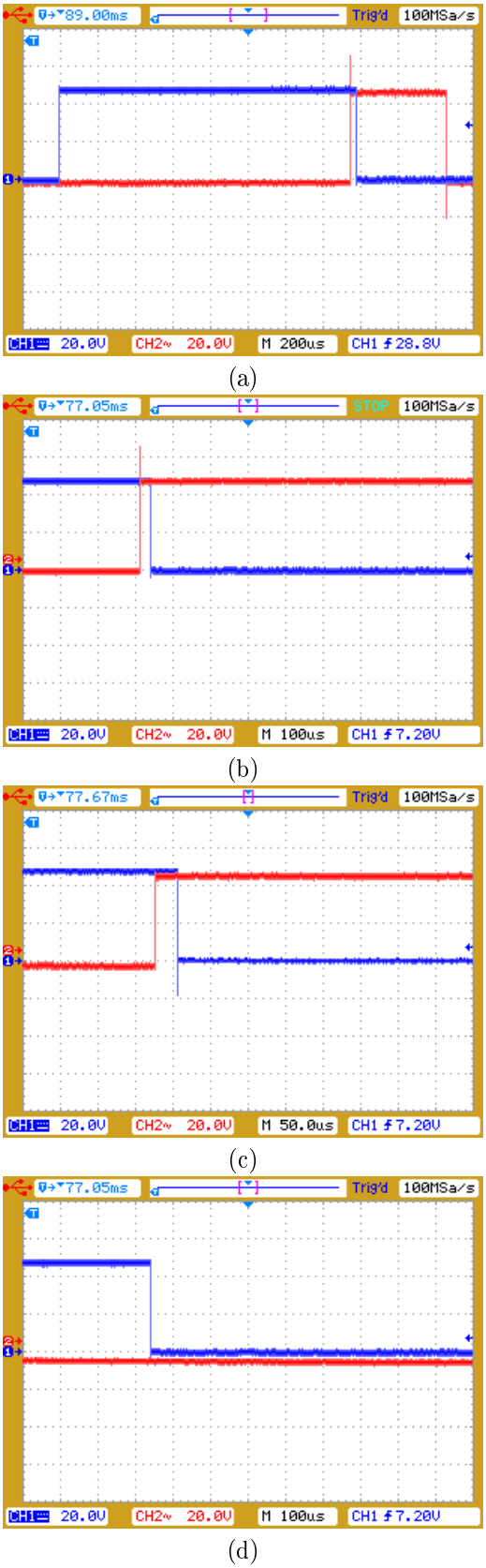

Fig.10: *Gate signal of switches.*

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