An All-Digital PLL Proposal using Gain Control Technique

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ABSTRACT

Time-to-digital converter (TDC) has been the main technique used in all-digital phase-locked loops (ADPLL). However, this approach has several design issues, and the solutions to resolve them always increase the complexity of the system. In this paper, an alternative method for handle the frequency error detection using a type II ADPLL architecture is presented. The proposed technique does not perform direct conversion from time to digital, but employs the discrete-time processing of compared signals from phase error detection. This architecture has the advantage of scalability and integration of all-digital techniques and has less complexity than conventional ADPLLs. The derivation of equations for the proposed architecture and its noise analysis is provided. The results are validated through system level simulations using macro-models of the devices. The result of the transient simulation shows the theoretical predictions about the trajectory of output frequency.

Keywords: Discrete-time model, Phase locked loop.

1. INTRODUCTION

Since the first all-digital PLLs the TDC is the main approach to digitize the measured phase error between reference frequency and output frequency [1], which has one of the main applications in the design of frequency synthesizer. The block obtains fine resolution in the conversion and therefore is suitable for the stringent specifications of wireless systems. Nevertheless, several issues in this method make the research remain focused on improving the resolution of the conversion [2], [3]. A different approach is to use a block that obtains the phase error given by a time interval value. This value is periodically sampled by a frequency that is several times higher than the reference frequency. In this approach, the direct conversion from time to digital is avoid, instead the digital word is generated after the digital integration of phase error. In the next section, an analysis of main issues of ADPLLs is accomplished and the advantages of proposed method are presented.

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2. ANALYSIS OF ADPLL DESIGN ISSUES

This section is divided into two parts: (2.1) the background to the ADPLLs design, and (2.2) a comparative analysis of frequency detection methods.

2.1 Background to the ADPLLs design

Most of architectures proposed in recent years must fall in the system shown in Fig. 1. Basically, TDC digitalizes the frequency difference between $f(F_{out})$ and F_{ref}, the phase error is processed by a digital loop filter, in order to ensure noise suppression and the stability of system. The tuning word is composed of the signal generated from the loop filter and some techniques for increasing the speed of frequency acquisition [4], [5]. The main design issues are related to phase noise balance and use of fractional techniques. For reasons that are explained with more detail in the next paragraph, the quantization noise has its value reduced when some design techniques are employed to improve the resolution of TDC. Due the use predominant of fractional-N frequency synthesizers, TDC is the better option since fractional division increases the requirements of conventional phase detector. However, TDC introduces more quantization error, and for reduce this source of noise is necessary improve its resolution. Thus, there are a trade-off between the quantization error and the complexity of TDC design.

The noise filtering schemes in ADPLLs has changed the issues because the noise sources are different than the analog approaches, but the trade-off between in-band noise and out-of-band noise remains the same as before. The in-band noise is now dominated by the noise of the time-to-digital converter (TDC) while the out-of-band noise is still dominated by the phase noise of the controlled oscillator which is now a digitally controlled oscillator (DCO) [6]. See Fig. 2 [7]. Regardless of how is generated the fractionary signal, PLL still can be affected by injection spurs and pulling effect. In ADPLL, the in-band spurs are intrinsic and coming from quantization error, due to the finite resolution of the time-to-

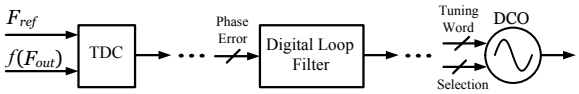

Fig.1: *Generic diagram for ADPLL using state of the art architectures.*

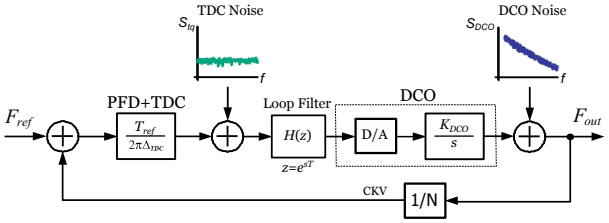

Fig.2: *Modelling of All-digital PLL.*

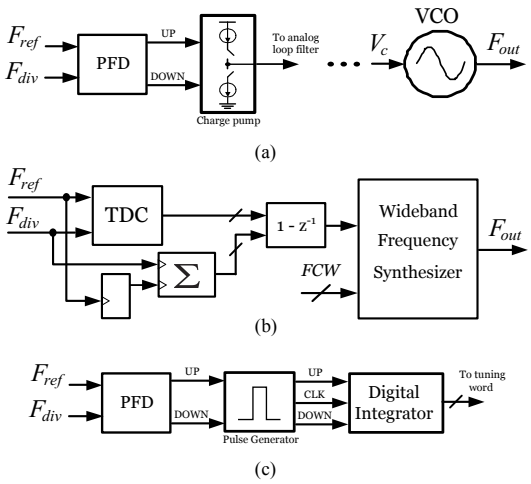

Fig.3: *Detail of phase error detection for (a) classical analog method, (b) the TDC-based frequency-to-digital conversion, and (c) the proposed phase error detector.*

digital converter (TDC) [2]. The effect of injection pulling, that also produces spurs, can be eliminated by the retiming method [8], which avoids the well-known method of transforming spur to noise, therefore the better way to improve the noise trade-offs in the ADPLL is to increase the resolution. Thus, the TDCs designs are focused on obtaining high resolution without generating spurious tones in the process. The main techniques are fractional counter vernier delay line [2] and gated ring oscillator-based TDCs [9].

2.2 Comparison between Methods

Methods for obtaining the phase/frequency error are illustrated in Fig. 3. Analog PLLs are well known and characterized [10], but do not have the scalability of the digital approaches. ADPLLs have become an attractive option for the design of frequency synthesizers with wideband frequency modulation [1]. However, the process to obtain the fractional frequency division is very complex. Basically, the ratio between output and input frequency is compared with the frequency control word (FCW) and thus the phase error is obtained. The retimed method is used to synchronize the edges of reference frequency with the output frequency. Otherwise, the PLL would face troubles with metastability and injection pulling.

In Fig. 3(c) is shown the mechanism of frequency error detection employed [11]. The charge pump absence in this method eliminates problems with amplitude noise or metastability. In its place has been used the digital integrator, which receives the sampled signal from PFD. The integrator is metastability free, because it is a synchronous circuit with in line clock, so TDC issues related to the nature of the delay chain do not occur in this circuit [12]. The pulse generation scheme provides a sampling process. The sampling process produces quantization error like the TDC-based method, but it generates less noise than when the whole circuit is analog. The digital PFD also features linearity problems, as the dead zone, but these can be solved by classical methods in the implementation [10].

In the method of Fig. 3(c) is applied the gain control technique [11]. An advantage of this technique is that it inherently avoids injection pulling. Due to the use of the technique of changing resolution during the settling process, PLL use a coarse adjustment of the output frequency until getting closer to the target frequency. Therefore, injected signal does not affect the PLL [13]. Furthermore, it will be demonstrated that the proposed architecture does not increase the phase noise significantly.

The following statements summarize why the proposed method has low complexity compared to using TDC. First, the TDC alone is not able to get the information of the phase difference and requires phase accumulators and synchronous samplers to determine it. The proposed architecture (see next section) provides the phase detection and filtering simultaneously. Second, the TDC requires the use of the retiming method to avoid metastability and injection pulling, but in the proposed architecture it is inherently avoided by using the gain control technique. Finally, current techniques for reducing the quantization error in TDCs generally increase the complexity and may cause metastability again [2], while in the proposed architecture the efforts to reduce the quantization error are focused on increase the clock of pulse generator.

3. PROPOSED ADPLL ARCHITECTURE

In the ADPLL architecture described in [14] a FDC (Frequency-to-Digital Converter) provides a digital word to be processed in the phase detection and filtering schemes. Alternatively, in the architecture proposed here the digital integrator is performed

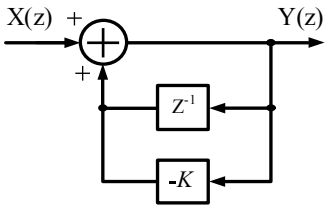

Fig.4: *Proposed Basic Cell.*

using counters [11], and receives the signal from the phase detection block to generate the digital word, which contrasts with previously mentioned. A type-II PLL can be used in this case, in order to get adequate noise filtering [14]. The main circuit is called basic cell, which produces the second pole of the type-II ADPLL. The whole architecture is a dual-path constituted from two PFD circuits. The equations of the architecture are provided below, including the noise analysis.

3.1 Basic Cell

The proposed basic cell is shown in Fig. 4. It may be noted that this diagram is part similar to a discrete integrator. The integrator function can be performed by using the method proposed in [11] and the gain K is used to generate a pole in discrete domain, as is deduced below

$$Y(z) = X(z) + Y(z)z^{-1} - Y(z)K \tag{1}$$

and solving for $Y(z)/X(z)$

$$\frac{Y(z)}{X(z)} = \frac{1}{(K+1)} \frac{z}{\left[z - \frac{1}{(K+1)}\right]}. \tag{2}$$

The continuous-time pole frequency can be found as $\omega_p = ln(1/(K+1))/T$, where Té the sample period and the transformation $Z = e^{sT}$ has been used.

The mechanism of the basic cell works as follows: First, the integrator is accounting the variation of phase error. A device produces a reduction in phase error that is proportional to integrator output value, which corresponds to the feedback loop with gain K. This device could use a variable delay block in order to control the phase of an input signal, and needs to be digitally programmable. Thus, the pole that is generated by the basic cell can be used in the design of a type 2 all-digital PLL, as shown in next section.

3.2 Type-II ADPLL Architecture

In Fig. 5 is presented an ADPLL architecture similar to the dual-path proposed in [11]. The basic cell creates a pole in discrete domain without to use analog devices, which makes the architecture all-digital. Next, one can show that this architecture has the characteristic of a type II ADPLL.

The PLL open loop transfer function can be derived as following. First, let us consider as a first approximation that the transfer characteristic of the variable delay block is linear. Thus, the equation derived in [11] can be used for represent the feedback signal as

$$\frac{V_{out}}{\Delta\varphi_0}(z) = \frac{K_{dig}T}{2\pi} \frac{z}{(z-1)}. \tag{3}$$

The gain $K_{dig}T$ is used in the DCO. Therefore, the tuning word (TW) is

$$\frac{TW_{out}}{\Delta\varphi_0}(z) = \frac{1}{2\pi} \frac{z}{(z-1)} \tag{4}$$

and for $\Delta\phi = \omega \times \Delta t$, where ω represents the reference frequency, it is necessary to compensate the time-to-phase conversion and the PFD gain, so the gain of the variable delay (K_{vd}) is

$$K_{vd} = K \Big/ \left(\frac{2\pi}{T_{ref}} \times \frac{1}{2\pi}\right) = K \times T_{ref}. \tag{5}$$

Then, the open loop transfer function can be obtained as a zero-order hold discrete equivalence of VCO multiplied for the discrete loop gain and 1/N. The VCO discrete equivalence is

$$\frac{TK_{VCO}}{(z-1)} \tag{6}$$

and from (2) and (3)

$$\begin{aligned} F(z) &= \tfrac{T}{2\pi}\left[e^{-aT}\tfrac{K_{1dig}z}{(z-e^{-aT})} + \tfrac{K_{2dig}z}{(z-1)}\right]\tfrac{TK_{VCO}}{(z-1)}\tfrac{1}{N} \\ &= \tfrac{TK_1K_{VCO}z}{(z-1)(z-e^{-aT})} + \tfrac{TK_2K_{VCO}z}{(z-1)^2}, \end{aligned} \tag{7}$$

where $\omega p = ln[1/(K+1)]/T, K1 = TK_{1dig}e^{-aT}/2\pi N, K2 = TK_{2dig}/2\pi N and\ a = \omega p.$

In the derivation of equation 7 has been taken into account the true nature of DCO, which provides output value in continuous time. The DCO has been modeled as a VCO, preceded by an ideal DAC. In this case, the $K_{DCO} = TK_{dig} \times K_{VCO}$. The dividers have been modeled by its gains in phase domain. The open-loop zeros are $z_1 = 0$ and

$$z_2 = \frac{e^{-aT}(K_{1dig} + K_{2dig})}{(e^{-aT}K_{1dig} + K_{2dig})}. \tag{8}$$

The dynamic and noise suppression of PLL can be designed, using equations 7 and 8 by adjusting ω_p and ω_z. In the next sections those topics are addressed in detail.

3.3 Noise Analysis

The main sources of noise of ADPLLs are the quantization noise t_q and the noise of the DCO θ_{DCO} (See Fig. 6). If θ_o is the output noise, one can obtain the

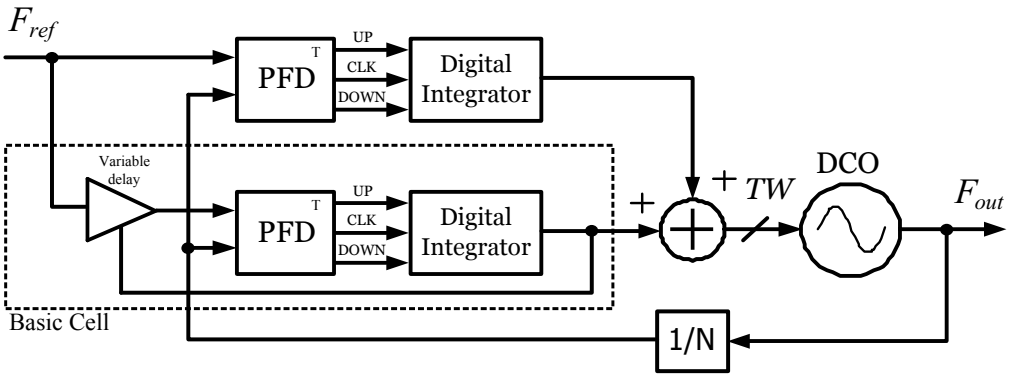

Fig.5: *Dual-path ADPLL Diagram using the Proposed Cell.*

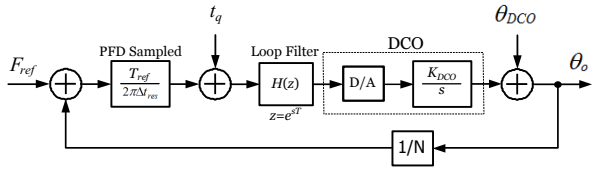

Fig.6: *Phase Domain Modelling of Proposed ADPLL.*

transfer function of the closed loop for noise sources as

$$\frac{\theta_o}{t_q} = 2\pi N \frac{F(s)}{1+F(s)} \tag{9}$$

$$\frac{\theta_o}{\theta_{DCO}} = \frac{1}{1+F(s)}, \tag{10}$$

where $F(s)$ is obtained as continuous equivalence.

The equation of in-band phase noise quantization contribution can be derived as in [14]. The variance of quantization error is proportional to resolution of converter, given by

$$\sigma_t^2 = \frac{(\Delta t_{res})^2}{12}. \tag{11}$$

In TDC, Δt_{res} is the inverter or buffer time delay. Similarly, in the proposed circuit the resolution depends on the clock of circuit of pulse generation.

The output phase noise due the quantization error is derived by the spectral density of noise (eq. 9) compensated for the sampling of reference frequency as [15]

$$S_\varphi = \frac{1}{T_{ref}} \left|\frac{\theta_o}{t_q}\right|^2 \frac{(\Delta t_{res})^2}{12} \tag{12}$$

If considered low frequency offsets so that the two approaches could be compared, the phase noise become

$$S_\varphi = 10 \log \left[\frac{1}{T_{ref}} (2\pi N)^2 \frac{(\Delta t_{res})^2}{12}\right]. \tag{13}$$

Such result is similar to TDC phase noise. Unfortunately, the proposed architecture cannot have a division ratio N as small as that of TDCs, usually between 2 and 4. Also, the fractional division in feedback path introduces spurs. It makes necessary to use integer-N methods so that the approaches can match.

3.4 Transient Response and Stability of Proposed ADPLL

The method used to study the transient response of the proposed ADPLL is to obtain the parameters in the continuous domain according to a second order approximation. These parameters allow analyzing the stability and transient response through classical performance metrics, such as phase margin, overshoot, steady state, etc. After obtaining the parameters, these methods can be adapted to the proposed architecture.

In Fig. 7 is shown the diagram for a regular analog loop filter to be compared with the proposed approach. The similarities become evident at end of derivation.

In a charge pump PLL (Fig. 7(a)), the output voltage for the analog loop filter can be derived as:

$$\begin{aligned} Z_{eq} &= R_1 + \tfrac{1}{sC_1} // \tfrac{1}{sC_2} \\ &= \frac{(sR_1C_1+1)}{(C_1+C_2)\left(\frac{sR_1C_1C_2}{C_1+C_2}+1\right)s}, \end{aligned} \tag{14}$$

where $\omega_z = \frac{1}{R_1C_2}$ and for $C1 >> C2 \Rightarrow \omega_p \approx \frac{1}{R_1C_2}$.

The ratio between the capacitances is

$$\frac{C_1}{C_2} = R_1C_1\omega_p - 1 = \frac{\omega_p}{\omega_z} - 1 \tag{15}$$

The open loop PLL transfer function can be written as [10]

$$H_{open}(s) = \frac{K_D K_{VCO}\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_p}\right)s^2} \tag{16}$$

where $K_D = \frac{I}{2\pi C_1 N}$.

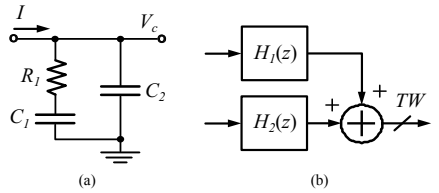

Fig.7: *Loop filter diagram using (a) analog elements, and (b) the proposed approach.*

Equation (16) is used to design the stability and design the noise suppression through the proper take of parameters. The transient response and settling time performance can be obtained by analyzing the closed loop transfer function $H_{closed}(s) = H_{closed}(s)/[1 + H_{closed}(s)]$. If it is assumed that $\omega_p >> \omega_n$, where $\omega_n^2 = K_D K_{VCO}$, then the system becomes second order

$$H_{closed}(s) \approx \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_z} + \frac{s^2}{K_D K_{VCO}}} \tag{17}$$

The term $s^3/\omega_p K_D K_{VCO}$ is neglected in the calculation above.

Finally, it should be noted that even the charge pump PLL is a discrete system sampled by the reference frequency. If $\omega_c << \omega_{ref}$, where ω_c is the crossover/loop bandwidth frequency, it can be approximated as [10]

$$\omega_c \approx \frac{\omega_n^2}{\omega_z} \tag{18}$$

Thus, the phase margin can be given as

$$\varphi_m = tag^{-1}\left(\frac{\omega_c}{\omega_z}\right) - tag^{-1}\left(\frac{\omega_c}{\omega_p}\right) \tag{19}$$

Equations (14) to (19) describe the main characteristics of transient response and stability of proposed ADPLL. In the case of ADPLL, the same approximation has been employed, but the parameters are calculated accurately by the method set forth in subsection 2.2.

In order to determine the natural frequency, equation (7) can be written as a second order approximation as

$$\frac{TK_{VCO}(K_1 + K_2)z\,(z - z_2)}{(z-1)^2}. \tag{20}$$

Taking into account a zero-order hold discrete equivalence, $\omega_p = ln[1/(K+1)]/T, \omega p = ln[z2]/T$, the continuous-time second-order approximation gives

$$\omega_n^2 = \frac{2K_{VCO}(K_1 + K_2)}{T} \times \frac{\omega_z}{\omega_p}. \tag{21}$$

Thus, the set of parameters required for PLL design is complete. According to (21), the natural frequency is proportional to $e^{-aT}K_{1dig} + K_{2dig}$. It can be shown that the ratio of the frequencies between pole and zero in continuous and discrete domain can be related to ratio K_{1dig}/K_{2dig}.

Making $\omega_p/\omega_z = \alpha$, then $|Z_2| = e^{\frac{-at}{\alpha}}$ and (8) can be rewritten as

$$\frac{e^{-aT}\,(K_{1dig} + K_{2dig})}{(e^{-aT}K_{1dig} + K_{2dig})} = e^{\frac{-aT}{\alpha}}. \tag{22}$$

The equation can be solved by applying logarithm properties as

$$\begin{aligned} &ln\left[\tfrac{(K_{1dig}+K_{2dig})}{(e^{-aT}K_{1dig}+K_{2dig})}\right] - aT = \tfrac{-aT}{\alpha} \\ &\Rightarrow ln\left[\tfrac{(K_{1dig}+K_{2dig})}{(e^{-aT}K_{1dig}+K_{2dig})}\right] = \tfrac{(\alpha-1)aT}{\alpha} \end{aligned} \tag{23}$$

and solving to K_{1dig}/K_{2dig}

$$\frac{K_{1dig}}{K_{2dig}} = \frac{e^{\frac{(\alpha-1)aT}{\alpha}} - 1}{1 - e^{\frac{-aT}{\alpha}}}. \tag{24}$$

Comparing $e^{\frac{1}{x}} \approx 1 + \frac{1}{x}$ with the exponential function expansion series, the next terms can be neglected if $x \to \infty$. Therefore, for $T \ll 1$

$$\frac{e^{\frac{(\alpha-1)aT}{\alpha}} - 1}{1 - e^{\frac{-aT}{\alpha}}} \approx \frac{\frac{(\alpha-1)aT}{\alpha}}{\frac{aT}{\alpha}} \tag{25}$$

and the solution of (24) become

$$\frac{K_{1dig}}{K_{2dig}} \approx \frac{\omega_p}{\omega_z} - 1. \tag{26}$$

Thus, the characterization of system in time-domain, such as transient response and the behavior in frequency domain, such as noise suppression, can be found. For instance, the digital gain is found through (21), the stability from (19) and the frequency response estimated from (18). As in the analog PLL design, all parameters depend on the ratio between ω_p and ω_z. Thus, the design is defined from equation (26), through the digital gains attributed to K_1 and K_2 in the DCO block. It should be noted that the proposed architecture, the gains K_1 and K_2 are changed during the locking process, so it cannot be taken the same design as in conventional PLLs.

4. RESULTS

Results are divided in transistor level simulation and system level simulations. In the transistor level simulation, the method of the phase error detection is presented using back-end design. In the system level, the results of the whole architecture are simulated using calibrated parameters from previous transistor level design. Although the design could be driven otherwise, for example in Field Programmable Gate Array (FPGA), the back-end results show that the method works, and so the implementation in other technologies is an option.

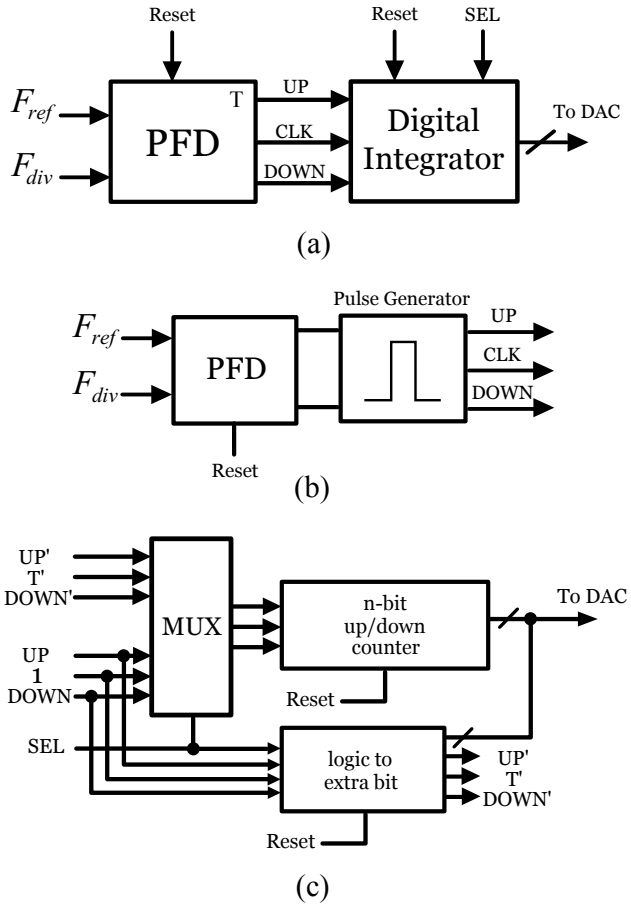

Fig. 8: *Phase Error Detector Diagram. (a) Overall circuit. (b) Detail of sampled PFD. (c) Detail of digital integrator.*

4.1 Phase Error Detector

Simulations have been obtained using 0.35-μm AMS parameters for Spectre^R. The diagram of circuit is shown in Fig. 8. The pulse generator circuit (Fig. 8(b)) extracts the value of the phase difference using the integrator (Fig. 8(c)). An ideal DAC has been used to generate the circuit output (See appendix A). The circuit provides the phase error detection by accumulating the phase error at output. A signal (SEL) selects the changes in resolution of the output frequency. The results are shown in Fig 9. The slope shows the increments in output through detection of signal UP. In this case, the signal SEL does not change.

4.2 Step Response of Architecture

System level simulations of proposed architecture have been performed in order to demonstrate the theoretical predictions. Device models are used for transient simulation with Simulink^{TM}. The blocks consist of macro-models that are equivalent to the architecture blocks. In this modeling, it is not necessary to know each particular block of ADPLL implementation. Therefore, the macro models are calibrated according to the average of cases found for this kind of purpose. In the following, the main features of modeling are listed.

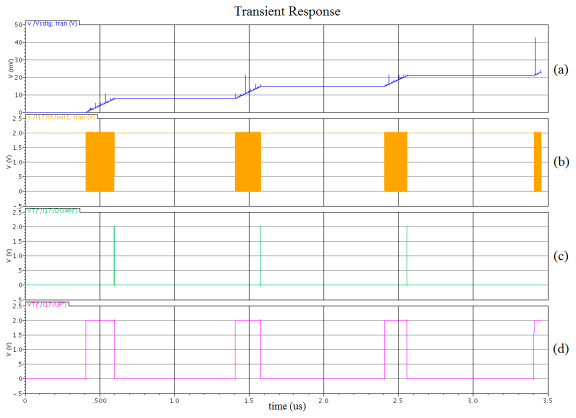

Fig. 9: *Simulated Phase Difference of circuit for (a) DAC output, (b) CLK signal, (c) DOWN signal, and (d) UP signal.*

1) **Combinational logic blocks:** In this case, each gate is modeled from their individual delays. The combination of these blocks represents the combinational circuit. In this architecture, all the blocks are sequential, but have the aforementioned characteristic as any sequential system has combinational circuits. The internal logic of sampled PFD block is illustrated in Fig. 10.

2) **Sequential logic blocks:** These blocks can be implemented with appropriate back-end cell-based design or behavioral description, as well as HDLs. In modeling of these blocks it is assumed that the project will get the best possible resolution. The macro-models are equivalent to the sequential logic circuit, but always using synchronous counters. For example, in the modeling of the digital integrator (Fig. 11) has been used up / down counters with logic to add more counters bits [11]. The blocks modeling of integrator are shown in Fig. 11 and Fig. 12. In the case of pulse generator block, an asynchronous circuit that oscillates at a very high frequency, triggered by a logic coming from phase difference detection circuit is applied [16]. For modeling this block is considered the minimum delay of technology (Δt_{res}). Characteristics of implementation that influence performance, such as consumption are not taken into account.

3) **RF blocks:** Despite what all-digital name indicate, ADPLLs implementation architectures may include passive components and analog blocks as well as the DCO. For example, the DCO can be modeled by blocks from the Simulink library, corresponding to VCO and a bit-to-integer converter. The frequency divider uses an integer divider with a fixed division. The two critical points of the modeling are due to the generation of the RF carrier: the signal distor-

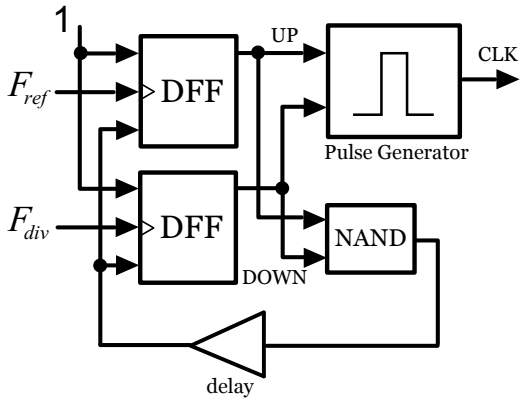

Fig.10: *Model of Sampled PFD Block.*

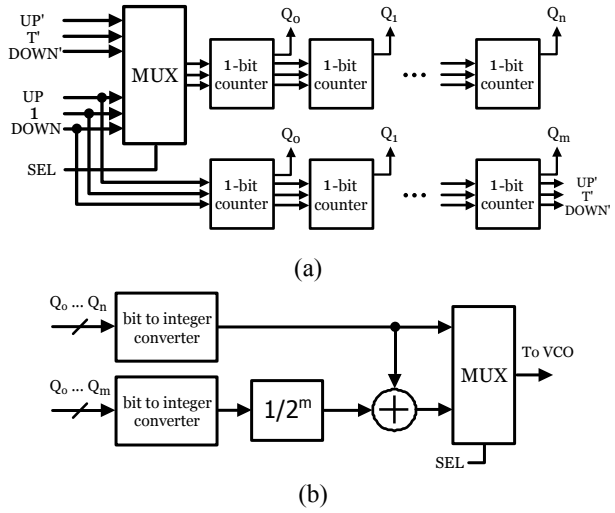

Fig.11: *Model of the proposed digital integrator circuit. (a) Overall diagram using 1-bit counters. (b) Conversion from tuning word to voltage.*

tion and the phase noise. Both can only be obtained after step response. Therefore, transient noise analysis is the most widely used approach to determining the phase noise of the PLLs. For qualitative analysis, the modeling of each block might include noise sources, which can be white or colored, and then the analysis is performed through appropriate choice of the simulation parameters. However, for quantitative analyzes are needed most accurate calibration methods, such as those based on PPV (Perturbation Projection Vector). Thus, the noise analysis has not been used.

4.2.1 Transient Simulation

Transient simulations with step of 40MHz have been accomplished. The responses present output values of the control voltage of PLL. In the modeling of architecture of Fig. 5 has been used the equations presented in section 3.4. The design include F_{ref} = 52MHz, N = 16, T = 1.5×10^{-9}s and a K_{VCO} = 2π×64MHz/V for an 832-872 MHz band.

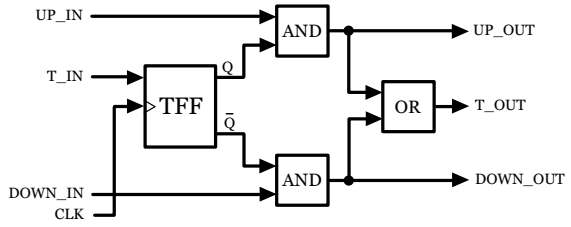

Fig.12: *Model for 1-bit counter.*

The parameters for simulation of three different runs are presented in Table 1. In appendix B one can find the equations used to get the parameters of Table 1. The equations are derived from (5), (7), (8) and (21). A ratio K_{1dig}/K_{2dig} of 15 is employed. The parameter K_{1dig} has been intentionally kept and K vary to change ω_p. The results are showed in Fig. 13. The regular trajectory of the type 2 PLL transient usually presents the effect of injection pulling. This behavior can cause serious instability problems. As illustrated in Fig. 14, the result indicates that the PLL is not affected by the injection pulling effect because of the trajectory without ripple. The basic cell use 18 bits working full time and 5 extra bits. The digital integrator block has switches the gain loop using the gain control technique. The detail for time of switching is presented in Fig. 15, where the 5 bits was added between 50Âţs and 60Âţs for switch the gain. The ADPLL works with 109Hz resolution at end, after switches the gain. This resolution is dominated by the integrator path. Note that after switches the

Table 1: *Design Parameters for Step Response Simulation.*

Parameters	Run 1	Run 2	Run 3
ω_p(rad/s)	1.3×10^{06}	2.6×10^{06}	5.2×10^{06}
K_{vd}(s)	3.75×10^{-11}	7.51×10^{-11}	1.51×10^{-10}
K	1.95×10^{-03}	3.91×10^{-03}	7.83×10^{-03}
p_1	9.98×10^{-01}	9.96×10^{-01}	9.92×10^{-01}
K_{dig}	8.72×10^{-04}	8.72×10^{-04}	8.72×10^{-04}
z_2	9.99×10^{-01}	9.99×10^{-01}	9.99×10^{-01}
ω_z(rad/s)	8.13×10^{04}	1.63×10^{05}	3.26×10^{05}

gain $\omega_p = ln[1/(\beta K + 1)]/T$, where $\beta = 1/2^m$ and m is the number of extra bits.

So, ω_p = 8.14 × 10^4 and ω_z= 5.09×10^3, after switch more 5 bits. The results shows that gain control technique improve the stability and frequency resolution.

5. CONCLUSION

In this paper, the use of other techniques for detecting output frequency error has been presented. The proposed architecture employs integrators based on the gain control technique to obtain a type-2 ADPLL. The main advantages are inherently avoids injection pulling and the low complexity of building blocks. Characterization of system has been obtained

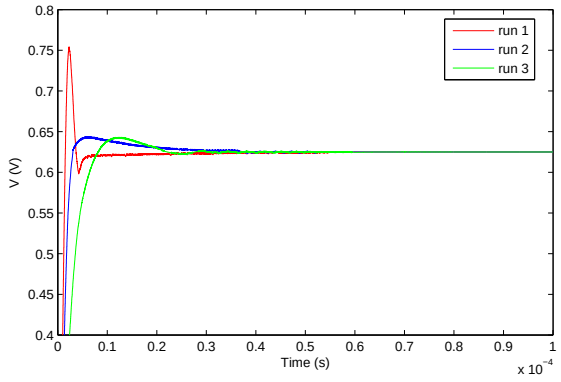

Fig.13: *Step response of ADPLL for different K values.*

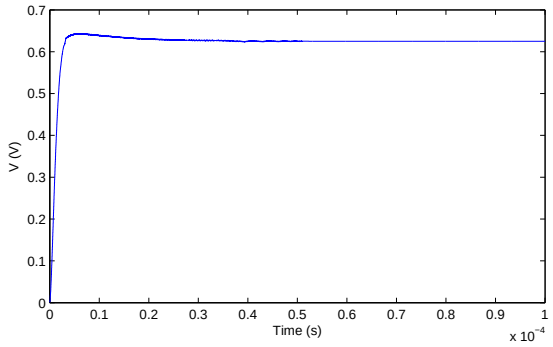

Fig.14: *Step response of ADPLL when* $K_{vd} = 7.51\times10^{-11}$, $K_{1dig} = 8.18\times10^{-04}$ *and* $K_{2dig} = 5.45\times10^{-05}$.

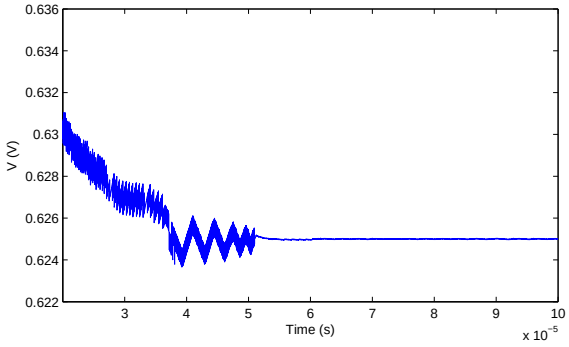

Fig.15: *Detail at the time of gain reduction.*

from the open loop discrete-time transfer function, where continuous-time equations have been related to discrete one. Compared to analog ones, the proposed method has better spur suppression and immunity to time or amplitude-domain perturbations, which significantly reduces the noise sources. Regarding the ADPLL using TDC, the proposed PFD has better linearity and avoid metastability. In addition, it has been shown that the proposed architecture does not increase the phase noise significantly. In order to demonstrate the proposed method, a transistor level simulation and system level simulations have been held. The transistor level simulation result has shown the process of phase error detection. The system level simulation serves to demonstrate the theoretical prediction about step response and to show a design example of architecture. The results showed that in the ADPLL using the gain control technique, the overshoot is reduced, and avoids instability. It has been shown that the gain control technique efficiently reduces the ripple presented when frequency getting close to lock, because the resolution influences the stability. A fast frequency settling approach based on adaptative loop bandwidth will be presented in future works.

APENDIX A

Verilog-A code to convert the tuning word to voltage.

Note that part of code is omitted
‘include“constants.vams” ‘include“disciplines.vams”
module DAC_ideal(IN, OUT);
parameter integer bits=23;
parameter real thr=0.5;
integer a[0:bits-1];
real b[0:bits-1];
integer i;
input [22:0] IN;
output OUT;
electrical [22:0] IN;
electrical OUT;
analog begin
@(initial_step) begin
for(i=0;i<=bits-1;i=i+1)begin
b[i]=pow(2,i)*(1.4476e-6);
end end
if(V(IN[0]) > 0.5) a[0]=1; else a[0]=0;
if(V(IN[1]) > 0.5) a[1]=1; else a[1]=0;
*condition from IN[2] to IN[21] has been omitted
if(V(IN[22]) > 0.5) a[22]=1; else a[22]=0;
V(OUT)<+(a[0]*b[0]+a[1]*b[1]+a[2]*b[2]+a[3]
*b[3]+a[4]*b[4]+a[5]*b[5]+a[6]*b[6]+a[7]*
b[7]+a[8]*b[8]+a[9]*b[9]+a[10]*b[10]+a[11]
*b[11]+a[12]*b[12]+a[13]*b[13]+a[14]*b[14]
+a[15]*b[15]+a[16]*b[16]+a[17]*b[17]+a[18]
*b[18]+a[19]*b[19]+a[20]*b[20]+a[21]*b[21]
+a[22]*b[22]);
end
endmodule

APENDIX B

%clc
wp=2.6e6
Kv=((1/(exp(-wp*15e-10)))-1)/52e6 %gain of
the variable delay
K=((1/(exp(-wp*15e-10)))-1)
p1=(exp(-wp*15e-10)) %discrete pole
Kdg=16*2*pi*(15e-10)*15*(((2*pi*25e3)^ 2))/(64e6)
%overall digital gain
Kd1=Kdg*(3.75/4);

```
Kd2=Kdg*(0.25/4);
z2=p1*(Kd1+Kd2)/(p1*Kd1+Kd2) %discrete zero
%
wz=log(z2)/15e-10 %continuous zero
```

6. ACKNOWLEDGEMENT

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