A Nonisolated Bidirectional ZVS Converter for Low Power Application

Mahmood Vesali[*1] and **Majid Delshad**[**2], Non-members

ABSTRACT

In this paper, a new zero voltage switching bidirectional DC-DC converter with low number elements is proposed. The synchronous rectification and soft-switching techniques are adopted to reduce the conduction loss and switching loss respectively. In the proposed converter any auxiliary circuits for providing soft switching conditions are not used, therefore the efficiency can be improved. In this converter the switches are gated with PWM signal and in complementary form, therefore the implementation of control circuit is simple. Since the proposed bidirectional DC-DC converter has only three main components with two snubber capacitors, the power density is very high. Simulation and experimental results verified the theoretical analysis and the efficiency of proposed converter in full load is about 96%.

Keywords: Bidirectional DC-DC converter, Zero voltage switching (ZVS), Zero current switching (ZCS), Pulse width modulation (PWM).

1. INTRODUCTION

Nowadays the development and application of bidirectional dc-dc converters has become an important topic in power electronics. Bidirectional DC-DC converters are capable of reversing the direction of current flow and thereby the power flow between two DC sources. These converters are widely used in many industry applications. In equipment such as uninterruptible power supplies [1], fuel cell power systems [2], [3], hybrid electric vehicle [4]-[7], solar cell power systems [8], bidirectional DC-DC converters are applied to manage power flow and store energy for use in necessary times.

Bidirectional DC-DC converters are divided into nonisolated [5] and isolated [8]. The nonisolated type are always simple in structure and control. If high-voltage ratio and isolation are required, isolated type are used which increase cost and losses. In order to significantly reduce reactive component size and cost, switching frequency should be increased. But in hard switching bidirectional converters switching frequency is limited. To solve this problem soft switching converters introduced.

Zero-voltage switching (ZVS) and zero-current switching (ZCS) are two techniques that provided soft switching condition into conventional pulse width modulation (PWM) converters [9], [10] in order to reduced switching losses. In ZVS and ZCS converters used one or two auxiliary switches which provide soft commutation in both modes of operation of converters. However, due to the bidirectional characteristic of this converters, using several auxiliary elements is inevitable [11]. ZVS converters are proposed in [12] and [13] where all switches are soft switched and duty cycle is not limited. However, in [13], two split input voltages are required by means of inserting two equal capacitors between the input line and ground. Moreover, in order to balance the capacitors, the auxiliary switch are gated by twice of main switching frequency, resulting in more complex control circuit and switching losses. In [12] soft switching condition created with one auxiliary switch in two power direction, but the switches are not gated in complementary form and the control of this converter is difficult.

In this paper a new bidirectional converter without auxiliary circuit is introduced. In the proposed converter, soft switching is developed for two direct of power flow in zero voltage switching (ZVS) condition. Also, by reducing the number of elements in proposed converter, cost and volume decreased. This converter is suitable choice for low power applications.

The proposed ZVS bidirectional buck and boost converter is analyzed, and its operation is described in section 2. Design procedure are presented in section 3, simulation and experimental results of the proposed converter are presented in section 4, and conclusion of proposed converter presented in section 5.

2. CIRCUIT DESCRIPTIONAND OPERATION

The proposed converter is shown in Fig1. This converter operates at six intervals in both buck and boost modes. The key waveforms of converter in buck mode are introduced in Fig2.

For simplicity of circuit analysis, the following assumptions have be considered.

•The capacitors in the input and output of bidirectional converter are large enough, therefore the input and output voltage is considered to be fixed.

Manuscript received on June 28, 2016 ; revised on August 7, 2016.

* The author is with Department of Electrical Engineering, Isfahan (Khorasgan) Branch, Islamic Azad University, Isfahan, Iran, E-mail : mahmoodvesali645@gmail.com[1]

** The author is with Department of Electrical Engineering, Isfahan (Khorasgan) Branch, Islamic Azad University, Isfahan, Iran, E-mail : delshad@khuisf.ac.ir[2]

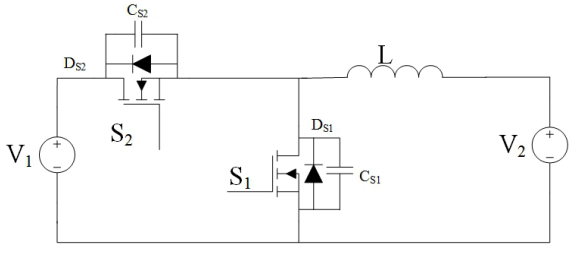

Fig.1: *Proposed soft-switching bidirectional converter.*

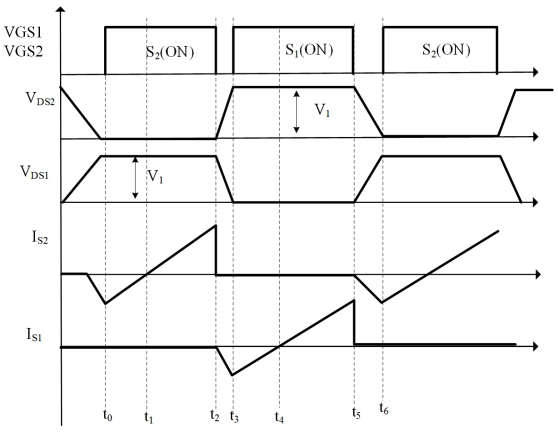

Fig.2: *Key waveform of proposed converter for buck operation.*

•All semiconductor devices are ideal.

2.1 The buck mode of operation

First assumed that S_2 is off and body diode of S_2 conducts and the energy of L is discharged to high voltage side.

Mode $1(t_0 - t_1)$: At t_0, the power switch S_2 is turned on with zero voltage switching (ZVS) condition, because of conducting S_2 body diode in mode 6. The current of inductance L (i_L) will increase linearly because the voltage across L is constant and equal to $(V_1 - V_2)$. When the current is zero this mode ends.

Mode $2(t_1 - t_2)$: By changing the direction of switch current, the current transfer from body diode of switch to switch S_2 and increase with the same slope in previous mode. This mode ends when S_2 is turned off.

Mode $3(t_2 - t_3)$: In this mode, S_2 is turned off with ZVS due to snubber capacitor of S_2. i_L charges D_{S2} and discharges D_{S1} and when C_{S1} is discharged completely and turns on D_{S1} to clamp S1 voltage to zero this mode ends.

The duration of this mode is calculated from (1).

$$t_{32}=\frac{(C_{S1}+C_{S2})\,V_1}{I_{Lmax}} \tag{1}$$

Mode $4(t_3 - t_4)$: D_{S1} turns on to clamp S_1 voltage at zero. Therefore ZVS condition provided for S_1. In this mode, S1 is turned on with ZVS condition duo to D_{S1}. The voltage across L is constant and equal V_2, thus i_L decreases linearly. The slop of decreasing current equals to (V_2/L).

Mode $5(t_4 - t_5)$: In this mode the current of S_1 become positive and increases with previous slope. At t_5, S_1 is turned off and this mode ends.

Mode $6(t_5 - t_6)$: When S_1 is turned off under ZVS duo to C_{S1}, L starts to charge C_{S1} and discharge C_{S2}, this mode begins. When C_{S2} discharges completely, the body diode of S_2 conducts and this mode finishes.

The equivalent of these six modes in buck operation is introduced in Fig 3.

2.2 The boost mode of operation

For the boost mode, the proposed converter operates similar to buck mode. To summarize the body of this paper the intervals of boost modes operation is ignored. The equivalent circuits of boost mode operation is shown in Fig 4.

3. DESING PROCEDURE OF PROPOSED CONVERTER

3.1 Snubber capacitors

For snubber capacitors design the [14] is used, witch in this reference the capacitors design for all converter have been described.

The snubber capacitor can be obtained as below:

$$i_{CS}=\frac{I_O t}{t_{fi}} \qquad 0 < t < t_{fi} \tag{2}$$

$$V_{CS}=V_{DS}=\frac{1}{C_S}\int_0^t i_{CS}dt=\frac{I_O t^2}{2C_S t_{fi}} \tag{3}$$

$$C_S=\frac{I_O t_{fi}}{2V_{DS}} \tag{4}$$

Where t is time and I_o is output current in buck or boost mode and t_{fi} is falling time of switch current.

3.2 Selection of inductor

For inductor design two conditions must be satisfied. First, to transfer power to the output, the slop of inductor current should be high. Therefore the inductor must be designed small enough. Second, to provide ZVS condition for switches, the inductor must be large enough.

Therefore the peak-to-peak current of L is calculated from (5).

$$\Delta I=\frac{V_2\,(1-D)\,T}{L} \tag{5}$$

Where (1-D) is the duration of fourth mode. The minimum current value of L is obtained from (6) and (7).

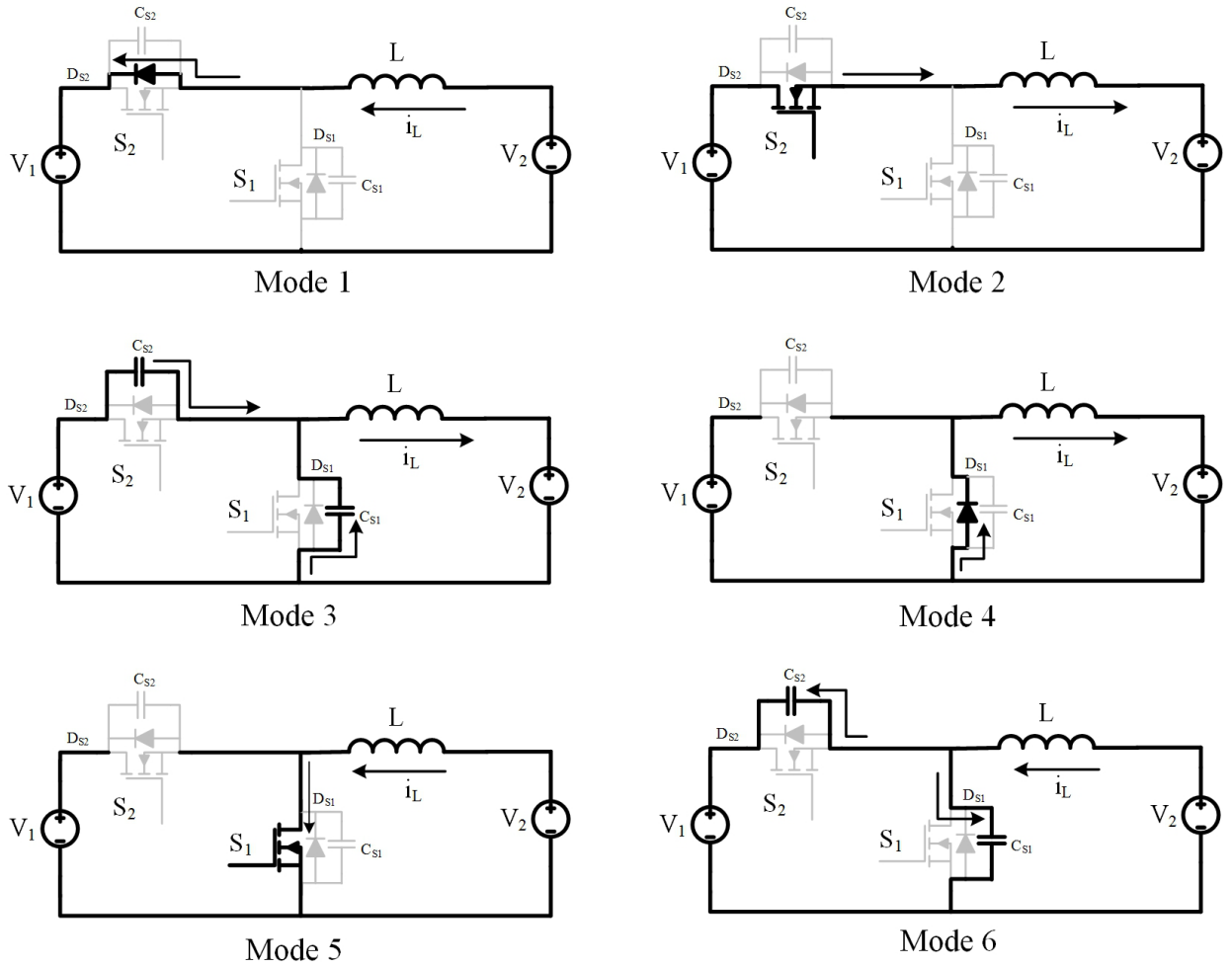

Fig.3: *Equivalent of circuit diagram for buck operation.*

$$I_{L,max}=\frac{\Delta I}{2}+I_O=\frac{V_2\,(2-D)\,T}{2L}+I_O \tag{6}$$

$$I_{L,min}=\frac{\Delta I}{2}-I_O=\frac{V_2\,(2-D)\,T}{2L}-I_O \tag{7}$$

Where Io is output current in buck operation.

As described in section 2, the minimum inductance current ($I_{L,min}$) discharges C_{S2} and charges C_{S1} to provide the ZVS condition of S_2, also the maximum inductance current ($I_{L,max}$) discharges C_{S1} and charges C_{S2} to prepare the ZVS condition S_1.

$$\frac{1}{2}\,(C_{S1}+C_{S2})\,V_C^2 \le \frac{1}{2}L\left(\frac{V_2\,(1-D)\,T}{2L}-I_O\right)^2 \tag{8}$$

$$\frac{1}{2}\,(C_{S1}+C_{S2})\,V_C^2 \le \frac{1}{2}L\left(\frac{V_2\,(1-D)\,T}{2L}+I_O\right)^2 \tag{9}$$

It can be deduced from (8) and (9) that the critical requirement for S_2 or S_1 to realize ZVS is that the energy in the L is large enough to completely discharge C_{S1} or C_{S2}. The IL can be assumed constant during the dead-time because the interval is very short, in other words, a constant current source, which its value is (V_2(1-D)T/2L-I_o), discharges C_{S2} and charges C_{S1} for providing ZVS of S_2, also the constant current source, which its value is (V_2(1-D)T/2L+I_o), discharges C_{S1} and charges C_{S2} for providing ZVS of S_1.

Since $I_{L,max} > I_{L,min}$, so it is harder to provide ZVS condition for S_2 than S_1.

Therefore, to design inductor L the equation (9) should be assumed. To ensure providing ZVS condition the duration of modes 2 and 6 depends on $I_{L,max}$ and $I_{L,min}$ should be calculated according to equation (10) and (11).

$$t_{dead1,min}=t_{32}=\frac{(C_{S1}+C_{S2})\,V_1}{I_{L,max}} \tag{10}$$

$$t_{dead1,max}=t_{65}=\frac{(C_{S1}+C_{S2})\,V_1}{I_{L,min}} \tag{11}$$

According to the above discussion the maximum value of inductor can be calculated in (12).

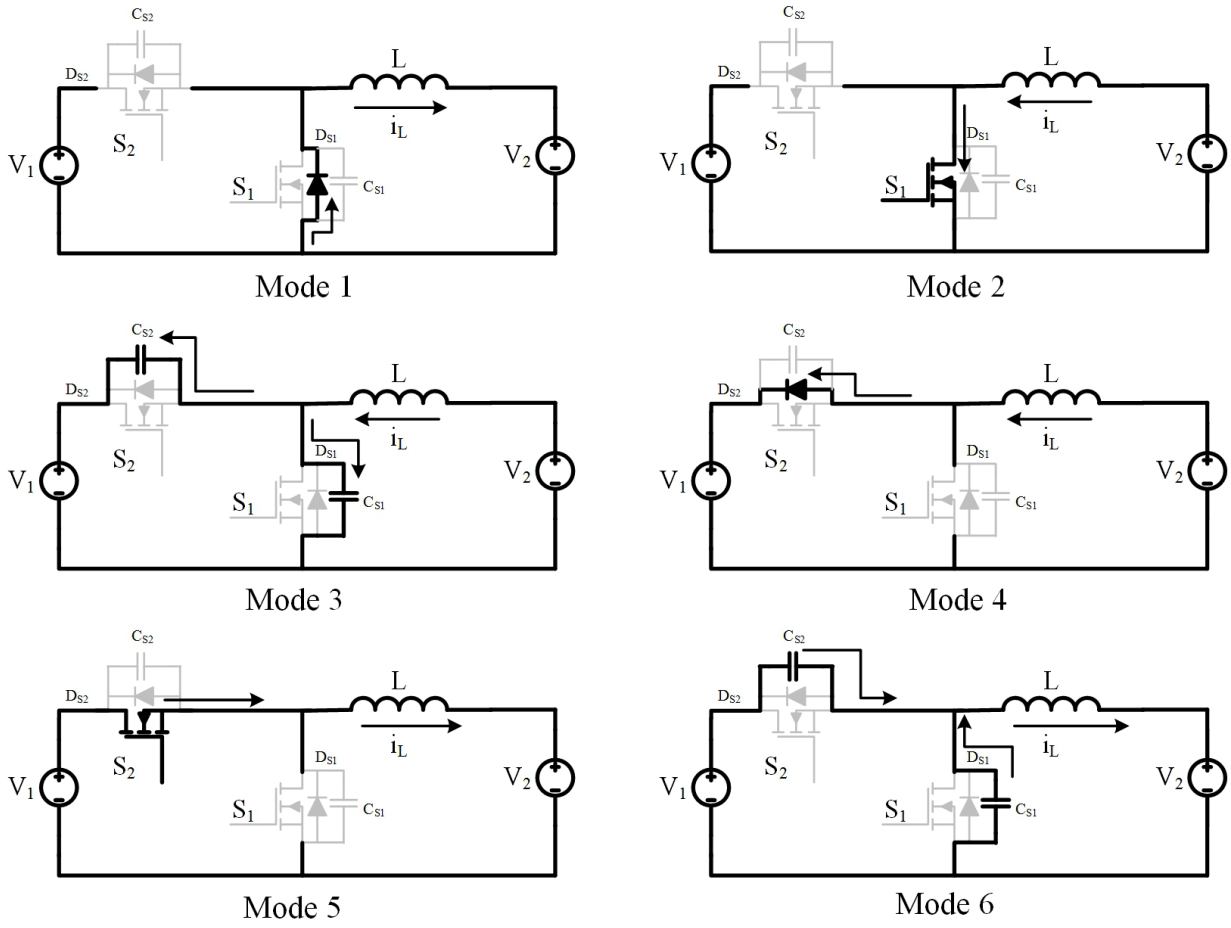

Fig.4: *Equivalent of circuit diagram for boost operation.*

$$L_{max}=\frac{V_2\,(1-D)\,T}{\frac{2(C_{S1}+C_{S2})V_1}{t_{dead1,max}}+2I_O} \tag{12}$$

With using (11) and (12) can be defined L_{max} according to below $t_{dead1,max}=\frac{(2\times10^{-9})100}{2}=200ns$ Where C_{S1} and C_{S2} equals to 1nF $L_{max}=\frac{50(1-0.5)10\times10^{-6}}{\frac{2(2\times10^{-9})100}{100\times10^{-9}}+6}=25\mu H$ Which in this paper L is selected 22μH.

By using (8) and (9) equations L_{min} and L_{max}can be determined with respect to power and duty cycle and CS, as shown in Fig 5 and Fig 6.

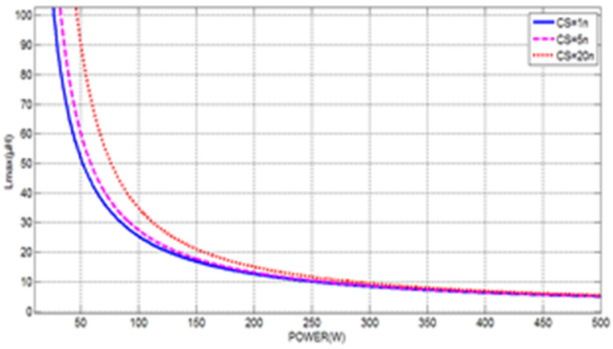

Fig.5: *L_{max} according to power and CS.*

3.3 Voltage gain in buck mode

To obtain voltage gain of the proposed converter, first D_{loss} should be calculated from (13).

$$D_{Loss}T=\frac{I_O L}{(V_1-V_2)} \tag{13}$$

Where D_{loss} is lossing duty cycle in proposed converter when the body diode of switch is conducted which is shown in Fig 7, and IO is output current in low voltage side.

$$D_{Loss}=\frac{I_O\times L\times f}{(V_1-V_2)} \tag{14}$$

Since voltage gain of proposed converter in buck mode is obtained according (15).

$$Gain=[D-D_{LOSS}] \tag{15}$$

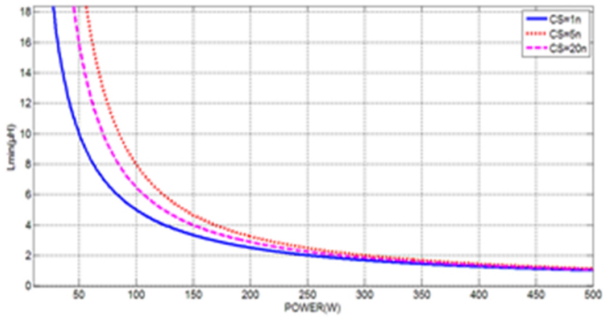

Fig.6: *L_{min} according to power and CS.*

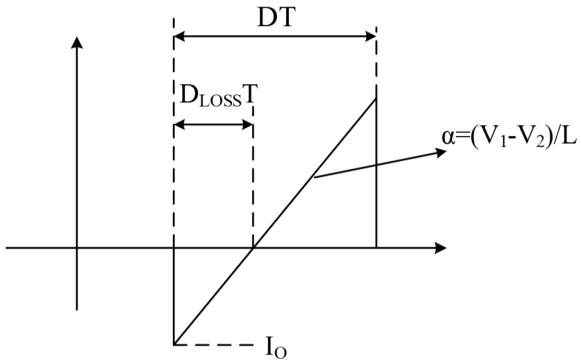

Fig.7: *Duty cycle loss in switch current.*

$$Gain = D - \frac{I_O \times L \times f}{(V_1 - V_2)} \tag{16}$$

By using voltage gain of proposed converter in buck mode, the plotted curves in Fig 8 can be obtained which shows the relation between gain and power of proposed converter versus duty cycle.

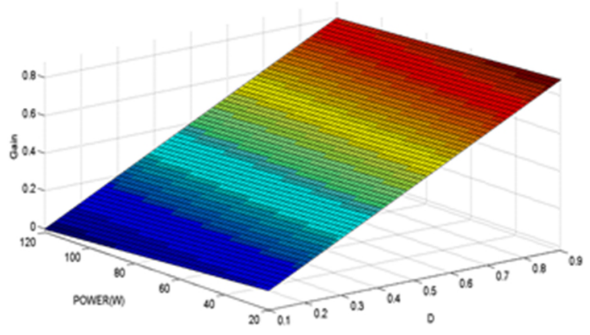

Fig.8: *Voltage gain in according to power and D in buck mode (f_{sw}=100kHZ and L=22μH).*

3.4 Voltage gain in boost mode

In boost mode to calculate voltage gain of proposed converter, first D_{Loss} obtains from (17).

$$D_{Loss}T = \frac{I_{in}L}{(V_2)} \tag{17}$$

Where D_{Loss} is lossing duty cycle in proposed converter when the body diode of switch is conducted according Fig 9.

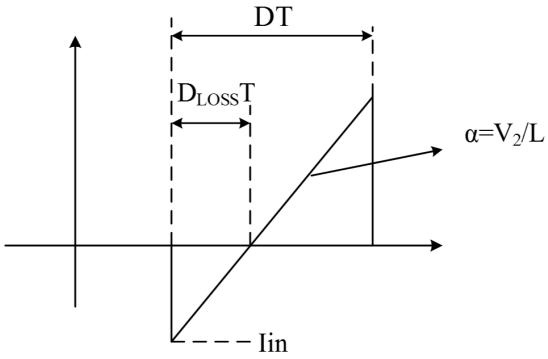

Fig.9: *Duty cycle loss in switch current.*

$$D_{Loss} = \frac{P \times L \times f}{V_2^2} \tag{18}$$

Where P is output power of proposed converter.

Therefore the boost mode voltage gain of proposed converter can be obtained from (20).

$$Gain = \frac{1}{1 - (D - D_{LOSS})} \tag{19}$$

$$Gain = \frac{1}{1 - \left(D - \frac{P \times L \times f}{V_2^2}\right)} \tag{20}$$

For simplicity design of proposed converter, the shown curve in Fig 10 is introduced. In Fig 10, shows the voltage gain in terms of variation of power and duty cycle.

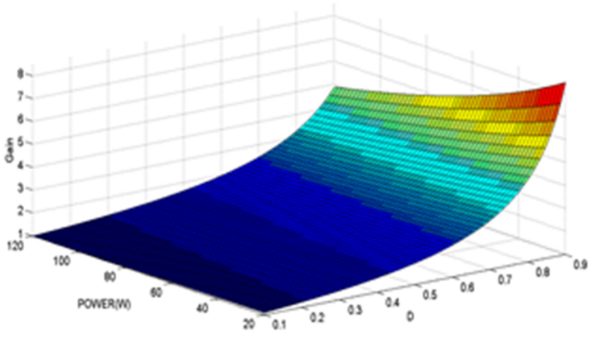

Fig.10: *Voltage gain in according to power and D in boost mode (f_{sw}=100kHZ and L=22μH).*

4. SIMULATION AND EXPERIMENTAL RESULTS OF PROPOSED CONVERTER

4.1 Simulation result

To verify theoretical analysis, the operation principle of soft-switching buck and boost converter has been simulated by PSPICE software. The parameters used in the simulation are listed in Table 1 that is calculated by using introduced equations and figures in section 3.

Table 1: *Parameters of simulation.*

component	symbol	value
Input voltage	V_1	100v
Output voltage	V_2	50v
inductor	L	22μH
Duty cycle	D	0.5
Switching frequency	f_{SW}	100KHz
switch	S_1, S_2	IRF640
Snubber capacitors	C_{S1}, C_{S2}	1nF

Fig 11 shows the drain current and drain-source voltage of S_2 when the converter operates in buck mode. As can be seen in this Fig the switch current is negative when the switch turned on, therefore the body diode is conducted and ZVS condition for turn on instant is introduced.

It is illustrated in Fig 11, the voltage of the switch S_2 rises with slope and therefore almost ZVS condition for turn off instant is prepared.

Fig 12 shows the drain current and drain-source voltage of S_1 when converter operates in buck mode. Similarly Fig 13 and Fig 14 show the drain current and drain-source voltage of S_1 and S_2 when converter operates in boost mode.

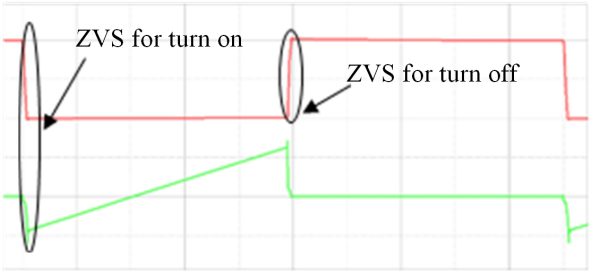

Fig.11: *The simulation results of drain current (bottom) and drain-source voltage (top) of S_2 when converter operates as buck mode (vertical scale 20 volt/div or 2A/div, time scale 1μs/div).*

4.2 Experimental result

To verify theoretical analysis and simulation results, this circuit is made with parameters in table I that are shown in Fig 15 and experimental results of current and voltage S_2 and S_1 are shown in Fig 16,17,18, and 19.

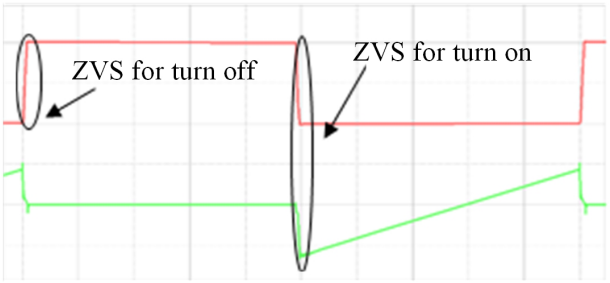

Fig.12: *The simulation results of drain current (bottom) and drain-source voltage (top) of S_1 when converter operates as buck mode (vertical scale 20 volt/div or 2A/div, time scale 1μs/div).*

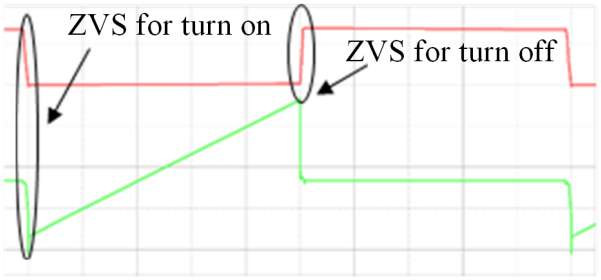

Fig.13: *The simulation results of drain current (bottom) and drain-source voltage (top) of S_1 when converter operates as boost mode (vertical scale 40 volt/div or 2A/div, time scale 1μs/div).*

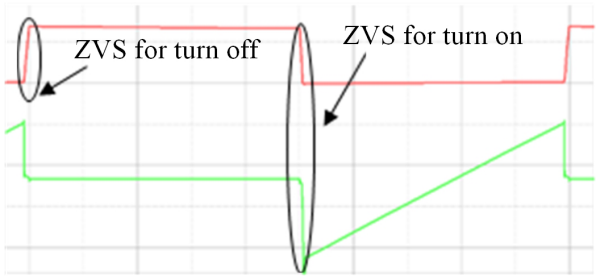

Fig.14: *The simulation results of drain current (bottom) and drain-source voltage (top) of S_2 when converter operates as boost mode (vertical scale 40 volt/div or 2A/div, time scale 1μs/div).*

From the Fig 16 it can be seen that switch current is negative when the switch turned on, that shows body diode of switch conducts and ZVS condition in this instant is provided. Also, these conditions are maintained for another switch. As seen in figures 16 and 19 there are resonance in the voltage across the switch. It seems that this resonance duo to the leakage inductance of L can be modified with better warping transformer.

Because of the resonance between the inductor with switch parasitic capacitance, there is a ringing in Fig 16 and 19 at switch voltage.

As shown in the simulation and experimental re-

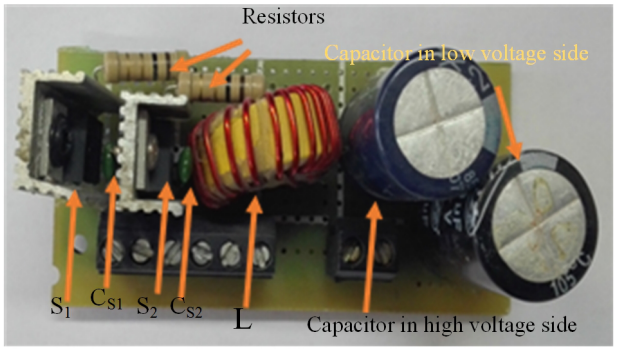

Fig.15: *The experimental prototype of circuit.*

sults, in addition to providing ZVS condition on all switches the voltage spike due to parasitic elements across the switches well absorbed that can be illustrated in Fig 17 and 18.

In Fig 15 there are two resistors, which these resistors are placed for display current waveform in oscilloscope.

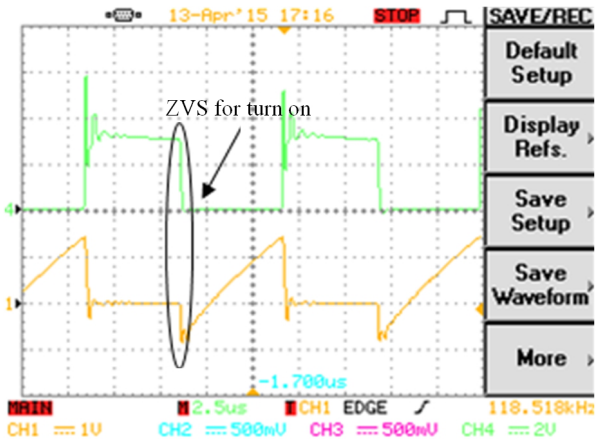

Fig.16: *The experimental drain current (bottom) and drain-source voltage (top) of S_2 in buck operation (vertical scale 20 volt/div or 2A/div, time scale 1.5μs/div).*

The circuit diagram of the proposed converter with control unit is shown in Fig 20. The dead time between S_1 and S_2 is provided with no gate in control unit. Therefore the proposed converter is controlled by just one PWM signal.

The efficiency of proposed converter and regular ones versus of various output power is shown in Fig 21. The used data in Fig 21 is obtained by simulating the proposed converter at different loads and calculating the power at the input and output.

As can be observed, the efficiency of proposed converter is higher than regular one in all output power range. These curves are obtained by PSPICE software.

The proposed converter are compared with two other ones and the results are shown in table 2. This

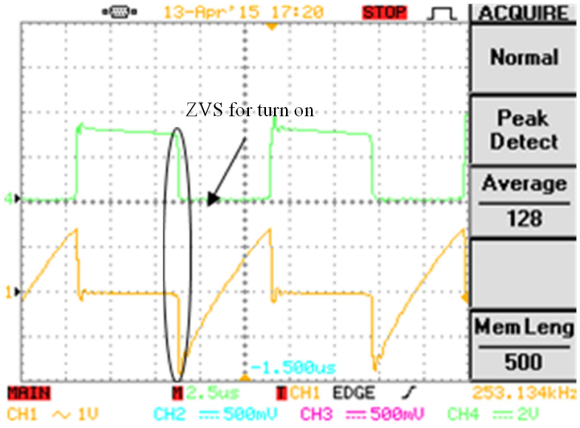

Fig.17: *The experimental drain current (bottom) and drain-source voltage (top) of S_1 in buck operation (vertical scale 20 volt/div or 2A/div, time scale 1.5μs/div).*

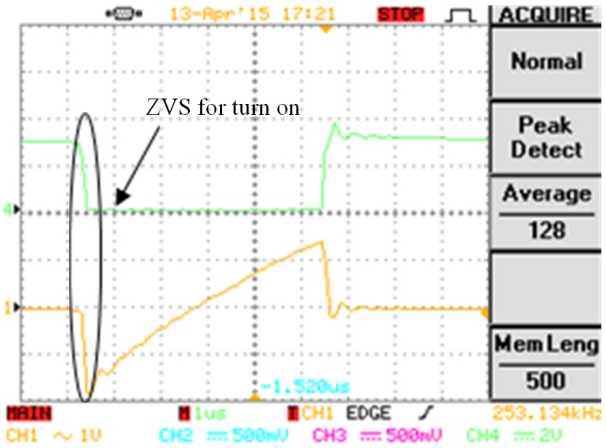

Fig.18: *The experimental drain current (bottom) and drain-source voltage (top) of S_1 in boost operation (vertical scale 20 volt/div or 2A/div, time scale 1μs/div)*

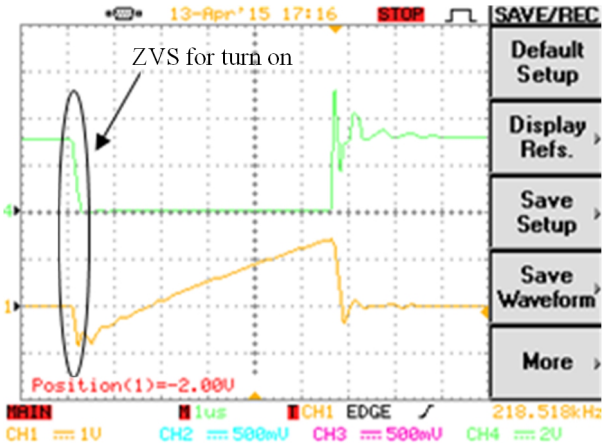

Fig.19: *The experimental drain current (bottom) and drain-source voltage (top) of S_2 in buck operation (vertical scale 20 volt/div or 2A/div, time scale 1μs/div)*

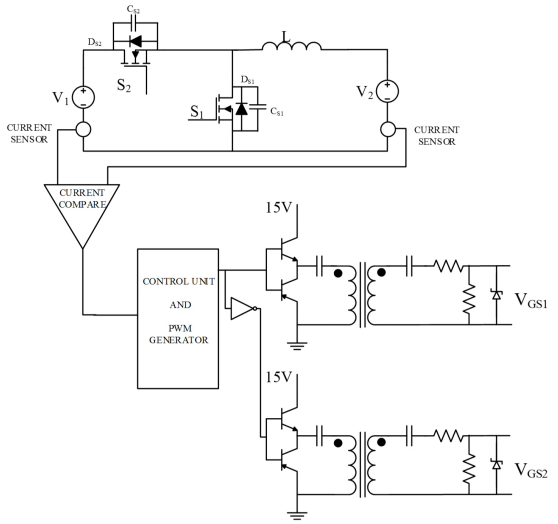

Fig.20: *Circuit diagram of proposed converter with control unit.*

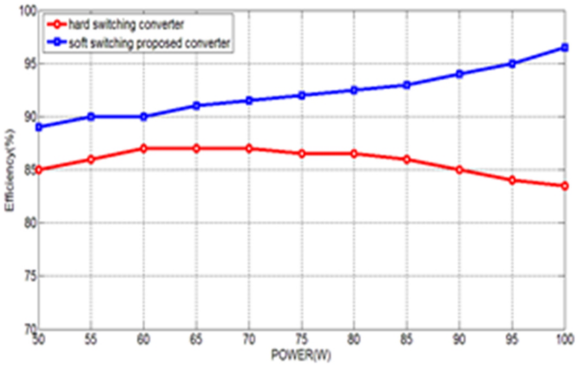

Fig.21: *Comparison of efficiency between hard-switching converters with soft-switching proposed converter.*

results are obtained by PSPICE simulation with the same output power and switching frequency. As it is observed, the converter in [12] and [13] has lower switch current stress than the proposed converter, but the proposed converter has lower number of elements including main and auxiliary circuits and therefore has higher efficiency in comparison with [12] and [13].

5. CONCLUSION

In this paper, a new ZVS bidirectional buck-boost converter is proposed. This converter is controlled by PWM signal and does not require any extra circuit to achieve soft-switching condition. In addition, by reducing value of inductance L, this element in addition to the stored energy, provides soft-switching condition for both buck and boost modes. Since the switches are gated complementary, the extra switch driver is not needed. Since reducing elements in the proposed converter, the conduction loss decreases in addition to the switching loss. Therefore the efficiency increases significantly. The proposed converter is implemented to verify theoretical analysis and its measured efficiency is 96%.

Table 2: *Comparison between proposed converter with two other ones.*

converter	Converter in[12]	Converter in[13]	Proposed converter
Output power (w)	100	100	100
Efficiency (%)	93	95	96
Switch voltage stress (V)	50	70	50
Switch current stress (A)	2	3	5
Number of switch	3	4	2
Number of auxiliary elements	4	8	0
Frequency(kHZ)	100	100	100

References

[1] A. Nasiri, Z. Nie, S. B. Bekiarov, and A. Emadi, "An on-line UPS system with power factor correction and electric isolation using BIFRED converter," *IEEE Trans. Ind. Electron*, vol. 55, No. 2, pp. 722-730, Feb. 2008.

[2] L. Wang, Z. Wang, H. Li, "Asymmetrical Duty Cycle Control and Decoupled Power Flow Design of a three-port Bidirectional DC-DC Converter for Fuel Cell Vehicle Application," *IEEE Trans. Power Electron*, vol. 27, No. 2, pp. 891-904, 2012.

[3] K. Jin, M. Yang, X. Ruan, and M. Xu, "Three-level bidirectional converter for fuelcell/battery hybrid power system," *IEEE Trans. Ind. Electron*, vol. 57, No. 6, pp. 1976-1986, Jun. 2010.

[4] B. Allaoua, A. Laoufi, B. Mebarki, "Bat Optimization for a Dual-Source Energy Management in an Electric Vehicle Energy Storage Strategy," *ECTI Trans on electrical ENG*, vol. 11, No. 2, pp. 95-100, 2013.

[5] I1. O. Lee, "A Hybrid PWM-Resonant DC-DC Converter for Electric Vehicle Battery Charger Application," *Journal of Power Electronics*, vol. 15, No. 5, pp. 1158-1167, September. 2015.

[6] Z. Amjadi, S. S. Williamson, "A novel control technique for a switched-capacitor-converter based hybrid electric vehicle energy storage system," *IEEE Trans, Ind. Electron*, vol. 57, No. 3, pp. 926-934, Mar. 2010.

[7] M. B. Camara, H. Gualous, F. Gustin, A. Berthon, and B. Dakyo, "DC/DC converter design for super capacitor and battery power management in hybrid vehicle application-Polynomial control strategy," *IEEE Trans. Ind.*

Electron, vol. 57, No. 2, pp. 587-597, February. 2010.

[8] T. LaBella, Y. Wensong, L.J. Sheng, M. Senesky and D. Anderson, "A Bidirectional-Switch-Based Wide-Input Range High-Efficiency Isolated Resonant Converter for Photovoltaic Applications," *IEEE Trans. Power Electron*, vol. 29, No. 7, pp. 3473-3484, July. 2014.

[9] Y. S. Lee, G. T. Cheng, "Quasi-Resonant Zero-Current-Switching Bidirectional Converter for Battery Equalization Applications," *IEEE Trans, Power Electron*, vol. 21, No. 51, pp. 1213-1224, 2006.

[10] G. Ma, W. Ou, G. Yu, Y. Liu, N. Liang, W. Li, "A zero-voltage switching bidirectional dc-dc converter with state analysis and soft switching-oriented design consideration, " *IEEE Trans. Ind. Electron*, vol. 56, No. 6, p. 2174-2184, June 2009.

[11] M. R. Mohammadi, H. Farzanehfard, "New Family of Zero-Voltage-Transition PWM Bidirectional Converters with Coupled Inductors," *IEEE Trans, Ind. Electron*, vol. 59, No. 2, pp. 912-919, 2012.

[12] P. Das, B. Laan, S. A. Mousavi, G. Moschopolous, "A Nonisolated Bidirectional ZVS PWM Active Clamped DC-DC Converter," *IEEE Trans. Power Electron*, vol. 24, No. 2, pp. 553-558, February 2009.

[13] J. W. Yang, H. L. Do, "Soft-Switching Bidirectional DC-DC Converter Using a Lossless Active Snubber," *IEEE Trans. Circuits and System*, vol. 61. No. 5, pp. 1588-1596, 2014.

[14] N. Mohan, T. M. Undeland, and W. P. Robbins, "Power Electronics: Converters, " *Applications and Design*, 3d ed., Wiley, New York, 2003.

Mahmood Vesali was born in Isfahan, Iran, in 1987. He received the B.S and M.S degrees in electrical engineering in 2008 and 2015 from Sepahan University and Islamic Azad University, khorasgan branch, respectively. His research interest are bidirectional DC-DC converters and soft switching DC-DC converters.

Majid Delshad was born in Isfahan, Iran, in 1979. He received the B.S and M.S degrees in electrical engineering in 2001 and 2004 from Kashan University and Isfahan University of Technology, Iran, respectively. He received the Ph.D degree also in electrical engineering in Isfahan University of Technology. He is assistant professor in Islamic Azad University, Khorasgan Branch. His research interest includes soft switching techniques in DC-DC converters and current-fed converters.