# Physical Insight of Junctionless Channel Transistor (JLCT) with Simulation Study of Relaxed SiGe on Insulator (SG-OI)

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## ABSTRACT

The article investigates towards the simulation study of junctionless transistor, exploiting channel engineering technique with ($Si_{1-x}Ge_x$) as device layer. An accurate and deep understanding of the gated resistor with a demonstration amended of lower off-state current; improve on-state drain current and transconductance with its conventional counterpart using numerical simulation. With the significance of SiGe material on Buried oxide (BOX) and Junctionless transistor (JLT) topology an improvement in electron mobility with zero electric field reduce the scattering rate across the channel. With these identifications SGOI-JLCT has a great potential for low power switching applications.


**Keywords**: Mole fraction, JLCT, $I_{ON}-I_{OFF}$, Electric field (E-Field), Silicon on Insulator (SOI).

## 1. INTRODUCTION

Over last few years, the rapid growth in MOS technology was conventionally dependent on Moore's theory and Dennard's scaling theory which later moved to Moore than Moore [1]. Due to the scaling factors the MOS transistor reached to the ultra-deep submicron technology, which reduced up to three orders of magnitude within past 20 years. The physical parameters such as $L_G$ (gate length), $T_{OX}$ (gate oxide thickness), $T_{Si}$ (substrate thickness) etc. has scaled to reach nanometer regime. The interpretation of technology scaling was initiated through ITRS [1], with a particular technology node parameter has been instructed, which help the device engineers to innovative new device architectures to follow short channel technology.

Understanding the scaled channel architecture, gate controls the total charge carriers across channel. But a part of charge carriers controlled by source/drain depletion region becomes more significant which induces short channel effects (SCEs). The major issues for SCEs are formation of sharp source/drain dopants diffusion in to the channel. Various voltage control devices with source drain regions and at zero bias gate voltage the amount of current drop across interfaces give rise to leakage currents.

Due to the constant field scaling, an approximation is accountable to reduce leakage currents. [2] [3], Young *et al.*. has reported an idea about the preferable scaled technology of MOS device and the various leakage currents are also discussed. MOSFET at nanometer regime suffers from various SCE such as drain induced barrier lowering (DIBL), subthreshold swing (SS), hot carrier effect, junction leakage, etc. Thus, to overdrive these effects device engineers gave up with different architectural proposals and resourceful materials to improve the circuit analysis through device performance. The proposed unconventional devices like SOI, partially depleted SOI, Fully depleted SOI, Multi-gate (MGFET), Gate all around (GAA-FET) were developed in 2D-3D [4]. In sub-micron regime, the formation of ultra-shallow junctions with high doping profiles becomes a challenging task for the semiconductor industry for reducing SCEs. Besides this, for the first time an unconventional MOS structure with no junctions across source/channel and channel/drain edges was proposed by [5], forming a simple gated resistor that controls the electric field along the channel with applied gate voltage and later named as the JLT [6]. This device imposes several challenges on doping profiles and the thermal budget. Interestingly JLT required no doping concentration gradients; besides this, it requires a uniform heavily doped nanowire with fully depleted when the device is OFF. This is one of the key merits that improve the SCE. [7]. In ON condition, depletion region slowly degrades with an increase in gate voltage ($V_G$) at this the band becomes flat at flat band voltage ($V_{FB}$) with a positive shift in the $V_{TH}$ from partially depleted to conduction region. The study on SOI-JLT with various investigation on the band gap narrowing, SCEs, electrostatic integrity, and scaling $I_{OFF}$ using spacers is reported by Gundapaneni *etal.*. [8]-[11].

The paper investigates towards JLMOSFET exploiting channel engineering technique with ($Si_{1-x}Ge_x$), with relaxed biaxial tensile type along SiGe film. The importance of the fully depleted SG-OI (SiGe/BOX) significantly enhances the quality of the device performance than that of the SOI counterpart [12]. The

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brief idea of the FD strained-Si devices on ultrathin SGOI substrates is discussed and stated by Mizuno et al. in [13] on non-bonded SGOI substrates. This introduces with small band gap materials ($Si_{1-x}Ge_x$OI with x = 0.25, 0.5, 0.75) with the same SOI process flow [14]. The physics behind the SiGe/BOX is to improve the electron mobility with high electric field and to reduce the scattering rate across the channel. The physical insight of relaxed SiGe is applicable for JLT, as the SiGe nanofilm is considered as the device layer, which is known to cause large changes in the gate current ($I_G$). Therefore, an application of strain enables an intrinsic relationship between the oxide and the $I_G$ [15], [16]. This improves leakage current across gate and the bulk substrate.

Along with the introduction, the rest of the paper is labeled in section II, which converses the device structure and the physics behind the device, and the activated models which are carried out for simulations. Section III describes the study of the electrostatic integrity of (Extremely thin SGOI-JLCT) ETSG-OI JLCT followed by conclusion and remarks in Section IV.

## 2. EXTREMELY THIN SILICON GERMANIUM ON INSULATOR JUNCTIONLESS CHANNEL TRANSISTOR (ETSG-OI JLCT)

The paper introduces an ETSG-OI JLCT with high $k$ spacers is shown in Fig. 1 (a), (b) with ON and OFF condition. The device utilizes the transistor on insulator technique with SiGe as a device layer. The parameters listed in Table 1 are used to scrutinize ETSG-OI JLCT. A bulk planar structure with Si as substrate $N_A$ is initiated. BOX is grown, forming a bulk planar device on an insulator. A layer of SiGe is grown epitaxial over a BOX forming a device or a transistor layer. The device layer formation is of source/drain (S/D) and channel with uniform $N_D^+$ of $10^{19}$ $cm^{-3}$. For isolation purpose at oxide/channel interface effective oxide thickness (EOT) of thickness, 1nm is used and a poly-Si p-type gate with the metal workfunction ($\phi_M$) of 5.1 eV is considered. Metal electrodes are taken as source and drain contacts in JLCT. Introducing the high $k$ $HfO_2$ spacer on either side of the gate [17], [18] which will improve the fringing electric field in OFF condition.

## 3. CONDUCTION MECHANISM OF JLT

Intentionally the JLT device is fabricated to scale SCE in DSM technology, [7]. The architecture is similar to inversion mode transistor (IMT), forming a metal oxide semiconductor. Usually, a P-type poly-Si gate and an interfacial oxide layer between the metal gate and the N-type semiconductor layer are formed. This can substantiate as heavy doping dependency ranging with $N_D^+$ $10^{19}$ - $10^{22}$ $cm^{-3}$. Gate source voltage ($V_{GS}$) = drain voltage ($V_D$) = 0 V the channel is fully depleted < threshold voltage ($V_{GS} < V_{TH}$) a $\phi_M$ semiconductor workfunction $\phi_S$ difference is achieved from gate to substrate where no conduction takes place across the channel. The carriers flow through diffusion, providing an exponential increment in current as the $V_G$ varies. If $V_{GS} = 1$ V the band becomes flat at $V_{FB}$ with a positive shift in $V_{TH}$ providing a conduction path in the semiconductor layer, where the bulk current flows through the neutral path. The shift in the $V_{TH}$ depends on the $N_D$, $T_{Si}$, EOT, and $W_{Si}$. $V_{GS}$ with zero bias and high $N_D^+$ attributes of a high electric field (E-field) at the center of the channel but not at $Si/SiO_2$ interface. As with the current flow with the positive $V_{GS}$ low E-field (above $V_{TH}$ the E-field drops to zero) is observed perpendicular to the direction of the carrier in the device layer with high mobility. A bulk conduction mechanism with E-field perpendicular to current flow is observed in JLT.

The advantage in dealing with the SiGe is, compatible with standard (silicon) Si technology. [19], [20] the compound material SiGe have 4.2% of lattice mismatch with lattice constant an (x) = 5.431 $\overset{o}{A}$ for Si and 5.658 $\overset{o}{A}$ for germanium (Ge) respectively. The change in the x value includes lattice match, lattice constant of $Si_{1-x}Ge_x$ $(5.431 + 0.20x + 0.027x^2)\overset{o}{A}$ . The device layer is $Si_{1-x}Ge_x$ the (variation in mole fraction (x) results in a change in the band gap across conduction band ($E_C$) and valance band($E_V$)) [21].

Drift-diffusion carrier transport Mobility model is considered for the simulations having high field saturation carrier densities with transverse field dependency. Inversion Accumulation layer Mobility model includes doping and transverse field dependency which in turn accounts a 2D Coulomb impurity scattering [22]. As SiGe is a compound material with mole fraction dependency, effective intrinsic density & band gap narrowing model are also included. To solve this, a self-consistent drift-diffusion Equation is used. Due to high $N_D$ across lateral direction, OldSlotboom band gap narrowing and Schottky-Read-Hall mechanism are observed [23], [24]. The model calculates the intrinsic carriers for silicon material hence it improves the carrier mobility under high field saturation. The simulations are carried out using sentaurus TCAD 2D simulator [25]. The plot in Fig.2 denotes the $I_D - V_G$ characteristics of SOI-JLCT and ETSG-OI JLCT. This observes a change in $I_{ON} - I_{OFF}$ with variation in $L_G$ (15 to 30 nm) calibrate [6]. It is clearly observed that a drastic increment in $V_{TH}$ as a variation of the $L_G$ with $N_D = 1.5e^{19}cm^{-3}$.

## 4. RESULTS AND DISCUSSION

The electric properties like energy, electric field and electrostatic integrity along lateral direction of device layer is observed for ETSG-OI JLCT with the following factors: 1) at $V_{DLIN}$ and $V_{DSAT}$ for differ-

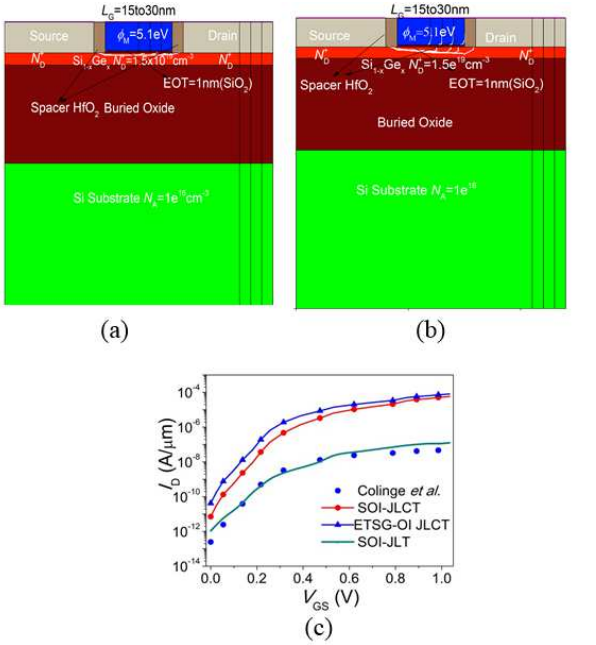


***Fig.1:*** *(a) Bird's Eye view of Extremely Thin Silicon Germanium Junctionless Channel Transistor (ETSG-OI JLCT), with channel fully depleted at $V_G$ = 0 V (b) ETSG-OI JLCT, with channel conducting at $V_G$ = 0.7 V. A depletion layer is observed beneath the oxide channel interface for different $L_G$ (c) Simulation results are in good agreement with Colinge et al.*

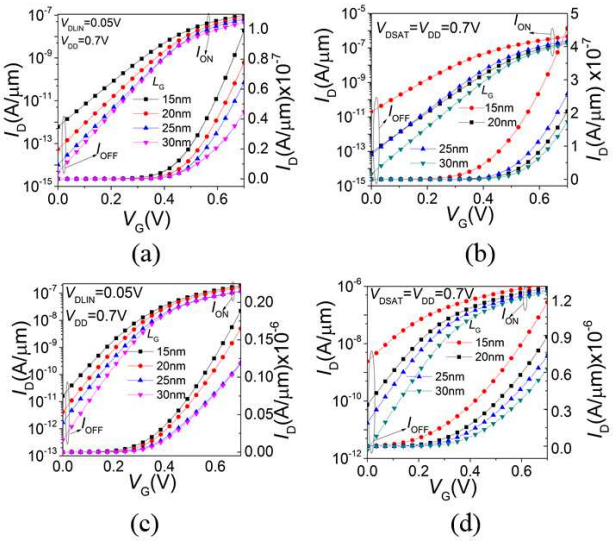


***Fig.2:*** *$I_D$ on $V_G$ for different $L_G$ (15 to 30 nm) is observed in linear and log scale for both SOI JLCT and ETSG-OI JLCT with $I_{OFF}$ and $I_{ON}$ are also given. (a) (b), shows the $I_{DLIN}, I_{DSAT}$ of SOI JLCT with Si on insulator. (c) (d), shows the $I_{DLIN}, I_{DSAT}$ of ETSG-OI JLCT with SiGe on insulator. For both the cases the graphs are drawn at $V_{DLIN}$ = 0.05 V, $V_{DSAT}$ = 0.7 V and $N_D = 1.5e^{19}cm^{-3}$.*

***Table 1:*** *Parameter Used for Simulation [8], [11]*

| **Parameters** | **ETSG-OI JLCT** | **SOI JLCT** |
|---|---|---|
| Device layer ($T_{Si}$) | 5 nm | 5 nm |
| Donor doping ($N_D$) | $1.5e^{19}$ $cm^{-3}$ | $1.5e^{19}$ $cm^{-3}$ |
| EOT of gate dielectric ($T_{OX}$) | 1 nm | 1 nm |
| Gate work-function ($\phi_M$) | 5.1 eV | 5.1 eV |
| Drain Supply Voltage ($V_{DD}$) | 0.05 V, 0.7 V | 0.05 V, 0.7 V |
| Channel length ($L_G$) | 15-30 nm | 15-30 nm |
| Energy gap ($E_G$) | 0.6 -1.1 eV | 1.1 eV |

ent $L_G$ , 2) high doping concentration $N_D$ and high $\phi_M$, 3) change in mole fraction values (x = 0.25, 0.5, 0.75) for SiGe channel. The change in "x" represents the variation in energy band diagram, electric field, and the surface potential is shown with fixed $L_G$ = 20 nm.

Fig. 3 (a, b) also shows the $I_D - V_G$ variation with x = 0.25, at which Si content in $Si_{1-x}Ge_x$ is high and signifying the Si material properties. It is observed that $V_{TH}$ value is approximately equal to both the device as considering an $N_D = 1.3e^{19}cm^{-3}to1.5e^{19}cm^{-3}$ and the use of high $k$ spacers is to improve the $I_{OFF}$. With the heavy doping and high $\phi_M$, the device shows better improvement in $V_{TH}$, $I_{ON}$ and $I_{OFF}$ is observed for ETSG-OI JLCT.

The energy band diagram of ETSG-OI JLCT is shown in Fig. 3(c) along the lateral direction (S/D and channel). As the thickness of the device layer is extremely thin about ($T_{Si}$ = 5 nm) the structure with the ultrathin channel is reported in [26]. The cut line is taken at 2.5 nm along X-axis with different "x" values, an energy band is calculated. In Fig. 3 (c) the channel SiGe, the band gap ($E_G$) varies from 1.1 eV to 0.6 eV. In SOI JLCT structure the channel is Si and $E_G$ = 1.1 eV. Therefore the difference between $E_C$ and $E_V$ is 1.1 eV. But in ETSG-OI JLCT as the value of "x" changes, a vast variation between $E_C$ and $E_V$ is observed. The architecture induces channel engineering technique in device layer through SiGe which forms a single crystal. In addition to this, the device layer induces the properties of both Si and Ge this can achieve through the molefraction variation. At x = 0.25 the $E_G$ = 0.8 eV, as it is 0.8 eV the content of Si is great in SiGe. Else if x = 0.75 EG = 0.6 eV this represents the content of Ge is high in SiGe. Hence it follows the band gap value of Ge. Therefore the channel imposes the properties of Si and also the advance merits of Ge material.

Another key factor is the Fermi energy ($E_{FN}$, $E_{FP}$) for conduction and valence band. As the cut

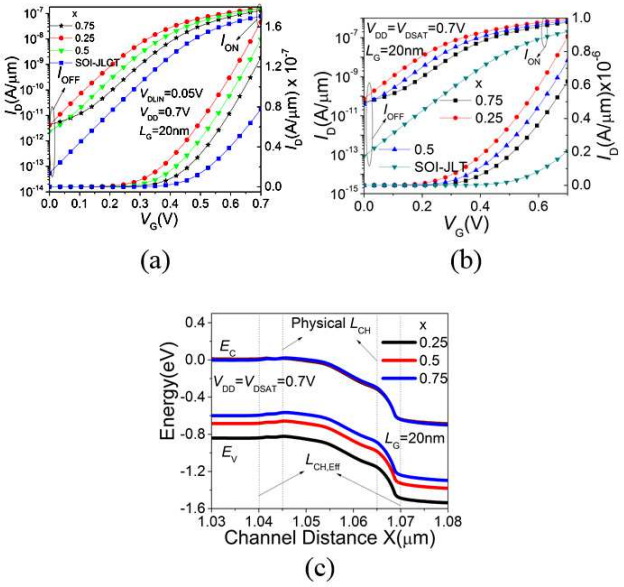


***Fig.3:*** *(a, b), $I_D - V_G$ for different value of x at $V_{DS}$ = 0.05 V and $V_{DS}$ = 0.7 V, the effect of $I_D - V_G$ (x = 0.25, 0.5, 0.75) of ETSG-OI JLCT and SOI JLCT at $L_G$ = 20 nm and $N_D = 1.5e^{19}cm^{-3}$. Fig. 3(c), Energy with respect to Distance "X" along the channel for ETSG-OI JLCT is shown. For $Si_{1-x}Ge_x$ channel (x = 0.25, 0.5, 0.75), high κ spacer $HfO_2$, $V_{DSAT}$ = 0.7 V and $T_{Si}$ = 5 nm is given.*

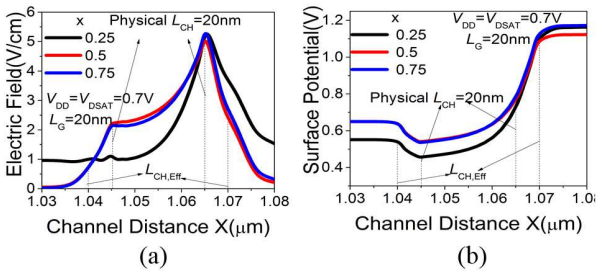


***Fig.4:*** *Electric Field with respect to Distance "X" along the channel for ETSG-OI JLCT is shown. For $Si_{1-x}Ge_x$ channel (x = 0.25, 0.5, 0.75), high κ spacer $HfO_2$, at $V_{DSAT}$ = 0.7 V and $T_{Si}$ = 5 nm is given. Fig. 4 (b), shows the effect of Surface potential (x = 0.25, 0.5, 0.75) of ETSG-OI JLCT at $V_{DSAT}$ = 0.7 V, $T_{Si}$ = 5 nm, $L_G$ = 20 nm and $N_D = 1.5e^{19}$ $cm^{-3}$.*

line is taken across the device layer (S/D channel) with high $N^+$ type doping, the $E_{FP}$ is zero and $E_{FN}$ are nearly close to the $E_C$.

Usually, at nanometer regime, it has been demonstrated that [3] the surface potential will no longer be symmetrical due to the higher channel potential. Minima of the potential parabola is shifted to the source side instead of being near to the mid of the channel. Therefore the scaling channel length affects the shift in the minima of the potential and also change in the $V_{TH}$ is identified. It is observed that the bulk potential in JLT increases abruptly from source to drain, but there is an enhancement in the electric field. Interestingly, as the effect of strain induces (x = 0.25, 0.5, 0.75) a constant E field is maintained which is shown in Fig. 4 (a).

The surface potential along the channel length is depicted in Fig. 4 (b). In IMT devices, at the nanoscale regime the channel with heavily doped and with positive $V_G$ the surface of the channel turn to be inverted and result in high E field. Due to this a sharp linear band bending across oxide/channel interface, which is attributed to induced electrons in the channel. In JLT bulk potential approximation is detected, as the high doping dependence generates a high electric field at $V_G$ = 0 V. Further with an increase in the positive $V_G$ low E-field is estimated at the midpoint of the channel given in Fig. 4 (a). In IMT E field is in the direction of current flow which gives a surface conduction mechanism, in JLT E-field is perpendicular to the current flow and a bulk conduction mechanism is observe at the center of the device [27]

Transconductance ($g_m$) as a function of $I_D$, for SOI JLCT and ETSG-OI JLCT for different $L_G$, is shown in Fig. 5 (a, b). It is observed that for different value of $L_G$ as the channel length decreases the $g_m$ value increases which results in high drain current. The device is operated at saturation current $V_{DSAT}$ = 0.7 V. The mobility degradation at high electric field reduces $g_m$ [28].

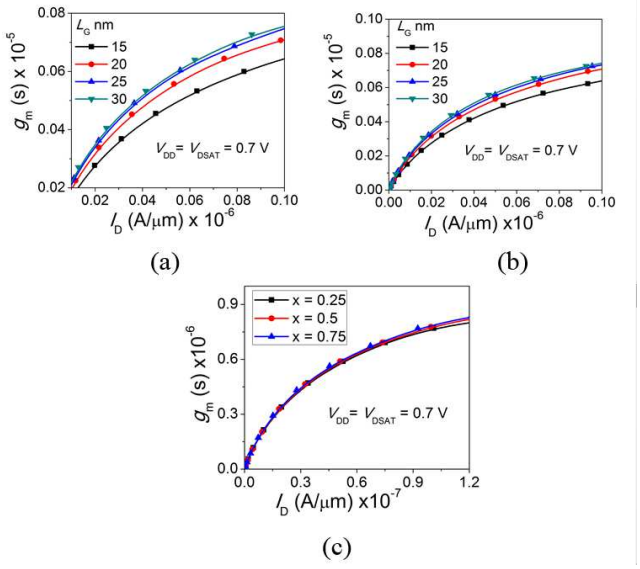


***Fig.5:*** *(a) $g_m$ with respect to $I_D$ is shown for SOI JLCT $\phi_M$ = 5.1 eV (b) ETSG-OI JLCT (c) ETSG-OI JLCT for different x values. $L_G$ = 15 to 30 nm, $T_{Si}$ = 5 nm, $N_D = 1e^{19}cm^{-3}$, $V_{DD} = V_{DSAT}$ = 0.7 V and $\phi_M$ = 5.1 eV (b) and 5. (c) $g_m$ as a function of $I_D$ for ETSG-OI JLCT with x variation factor is shown. .*

The high $g_m$ will further enhance the transconduc-

tance generation factor (TGF = $g_m/I_D$) which is the requirement for the realization of circuits operating at low supply voltage. Table II and III shows the calculated values for $I_{ON}, I_{OFF}$, leakage power and power dissipation at $V_{DLIN}$ = 0.05 V and $V_{DSAT}$ = 0.7 V. The product of $I_{OFF}$ and $V_{DLIN}$ $V_{DSAT}$ is used to calculate leakage power. For power dissipation, the product of $I_{ON}$ and $V_{DLIN}$ $V_{DSAT}$ is evaluated.

***Table 2:*** *Computed results at $V_{DLIN}$ = 0.05 V*

| $L_G$ nm | $I_{ON}$ $(A/\mu m)$ | $I_{OFF}$ $(A/\mu m)$ | Leakage Power (Watts) | Power Dissipation (Watts) |
|---|---|---|---|---|
| 15 | 1.89E-07 | 1.64E-11 | 8.2E-13 | 9.45E-09 |
| 20 | 1.65E-07 | 4.13E-12 | 2.07E-13 | 8.25E-09 |
| 25 | 1.19E-07 | 1.70E-12 | 8.5E-14 | 5.95E-09 |
| 30 | 1.18E-07 | 3.84E-13 | 1.92E-14 | 5.9E-09 |

***Table 3:*** *Computed results at $V_{DSAT}$ = 0.7 V*

| $L_G$ nm | $I_{ON}$ $(A/\mu m)$ | $I_{OFF}$ $(A/\mu m)$ | Leakage Power (Watts) | Power Dissipation (Watts) |
|---|---|---|---|---|
| 15 | 1.17E-06 | 2.41E-09 | 1.687E-09 | 8.19E-07 |
| 20 | 8.88E-07 | 7.52E-11 | 5.264E-11 | 6.22E-07 |
| 25 | 7.31E-07 | 1.73E-11 | 1.211E-11 | 5.12E-07 |
| 30 | 6.26E-07 | 1.94E-12 | 1.358E-12 | 4.38E-07 |

## 5. CONCLUSION

The paper investigate with the various topologies like (a) JLT topology, (b) SOI topology, (c) channel engineering technique using SiGe material, (d) Extremely thin SiGe film (nanoscale film) with relaxed SiGe etc. to improve the device performance. In order to identify the improvements a comparative analysis on $I_{ON}, I_{OFF}$, and $g_m$ for SOI JLCT and ETSG-OI JLCT is shown for different $L_G$ at $V_{DLIN}$ = 0.05 V, $V_{DSAT}$ = 0.7 V. Apart from this the band gap approximation, surface potential, and E field with x variation for ETSG-OI JLCT is observe using channel engineering technique. Over all the results gives a good agreement with the enhancement of device properties using both Si and Ge material

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