

Analytical Approach and Simulation of GaN Single Gate TFET and Gate All around TFET

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ABSTRACT

In this work, we investigate the impact of Gallium Nitride (GaN) based Single Gate Tunnel field effect transistors (SG TFET) and Gate All Around (GAA) TFET by using analytical models. The models are derived by solving the 2D-Poisson's equation and Parabolic Approximation Technique. The analytical model includes the calculation of the surface potential, lateral electric field and vertical electric field. Finally the drain current is extracted by using Kane's model. The device simulations are carried out using 2-D device simulator, Technology Computer Aided Design (TCAD). The model can be used to study the impact of GaN based SG TFET and GAA TFET in terms of higher ON current characteristics. The results expected by the model are compared with those obtained by 2-D simulation to verify the accuracy of the proposed analytical model.

Keywords: Single Gate Tunnel Field Effect Transistor, Gate All around (GAA) TFET, 2D-Poisson's equation, Kane's model, TCAD.

1. INTRODUCTION

Silicon CMOS has been the technology of choice of the micro and nano-electronics industry for the past four decades. In this regard, Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) have become the fundamental building blocks of Very Large Scale Integrated circuits (VLSI) due to their excellent properties. The demand for higher integration density, low power consumption, high speed and low cost requires aggressive scaling of the MOSFETs. While scaling the device, the key factors that limit the performance of MOS devices are increased short channel effects (SCE) and very high leakage current.

In the recent years, Tunnel field effect transistors has been proposed to overcome the short channel effects and reduced leakage current (femto Amps). Apart from merits, TFETs suffer from a low ON-current (ION). Therefore various techniques to improve the ION in the TFET has been reported [1-6].

In our previous work, we have presented Dual Material Gate (DMG) TEFT [7], Dual Material Gate TFET [8] and Surrounding Gate TFET [9] in order to improve the ON current characteristics. Eng-Hua [10] proposed germanium TFETs are studied for high performance and low power logic applications using two dimensional device simulations. It has been proved that Ge based TFET could achieve higher ION than Silicon TFET. However in the above structures, the ION current still need to be improved.

This paper deliberates the two promising new directions for tunneling junction formation that alter the ION and IOFF leakage characteristics of the GaN TFETs. GaN based devices have a superior relationship between on-resistance and breakdown voltage due to their higher critical electric field strength. This allows devices to be smaller and the electrical terminals closer together for a given breakdown voltage requirement.

Compared to silicon and Germanium based devices, GaN chips operate at higher voltages, frequencies and temperatures, helping to eliminate up to 90% of the power losses in electricity conversion. Wide bandgap refers to higher voltage electronic band gaps in devices, which are larger than 1 electronvolt (eV). GaN devices are currently fabricated on different substrate materials, such as GaN on silicon (Si) and GaN on silicon carbide (SiC) wafers, with some debate about which process offers the best performance.

2. MODEL DERIVATION FOR GAN SINGLE GATE TFET

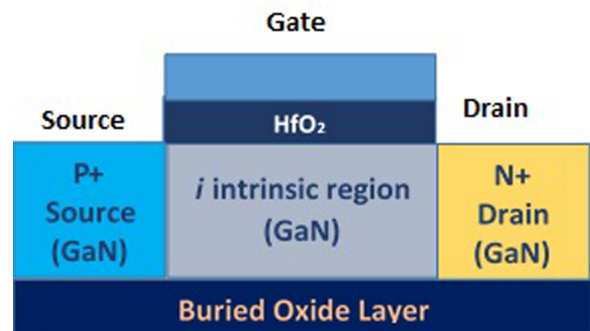


Fig.1: Schematic diagram of Single Gate GaN TFET.

The cross sectional view of a GaN SG TFET is

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shown in Fig. 1. The source and drain are highly doped p-type and n-type regions respectively. The intermediate channel region comprises a moderately doped p-type layer. GaN can be doped with silicon (Si) or with oxygen[12] to n-type and with Magnesium [11] to p-type. The high-k material Hafnium oxide (HfO₂) is used as the gate dielectric and the gate metal electrode work function is 4.05eV. The device parameters are listed in Table 1. On the operation of TFET, when the positive gate voltage V_{GS}=1V is applied, the bands in the intrinsic region are move downwards and the tunneling barrier is formed between the p+ source region and lightly doped p type channel region. This reduced tunneling barrier width and the electric field near the tunneling junction will tunnel the electrons from the valance band of the source to the conduction band of the channel region. These generated electrons are transported to the drain through drift diffusion and gives the ION current

Table 1: The values of parameters used in simulations

Quantities	Symbol	value
Doping of source	N_A	10^{20}cm^{-3}
Doping of drain	N_D	10^{20}cm^{-3}
Metal work function	ϕ_m	4.05eV
Oxide thickness	t_{OX}	2nm
GaN body thickness	R	20nm
Channel length	L	45 nm

2.1 Surface potential

The potential distribution in the gate oxide region is distinguished by two dimensional Poisson's equation.

$$\frac{\partial^2 \varphi(x, y)}{\partial x^2} + \frac{\partial^2 \varphi(x, y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{GaN}} \quad (1)$$

Where q is the electronic charge, ε_{GaN} is the GaN permittivity.

The potential profile in the vertical direction is assumed to be a second-order polynomial, i.e.,

$$\varphi(x, y) = c_0(x) + c_1(x)y + c_2(x)y^2 \quad (2)$$

Here $C_0(x)$, $C_1(x)$ and $C_2(x)$ are arbitrary constants. The Poisson's equation is solved using the following boundary conditions.

(a) Electric flux at the gate-oxide interface is continuous. Therefore

$$\frac{d\varphi(x, y)}{dy} = \frac{\varepsilon_{ox}}{\varepsilon_{GaN}} \frac{\varphi_s(x) - \psi_g}{t_{ox}} \text{aty} = 0 \quad (3)$$

(b) Electric flux at the back gate-oxide and the back channel interface is continuous. Therefore

$$\frac{d\varphi(x, y)}{dy} = 0 \text{aty} = t_{GaN} \quad (4)$$

(c) The potential at the source end is

$$\varphi(0, 0) = \varphi_s(0) = V_{bi} \quad (5)$$

(d) The Potential at the drain end is

$$\varphi(L, 0) = \varphi_s(L) = V_{bi} + V_{DS} \quad (6)$$

Where, $\psi_g = V_{GS} - \phi_m + \chi + \frac{E_G}{2}$

EG is the energy gap. χ is electron affinity of GaN, ϕ_m is Gate metal work function, V_{GS} is Gate to source voltage. V_{DS} is Drain to source voltage. V_{bi} is the built in potential. t_{GaN} is the Gallium Nitride body thickness and t_{ox} is the oxide thickness.

The constants $C_0(x)$, $C_1(x)$ and $C_2(x)$ in equations (2) can be obtained from the boundary conditions (3) and (4) as described.

$$\begin{aligned} c_0(x) &= \varphi_s(x) \\ c_1(x) &= \frac{\varphi_s(x) - \psi_g}{t_{ox}} \frac{\varepsilon_{ox}}{\varepsilon_{GaN}} \\ c_2(x) &= \frac{1}{2t_s} \frac{\varepsilon_{ox}}{\varepsilon_{GaN}} \frac{\psi_g - \varphi_s(x)}{t_{GaN}} \end{aligned} \quad (7)$$

Substituting the values of $C_0(x)$, $C_1(x)$ and $C_2(x)$ in equation (2) and using $\phi(x, y)$ in equation (1) we obtain the potential distribution as

$$\varphi_s(x) = Ae^{\lambda x} + Be^{-\lambda x} + \psi_g \quad (8)$$

Where, $\lambda = \sqrt{\frac{\varepsilon_{ox}}{\varepsilon_{GaN} t_{ox} t_{GaN}}}$ The coefficients A and B are now expressed as,

$$\begin{aligned} A &= \frac{-1}{2\sinh(\lambda L)} [V_{bi} \exp(-\lambda L) - (V_{bi} + V_{DS}) \\ &\quad + \psi_g(1 - \exp(-\lambda L)) + V_{DS}] \\ B &= \frac{1}{2\sinh(\lambda L)} [V_{bi} \exp(\lambda L) - (V_{bi} + V_{DS}) \\ &\quad + \psi_g(1 - \exp(\lambda L)) - V_{DS}] \end{aligned}$$

2.2 Electric field

The electric-field distribution along the channel length can be obtained by differentiating the surface potential. The electric field along the channel E_x can be written as

$$E_x = -\frac{d\varphi_s(x)}{dx} = -(A\lambda \exp(\lambda x) - B\lambda \exp(\lambda x)) \quad (9)$$

The electric field in the vertical direction E_y can be written as

$$E_y = -\frac{d\varphi_s(x)}{dy} = -[C_1(x) + 2yC_2(x)] \quad (10)$$

2.3 Drain Current

Finally, I_{DS} of TFETs can be calculated by integration band to-band tunneling (BBT) generation rate (G) over the channel region.

$$I_d = q \int G dx dy \quad (11)$$

For the calculation of Generation rate (G), Kane's Model has been employed [13] [14],

$$G(E) = A \frac{|E|^2}{\sqrt{E_G}} \exp[-B \frac{E_g^{3/2}}{|E|}] \quad (12)$$

Where, $|E|$ is the magnitude of the electric field which is defined as $|E| = \sqrt{E_x^2 + E_y^2}$ and E_G is the energy band gap. The Parameters used for TCAD simulation are $A=2.42 \times 10^{21} \text{eV}^{1/2}/\text{cm.s.V}^2$ and $B=15.7 \times 10^6 \text{V/cm} \cdot (\text{eV})^{3/2}$.

3. RESULTS OF GAN SINGLE GATE TFET

To verify the accuracy of the analytical model, two-dimensional device simulation has been performed using TCAD Sentaurus. The model is tested on a TFET with a channel length of 45 nm, with different gate biasing. The variation of surface potential along the channel length L in the device for different applied gate voltages is illustrated in Figure 2. The potential remains constant in the middle of the GaN area while it varies across the source and drain junctions when the bias voltage $V_{GS} = 0$. The potential variation is restricted to a small area near the tunneling junction as the biasing voltage is increased gradually. The reason for the potential being constant in the intrinsic region is attributed to the gates, and this forms the basic difference between the TFET and the p-i-n junction, with a constant electric field E between the p-source and n-drain illustrated in Fig 2. Analytical results are in excellent agreement with TCAD results.

Fig. 3 shows that calculated and simulated values of lateral electric field E_X and Vertical Electric field E_Y with channel length $L_{CH}=45\text{nm}$ of the SG TFET structure based on Equation (9) and (10). Lateral electric field is mainly contributed by the Drain to Source bias of the device. As the source-drain bias became more prominent and causes a raise in lateral electric field, it decreases the gate control over the channel. When gate voltage is varied, the lateral electric field remains constant at the channel region. It is clearly seen from the figure that the lateral electric field is less dominant on this device structure. Vertical electric field E_Y is mainly contributed by the gate to source voltage of the device. As the voltage applied to the gate increases, the high vertical electric field would be induced at the source to channel junction. Hence maximum vertical electric field is always present at the tunneling junction, this

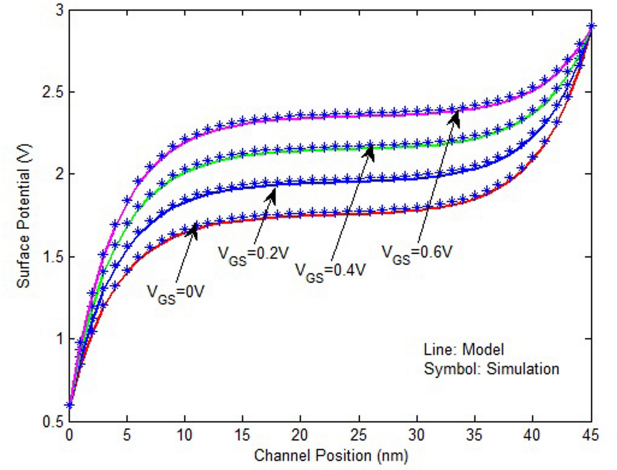


Fig. 2: Surface potential profiles with variations of V_{GS} at $V_{DS} = 0.5 \text{ V}$.

leads to reduced tunneling barrier width between the source region and intrinsic channel. Therefore, the reduced tunneling barrier width yields higher ION current performance. It can be seen that the Lateral electric field and vertical electric field distribution are in good agreement with simulation results.

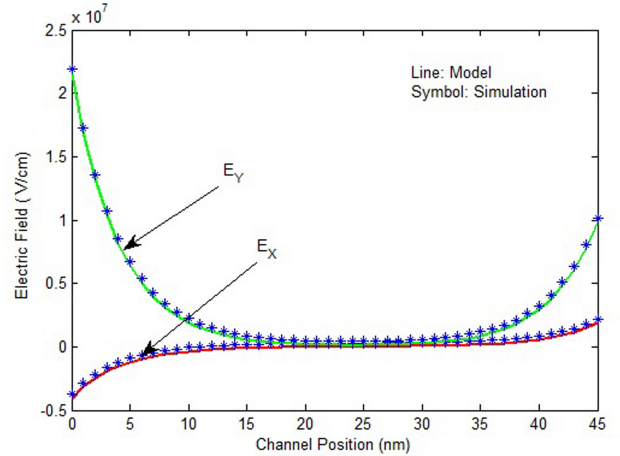


Fig. 3: Lateral Electric field (E_X) and Vertical electric field (E_Y) of SG-TFET for Channel length $L=45\text{nm}$ and $V_{DS}=0.5 \text{ V}$.

Fig. 4 shows the modeled and simulated values of I_{DS} - V_{GS} characteristics of Single Gate TFET with drain voltages (V_{DS}) 0.3V and 0.5V based on Equation (11). For the positive values of V_{GS} , electrons tunnel from valence band in p+ source region to conduction band in channel region and the tunneling current gets increased. In this condition, the device behaves as an n type single gate TFET. Analytical results are in excellent agreement with simulation results.

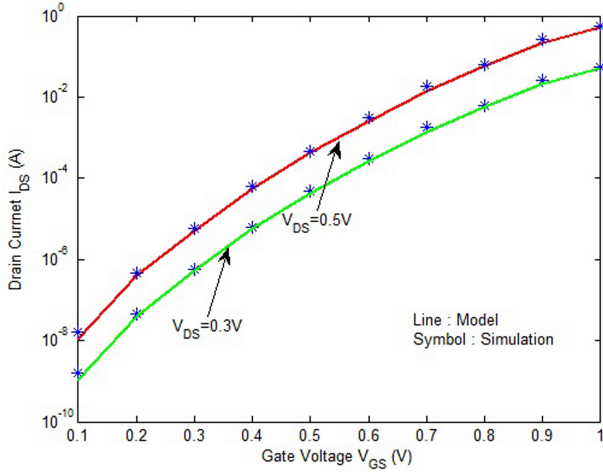


Fig.4: I_{DS} - V_{GS} Characteristics of SG TFET for channel length $L=45\text{nm}$ with $V_{DS}=0.3\text{V}$ and 0.5V .

4. MODEL DERIVATION FOR GAN GATE ALL AROUND TFET

The cross section view of a Gate all around TFET is shown in Figure 4. The coordinate system consists of a radial direction r , a vertical direction z , and an angular component θ in the plane of the radial direction. The source and drain is made of highly doped p-type and n-type regions respectively. The intermediate channel region is made of a moderately doped n-type layer. HfO_2 is used as the gate dielectric.

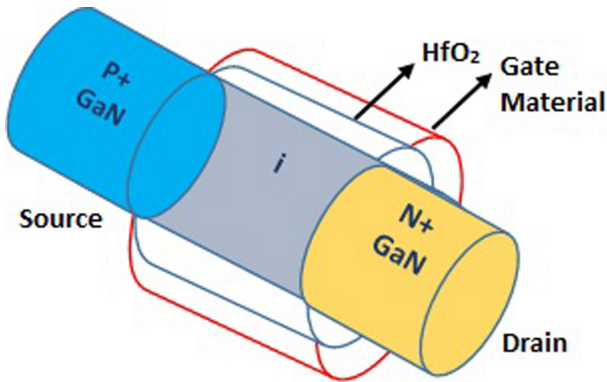


Fig.5: Schematic diagram of GAA-TFET.

For the simplicity of derivation, it has been assumed that the TFET is operated in the subthreshold region where mobile carriers are negligible and that source-channel and drain-channel junctions are abrupt. No depletion in the source and drain region has been assumed. To obtain potential distribution throughout the device and the channel potential at the HfO_2 -GaN interface, the 2-D Poisson's/Laplace Equation used is given as:

$$\frac{1}{r} \frac{\partial}{\partial r} \left(r \frac{\partial \varphi(r, z)}{\partial r} \right) + \frac{\partial^2 \varphi(r, z)}{\partial z^2} = \frac{qN_A}{\epsilon_{GaN}} \quad (13)$$

To solve the 2-D Poisson's Equation for n channel surrounding gate TFET, the parabolic approximation approach is employed. The parabolic approach is applied to estimate the potential distribution over the 2-D space (along the device length and device depth) and the potential solution is given as:

$$\varphi(r, z) = C_0(z) + C_1(z)r + C_2(z)r^2 \quad (14)$$

Where the arbitrary constants $C_0(z)$, $C_1(z)$ and $C_2(z)$ are functions of z only.

The boundary conditions required for the solution of Equation (13) are,

(a) The surface potential $\phi_s(z)$ is a function of z only.

$$\varphi(R, z) = s_1(z) = \varphi_s(z) \quad (15)$$

(b) The electric field in the center of the GaN pillar is zero.

$$\left. \frac{\partial \varphi(r, z)}{\partial r} \right|_{r=0} = 0 \quad (16)$$

(c) The electric field at the GaN / HfO_2 interface is continuous.

$$\left. \frac{\partial \varphi(r, z)}{\partial r} \right|_{r=R} = \frac{\epsilon_{ox}}{\epsilon_{si}R} \left(\frac{\psi_G - \varphi_s(z)}{\ln(1 + \frac{t_{ox}}{R})} \right) \quad (17)$$

Here $C_f = R \ln(1 + \frac{t_{ox}}{R})$

(d) The potential at the source end is

$$\varphi(0, 0) = \varphi_s(0) = V_{bi} \quad (18)$$

(e) The potential at the drain end is

$$\varphi(r, L) = \varphi_s(L) = V_{bi} + V_{ds} \quad (19)$$

Where V_{bi} is the built in potential. $V_{bi} = \frac{KT}{q} \ln \left(\frac{N_A N_D}{n_i} \right)$

E_G is Band gap energy, q is elementary charge, V_{GS} is Gate to Source voltage, V_{DS} is Drain to Source voltage, ϵ_{GaN} is relative permittivity of Gallium Nitride and ϵ_{ox} is relative permittivity of hafnium oxide.

Applying all the boundary conditions to equation (14), the coefficients $C_0(z)$, $C_1(z)$ and $C_2(z)$ can be rewritten as functions of surface potential $\varphi_s(z)$, i.e.,

$$\begin{aligned} C_0(z) &= \varphi_s(z) - \frac{R}{2} \frac{C_f}{\epsilon_{si}} (\psi_G - \varphi_s(z)) \\ C_1(z) &= 0 \\ C_2(z) &= \frac{1}{2R} \frac{C_f}{\epsilon_{si}} (\psi_G - \varphi_s(z)) \end{aligned} \quad (20)$$

Substituting the equation (20) in (14), we get

$$\varphi(r, z) = \varphi_s(z) - \frac{R}{2} \frac{C_f}{\epsilon_{si}} (\psi_G - \varphi_s(z)) + \frac{1}{2R} \frac{C_f}{\epsilon_{si}} (\psi_G - \varphi_s(z)) r^2 \quad (21)$$

The surface Potential $\varphi_s(z)$ can be obtained by solving the Poisson's equation (13) using (21).

$$\frac{d^2 \varphi_s(z)}{dz^2} - K^2 \varphi_s(z) = -K^2 \psi_G \quad (22)$$

Where, $K^2 = \frac{2C_f}{R\epsilon_{si}}$
 $\psi_G = V_{GS} - \varphi_m + \chi + \frac{E_g}{2}$

By solving the second-order differential equations (22), we get,

$$\varphi_s(z) = Ae^{Kz} + Be^{-Kz} + \psi_G \quad (23)$$

χ is the electron affinity. λ is the characteristics length. This natural length is an easy guide for choosing device parameters.

The coefficients of A and B can be expressed as,

$$A = V_{bi} - \psi_G - \frac{\left\{ e^{LK} V_{biS} - (V_{biD} + V_{DS}) \right\} - \left\{ e^{LK/2} \psi_G (2j \sinh(\frac{LK}{2})) \right\}}{2j \sinh(LK)}$$

$$B = \frac{\left\{ e^{LK} V_{biS} - (V_{biD} + V_{DS}) \right\} - \left\{ e^{LK/2} \psi_G (2j \sinh(\frac{LK}{2})) \right\}}{2j \sinh(LK)}$$

4.1 Electric Field

The electric-field distribution along the channel length can be obtained by differentiating the surface potential. The lateral electric field can be written as,

$$E_z = -\frac{\partial \varphi(r, z)}{\partial z} = \frac{\partial \varphi_s(z)}{\partial z} = K (Ae^{Kz} - Be^{-Kz}) \quad (24)$$

The vertical electric field can be written as,

$$E_r = \frac{\partial \varphi(r, z)}{\partial r} = 2C_2(z)r \quad (25)$$

4.2 Drain Current

The flow of current I_{DS} in a surrounding gate TFET is based on Band-to-Band Tunneling (BTBT) of electrons from the valance band of the source to the conduction band of the channel region. The tunneling generation rate (G) can be calculated using Kane's model [13],[14]. The total drain current is then computed by integrating the band to band generation rate over the volume of the device.

$$I_{DS} = q\pi r^2 \iint G(r, z) dr dz \quad (26)$$

For the calculation of tunneling Generation rate (G), Kane's Model has been employed [13], [14]

$$G(E) = A_{kane} \frac{|E|^2}{\sqrt{E_g}} e^{\left[-B_{kane} \frac{E_g^{3/2}}{|E|} \right]} \quad (27)$$

$$A_{kane} = \frac{q^2 \sqrt{2m_{tunnel}}}{h^2 \sqrt{E_g}}$$

$$B_{kane} = \frac{\pi^2 E_g^{3/2} \sqrt{m_{tunnel}/2}}{qh}$$

$$\frac{1}{m_{tunnel}} = \frac{1}{m_h m_0} + \frac{1}{m_e m_0}$$

Where, $|E|$ is the magnitude of the electric field which is defined as $|E| = \sqrt{E_r^2 + E_z^2}$ and E_g is the energy band gap. m_0 is the rest mass of an electron, m_e and m_h are the electron and hole effective masses respectively.

5. RESULTS OF GAN GAA-TFET

Fig. 6 shows the calculated surface potential profile for different gate voltage of Gate All Around TFET structure along with the simulated potential profile, which is analytically obtained by Equation (23). As the gate voltage increases, the potential in the lightly doped region increases. The analytical results have been compared with the TCAD simulated results and a good agreement is achieved.

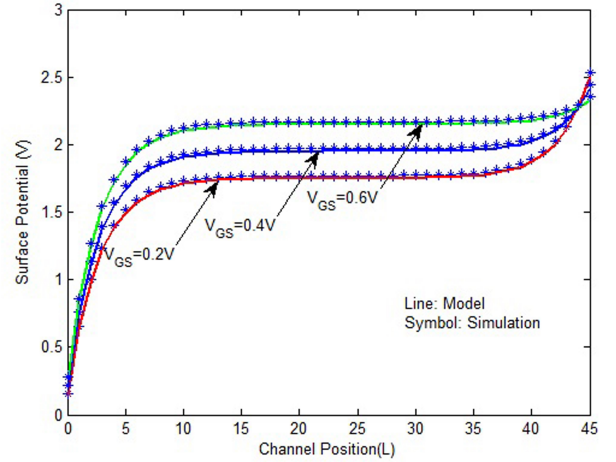


Fig. 6: Surface potential profiles of GaN based GAA-TFET for Channel Length $L=45\text{nm}$ and $V_{DS}=0.1\text{V}$ with different gate biases.

Fig. 7 shows the calculated and simulated values of vertical electric field distribution along the channel length, which is analytically obtained by Equation (24) and (25). It is evident from the figure that the peak of the vertical electric field appears near the source side. This leads to increase in tunneling generation rate. Due to this effect, the tunneling current gets increased. From the results, it is clearly understood that the calculated values of the analytical model tracks the simulated values very well.

Fig. 8 shows the I_{DS} - V_{GS} characteristics of GaN based SG TFETs. The work function of the gate

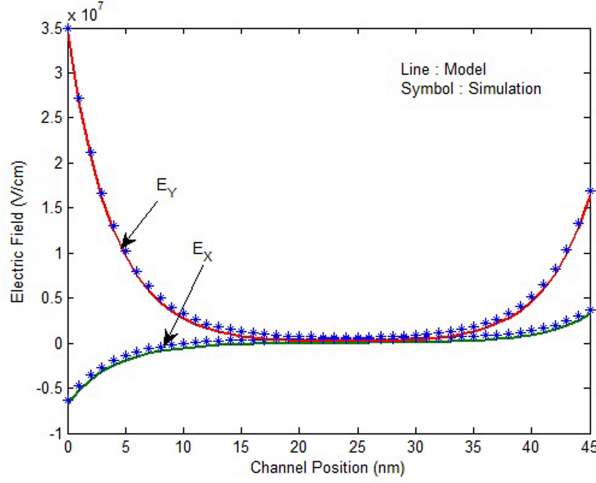


Fig.7: Lateral Electric field (E_X) and Vertical electric field (E_Y) of GAA-TFET for Channel length $L=45\text{nm}$ and $V_{DS}=0.5\text{V}$.

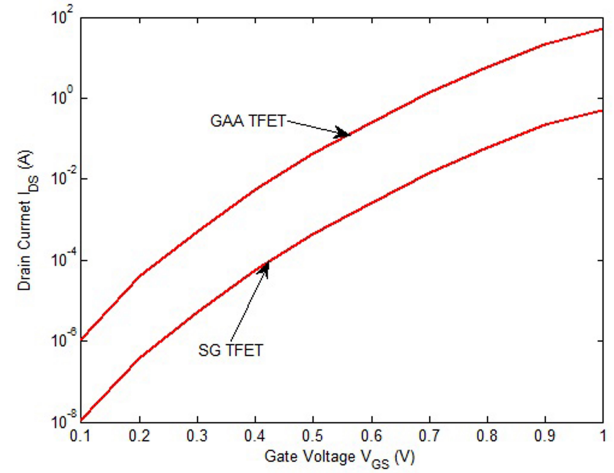


Fig.9: I_{DS} - V_{GS} Characteristics comparison of SG TFET and GAA TFET for channel length $L=45\text{nm}$ with $V_{DS}= 0.5\text{V}$.

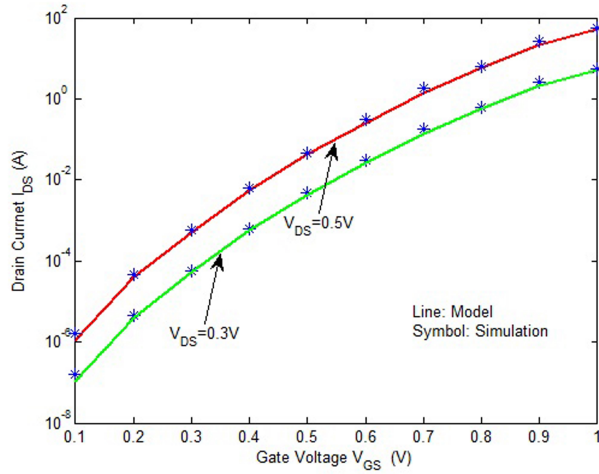


Fig.8: I_{DS} - V_{GS} Characteristics of GAA TFET for channel length $L=45\text{nm}$ with $V_{DS}=0.3\text{V}$ and 0.5V .

metal for SG TFET is chosen as 4.5 eV. As shown in the figure, the drain current increases with increasing gate-source bias. Furthermore, the comparative analysis of GaN based SG-TFET and GAA TFET devices is done and the outcome is shown in Fig. 9. From this figure, it is clear that, GaN based GAA TFET has more advantage compare to the SG TFET, in terms of its higher I_{ON} current

6. CONCLUSION

In this work, an attempt has been made to develop 2D models for analyzing surface potential, electric field along the channel, vertical electric field and drain current for GaN based SG TFET and GAA TFET. The results obtained clearly show that GaN based GAA TFET has more advantage compare to the SG TFET, in terms of its higher I_{ON} current. The an-

alytical results have been compared with the TCAD simulated results and a good agreement is achieved between both of them. This research can be extended further by doing elaborate studies.

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