Synthesis and Analysis of a Series-Connected Switched-Capacitor DC-DC converter

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ABSTRACT

In this paper, the synthesis and the analysis of a series-connected SC (Switched Capacitor) DC-DC converter is introduced. Aiming at an IC implementation of a stepped-down converter for mobile devices, we synthesize the series-connected DC-DC converter by using a family of the charge-averaging type converter. Different from conventional converters, the proposed converter provides only Q/P ($P \in \{2,3,\ldots,N\}$ and $Q \in \{1,2,\ldots,N-1\}$) stepped-down voltages. However, the number of power switches for the proposed converter is less than 75 % of that for the conventional converters. Furthermore, the characteristics concerning efficiency and ripple factor are clarified by theoretical analyses since the theoretical analyses concerning the series-connected SC power converters have not been performed as far as authors know. The analysis results provide the limitation values of the characteristics of designed circuits. The validity of the circuit design and the theoretical analysis is confirmed by SPICE simulations. Under the condition that the output load $R_L = 5\Omega$, the simulations show that 1. the power efficiency is more than 90 %, 2. the electrical power is about 440 mW, and 3. the ripple factor is less than 0.05.

Keywords: DC-DC converters, switched-capacitor circuits, series-connected circuits, step-down conversion

1. INTRODUCTION

Recently, in the field of mobile devices, switched-capacitor (SC) power converters [1-12] attract many researchers' attention, because they can be constructed without magnetic elements. Thus the SC power converters have possibility to implement into IC chips. In the field of mobile devices, supply voltages to the building blocks are becoming small with the progress of VLSI technology. Therefore, in the design of the SC power converters, flexibility of output voltages is desired. However, the number of combinations of voltage-conversion in the SC converters depends on it's structure[1].

Then they cannot convert the voltage continuously with high efficiency. To solve this problem, series-connected SC DC-DC converters have been proposed [5-6]. By connecting N ($N = 2,3,\ldots$) converters in series, they can provide various output voltages. In the previous studies, the series-connected DC-DC converters have been constructed with ring type converters [7-11]. The conventional converters are able not only to supply various output voltages but also to achieve long working-life[2].

However, the circuit size of the series-connected converters is large. Furthermore, as far as authors know, the theoretical analyses concerning the series-connected SC power converters have not been performed yet.

In this paper, in order to design a switched-capacitor (SC) DC-DC converter with various output voltages, a series-connected SC DC-DC converter is proposed, and its characteristics are analyzed theoretically. Aiming at an IC implementation of a stepped-down converter for mobile devices, we synthesize the series-connected DC-DC converter by using a family of the charge-averaging type converter [12]. Different from the conventional converters, the proposed converter provides only Q/P ($P \in \{2,3,\ldots,N\}$ and $Q \in \{1,2,\ldots,N-1\}$) stepped-down voltages. However, the number of power switches for the proposed converter is less than 75 % of that for the conventional converters. Furthermore, to clarify the limitation values of the characteristics of the designed circuit, theoretical analyses are performed concerning power efficiency and ripple factor.

2. CIRCUIT STRUCTURE

Figure 1 shows the block diagram of the series-connected SC DC-DC converter. The converter consists of N ($= 2,3,\ldots$) converter blocks, where N denotes the number of the converter blocks. To provide stepped-down voltages for mobile devices, a family of the charge-average type DC-DC converter [12] shown in Fig.2 is employed. As Fig.2 shows, the converter block can be constructed with $3P-1$ power switches and P ($P \in \{2,3,\ldots,N\}$) capacitors. The power switches $S_{1,k}$ and $S_{2,k}$ are driven by non-overlapped 2 phase clock pulses $\Phi_{1,k}$ and $\Phi_{2,k}$, respectively. By

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[1]The number of combinations of output voltages is determined by the number of capacitors in converters.

[2]The long working-life is achieved by separating the block that breaks down, and composing the circuit only of normal blocks.

controlling the timing of the clock pulses, the converter block performs Q/P ($Q \in \{1, 2, \ldots, N-1\}$) step-down conversion. The proposed converter of Fig.1 can be constructed with $N \times (3P-1)$ power switches and $N \times (P+1)$ capacitors.

On the other hand, the ring-type converter proposed in [7-11] is constructed with $4P$ power switches and P capacitors. Therefore, the series-connected converters using the ring-type converters require $N \times 4P$ power switches and $N \times (P+1)$ capacitors. Hence, the number of power switches for the proposed converter is less than 75 % of that for the conventional converters.

The theoretical analyses of the proposed converter are as follows.

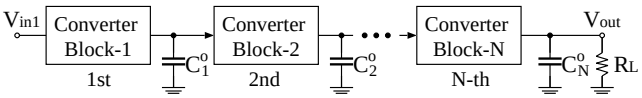

Fig.1: *Block diagram of series-connected converter.*

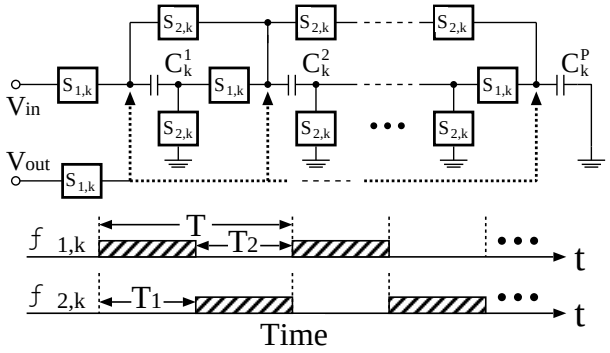

Fig.2: *Detail of converter block.*

3. THEORETICAL ANALYSIS

3.1 Equivalent Circuit

To simplify theoretical analyses, we assumed that the on-resistances of power switches are 0 and the influences of parasitic elements can be disregarded[3] . Firstly, the equivalent circuit of the converter block is analyzed.

The instantaneous equivalent circuits of the 1st converter block can be expressed by the circuit shown in Fig.3. In the steady state, the differential values of the electric charges in C_k^n ($k \in \{1, 2, \ldots, N\}$ and $n \in \{1, 2, \ldots, P\}$) and C_k^o satisfy

$$\Delta q_{\Phi_1}^n + \Delta q_{\Phi_2}^n = 0, \qquad (1)$$

where $\Delta q_{\Phi_1}^n$ and $\Delta q_{\Phi_2}^n$ denote the electric charges when $\Phi_{1,k}$ and $\Phi_{2,k}$, respectively.

[3]To clarify the maximum power efficiency, the theoretical analysis is performed under these conditions. The analysis will provide the design condition for the maximum efficiency, because non-ideal factors are neglected.

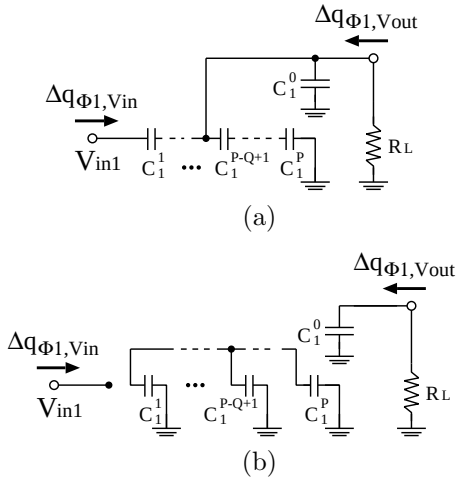

Fig.3: *Instantaneous equivalent circuits of 1-st converter block. (a) State: $\Phi_{1,k}$. (b) State: $\Phi_{2,k}$.*

In the case of $\Phi_{1,k}$, the differential values of the electric charges in the input and the output terminals, $\Delta q_{\Phi_1,V_{in}}$ and $\Delta q_{\Phi_1,V_{out}}$, are given by

$$\begin{aligned} \Delta q_{\Phi_1,V_{in}} &= \Delta q_{\Phi_1}^1 \\ &\vdots \\ &= \Delta q_{\Phi_1}^{P-Q} \\ \text{and} \quad \Delta q_{\Phi_1,V_{out}} &= -\Delta q_{\Phi_1}^1 + \Delta q_{\Phi_1}^o + \Delta q_{\Phi_1}^P \\ &\vdots \\ &= -\Delta q_{\Phi_1}^1 + \Delta q_{\Phi_1}^o + \Delta q_{\Phi_1}^{P-Q+1}. \end{aligned} \qquad (2)$$

On the other hand, in the case of $\Phi_{2,k}$, the differential values of the electric charges in the input and the output terminals, $\Delta q_{\Phi_2,V_{in}}$ and $\Delta q_{\Phi_2,V_{out}}$, are given by

$$\Delta q_{\Phi_2,V_{in}} = 0 \qquad \text{and} \qquad \Delta q_{\Phi_2,V_{out}} = \Delta q_{\Phi_2}^o. \qquad (3)$$

Furthermore, in the case of $\Phi_{2,k}$, C_k^n's satisfy the following condition:

$$\Delta q_{\Phi_2}^1 + \Delta q_{\Phi_2}^2 + \cdots + \Delta q_{\Phi_2}^P = 0. \qquad (4)$$

From Eqs.(1), (2), and (4), the following equation can be derived:

$$Q \Delta q_{\Phi_1}^P = -(P-Q) \Delta q_{\Phi_1}^1. \qquad (5)$$

Here, the average currents of the input and the output are given by

$$\begin{aligned} \overline{I_{in}} &= \frac{\Delta q_{\Phi_1,V_{in}} + \Delta q_{\Phi_2,V_{in}}}{T} \\ \text{and} \qquad \overline{I_{out}} &= \frac{\Delta q_{\Phi_1,V_{out}} + \Delta q_{\Phi_2,V_{out}}}{T}, \end{aligned} \qquad (6)$$

where T denotes a period of clock pulses. By substituting Eqs.(1), (2), (3), (5) into (6), the relation

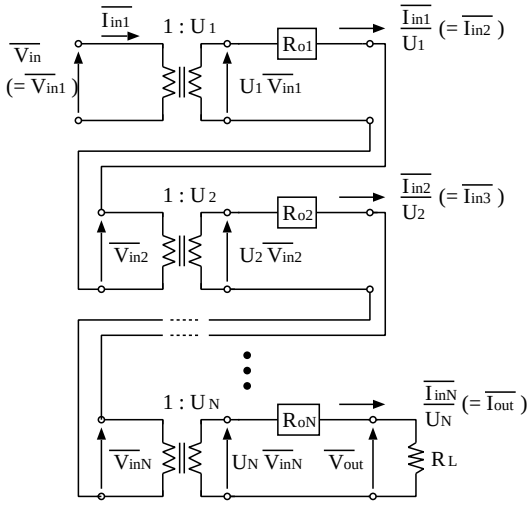

Fig.4: *Equivalent circuit of proposed circuit.*

between the input current and the output current is derived as follows:

$$\begin{aligned} T\overline{I_{in}} &= \Delta q^1_{\Phi_1} \\ T\overline{I_{out}} &= -\frac{P}{Q}\Delta q^1_{\Phi_1} \\ \text{and} \qquad \overline{I_{in}} &= -\frac{Q}{P}\overline{I_{out}}. \end{aligned} \tag{7}$$

Here, we assume that the voltages of capacitors, $V_{C^n_k}$'s, satisfy $V_{C^n_k}(sT) \simeq V_{C^n_k}((s+1)T)$ $(s = 1, 2, \dots)$ when $C^1_k = C^2_k = C^3_k = C^o_k = C$ and $C^o_k R_L \gg T$. Under these conditions, the following equation can be obtained from Fig.3:

$$\Delta q_{\Phi_1, V_{in}} = \frac{C}{P-Q}(\overline{V_{in}} - \overline{V_{out}}) - \frac{C}{P}\overline{V_{in}}. \tag{8}$$

By substituting Eqs.(2) and (7) into (8), the following equation is derived :

$$\overline{V_{in}} = \frac{P}{Q}\overline{V_{out}} - \frac{T(P-Q)}{C}\,\overline{I_{out}}. \tag{9}$$

From Eqs.(7) and (9), the following determinant can be obtained:

$$\begin{bmatrix} \overline{V_{in}} \\ \overline{I_{in}} \end{bmatrix} = \begin{bmatrix} \frac{P}{Q} & 0 \\ 0 & \frac{Q}{P} \end{bmatrix} \begin{bmatrix} 1 & \frac{Q(P-Q)T}{PC} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{out}} \\ -\overline{I_{out}} \end{bmatrix}, \tag{10}$$

where $Q(P-Q)T/(PC)$ is called an SC resistance. Hence, the equivalent circuit of the proposed converter can be expressed by the circuit of Fig.4. In Fig.4, U_k $(k \in \{1, 2, \dots, N\})$ denotes the ratio of the k-th ideal transformer, Q_k/P_k. Furthermore, the equivalent circuit of Fig.4 can be summarized as the circuit shown in Fig.5. The determinant which expresses Fig.5 is given by

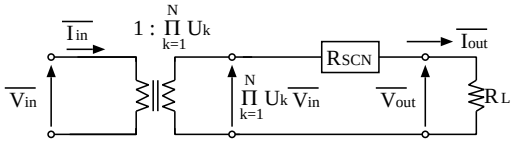

Fig.5: *Equivalent circuit of proposed circuit.*

$$\begin{bmatrix} \overline{V_{in}} \\ \overline{I_{in}} \end{bmatrix} = \begin{bmatrix} 1/\Pi_{k=1}^N U_k & 0 \\ 0 & \Pi_{k=1}^N U_k \end{bmatrix} \cdot \begin{bmatrix} 1 & R_{SCN} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{out}} \\ -\overline{I_{out}} \end{bmatrix}. \tag{11}$$

In Eq.(11), the summarized SC resistance R_{SCN} is given by

$$\begin{aligned} R_{SCN} &= R_{oN} + U_N^2 R_{SCN-1}, \\ \text{where} \qquad R_{SC1} &= R_{o1}. \end{aligned} \tag{12}$$

As Fig.5 shows, the averaged output voltage $\overline{V_{out}}$ is obtained by

$$\overline{V_{out}} = \frac{R_L}{R_L + R_{SCN}} \cdot \Pi_{k=1}^N U_k \overline{V_{in}}. \tag{13}$$

Obviously, the number of combinations of voltage-conversion increases according to the parameter N.

3.2 Power Efficiency

The electric power consumed by the output load R_L in one period is given by

$$\begin{aligned} P_{RL} &= (\overline{I_{out}})^2 R_L \\ &= (\frac{\overline{I_{in}}}{\Pi_{k=1}^N U_k})^2 R_L. \end{aligned} \tag{14}$$

On the other hand, the electric power consumed by the resistance R_{ok} $(= Q(P-Q)T/(PC))$ in one period is given by

$$\begin{aligned} P_{okLoss} &= I^2_{ink+1} R_{ok} \\ &= (\frac{\overline{I_{in}}}{\Pi_{i=1}^k U_i})^2 R_{ok}. \end{aligned} \tag{15}$$

From Eqs.(14) and (15), the efficiency is expressed by

$$\begin{aligned} \eta &= \frac{P_{RL}}{P_{RL} + P_{o1Loss} + P_{o2Loss} + \cdots + P_{oNLoss}} \\ &= \frac{\frac{R_L}{(\Pi_{k=1}^N U_k)^2}}{\frac{R_L}{(\Pi_{k=1}^N U_k)^2} + \sum_{j=1}^{N} \frac{R_{oj}}{(\Pi_{i=1}^j U_i)^2}} \\ &= \frac{R_L}{R_L + R_{SCN}}. \end{aligned} \tag{16}$$

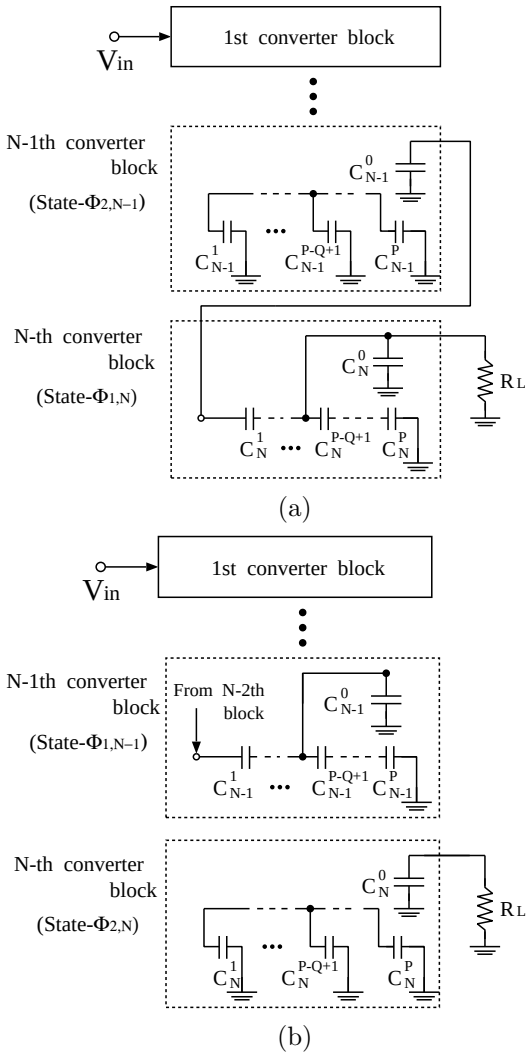

Fig.6: *Instantaneous equivalent circuits of proposed converter. (a) State-1. (b) State-2.*

The power efficiency of Eq.(16) means the maximum efficiency, because non-ideal factors are neglected. Therefore, the power efficiency obtained by simulations or experiments should be less than that of Eq.(16).

3.3 Output Ripple Factor

Figure 6 shows the instantaneous equivalent circuits of the proposed circuit. In consideration of the hardware cost, we assume that all converter blocks work synchronously. Furthermore, to prevent the input terminal being connected directly with the output terminal, the polarities of the clock pulses for k-th converter blocks are set to opposite to that for $k+1$-th converter blocks (see Fig.6).

In the case of $State-1$ (see Fig.6 (a)), the output voltage of the proposed converter, $V_{out,1}(t)$, is given by

$$V_{out,1}(t) = V_{max,1}\exp(-\frac{t}{\tau_1}), \quad (17)$$

$$\text{where} \quad \tau_1 = R_L C\{1+\frac{P+1}{Q(P-Q+1)}\}.$$

In Eq.(17), $V_{max,1}$ denotes the output voltage when $V_{out,1}(0)$.

On the other hand, in the case of $State-2$ (see Fig.6 (b)), the output voltage $V_{out,2}(t)$ is given by

$$V_{out,2}(t) = V_{out,1}(T_1)\exp(-\frac{t}{\tau_2}), \quad (18)$$

$$\text{where} \quad \tau_2 = R_L C.$$

Then the output voltage ripple ΔV_{out} is expressed by

$$\Delta V_{out} = V_{out,1}(0) - V_{out,2}(T_2)$$
$$= V_{max,1}\{1-\exp(-\frac{T_1}{\tau_1})\cdot\exp(-\frac{T_2}{\tau_2})\}. \quad (19)$$

Here, we consider the worst case: $T_2 \gg T_1\ (\simeq 0)$ [4] . Under this condition, Eq.(19) can be approximated by

$$\Delta V_{out} \simeq V_{max,1}\{1-\exp(-\frac{T_2}{\tau_2})\},$$
$$\simeq V_{max,1}\{1-\exp(-\frac{T}{CR_L})\}. \quad (20)$$

The average output voltage $\overline{V_{out}}$ is given by

$$\overline{V_{out}} = \frac{1}{T_1}\int_0^{T_1} V_{out,1}(t)dt + \frac{1}{T_2}\int_0^{T_2} V_{out,2}(t)dt. \quad (21)$$

Here, by applying the condition: $T_2 \gg T_1\ (\simeq 0)$ in

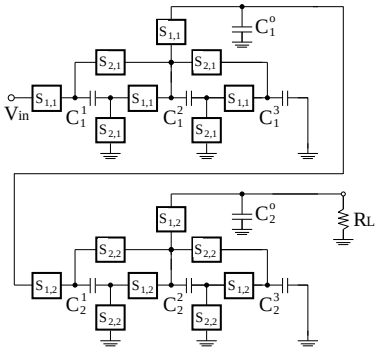

Fig.7: *Simulated converter.*

[4]From Eqs.(17) and (18), τ_1 is larger than τ_2. Therefore, the output ripple becomes large in proportion to the increase of T_2. That is, we can obtain the maximum value of the output ripple when $T_1 \simeq 0$. Through this analysis, the worst value of the ripple factor will be clarified.

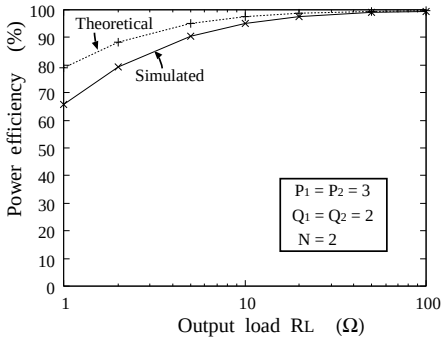

Fig.8: *Simulated power efficiency.*

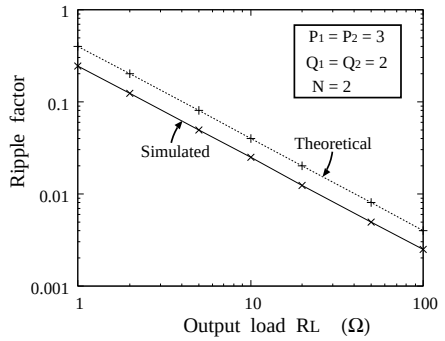

Fig.9: *Simulated ripple factor.*

Eq.(21), we derive the following equation:

$$\overline{V_{out}} \simeq \frac{1}{T}\int_0^T V_{max,1}\exp(-\frac{t}{CR_L})dt \simeq \frac{V_{max,1}CR_L}{T}\{1-\exp(-\frac{T}{CR_L})\}. \quad (22)$$

Then, from Eqs.(20) and (22), the worst case of the output ripple factor V_{rip} can be obtained by

$$V_{rip} = \frac{\Delta V_{out}}{\overline{V_{out}}} = \frac{T}{CR_L}. \quad (23)$$

The output ripple factor obtained by simulations or experiments should be less than that of Eq.(23).

4. SIMULATION

To confirm the validity of the circuit design, SPICE simulations were performed concerning the circuit shown in Fig.7. The SPICE simulations were performed under the conditions that $V_{in1} = 3.7$V [5] , $C_k^j = C_o^j = 5\mu$F, the clock frequency $f = 500$kHz, the number of capacitors $P = 3$, the number of converter blocks $N = 2$, and the on-resistance of the power-switch $R_{on} = 0.2\Omega$ [6] .

[5]The typical voltage of the lithium battery used in the mobile devices such as cellular phones is about 3.7 V.

[6]The power-switches were modeled by using the switch models of the SPICE simulator. In the SPICE simulations, the switches with small on-resistances were used, because the theoretical analyses were performed under the *ideal* conditions: 1. the on-resistances are 0, 2. the influence of parasitic elements is disregarded, and so on.

Figure 8 shows the simulated power efficiency. As Fig.8 shows, the power efficiency of the proposed converter is more than 90 % when the output load R_L is 5Ω. The electrical power of the simulated converter is about 440 mW at $R_L = 5\Omega$. In Fig.8, the best values of power efficiency calculated by Eq.(16) are larger than that of the simulated values.

Figure 9 shows the simulated ripple factor. As Fig.9 shows, the ripple factor of the proposed converter is less than 0.05 when the output load R_L is 5Ω. The simulated results are less than that of the theoretical results calculated by Eq.(23), because Eq.(23) provides the worst values of the ripple factor. In Fig.9, the tendency of these characteristic curves is same.

5. CONCLUSION

The synthesis and the analysis of a series-connected SC DC-DC converter employing charge-average type SC DC-DC converters has been performed in this paper. The validity of the circuit design and the theoretical analysis was confirmed by SPICE simulations. The number of power switches for the proposed converter is less than 75 % of that for the conventional converters. Under the condition that the output load $R_L = 5\Omega$, the simulations showed that 1. the power efficiency is more than 90 %, 2. the electrical power is about 440 mW, and 3. the ripple factor is less than 0.05.

The fluctuation analysis of the proposed converter is left to the future study, because it is important to analyze the influence of the fluctuation of circuit elements in the converters containing a lot of circuit components.

6. ACKNOWLEDGEMENTS

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