Cascode Current Mirror for a Variable Gain Stage in a 1.8 GHz Low Noise Amplifier (LNA)

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ABSTRACT

A high frequency CMOS variable gain low noise amplifier (VGLNA) constructed based on an inductive source degenerated LNA and a cascode current mirror is proposed. The 'variable' concept is to prevent the unwanted saturation phenomenon due to large input signal. A cascode current mirror cell which consumes minimal voltage headroom without sacrificing the accuracy of the circuit is proposed in the circuit. With a 0.18 m CMOS technology, this technique is applied on a VGLNA operating at 1.8 GHz for GSM band application. The simulation results reveal that the maximum gain is 17.29 dB with gain tuning range of 9.56 dB. The noise figure (NF) is less than 0.92 dB with the power consumption of 9.34 mW at power supply of 1.8 V. Comparison with several same operating frequency LNA circuits published show that this work demonstrated among the lowest NF and highest IIP3 with compromise on the gain.

Keywords: cascode current mirror, low noise amplifier, noise figure, variable gain

1. INTRODUCTION

Current sources are widely used in amplifiers, either single-stage or differential amplifiers. In these circuits, current source acts as a large resistor without consuming excessive voltage headroom. Some digital-to-analog converters (DAC) employed an array of current sources to produce an analog output proportional to digital input signal. Current sources, in conjunction with "current mirrors" can perform useful functions in analog signals. Some modifications to a current mirror, act as a low voltage cell can bring in lots of advantages to the analog design especially in the wireless communication field. With the trend towards fully integrated wireless transceivers which demand portable and low power consumption devices [1], a breakthrough of design techniques in transceivers is highly desirable.

This paper presents a design of variable gain stage utilizing a cascode current mirror as a low voltage cascode cell for a variable gain low noise amplifier (VGLNA). A variable gain in an LNA is to prevent saturation of the receiver when the input signal is relatively large. There has been several gain control techniques presented, such as using a bypass switch in the main amplifier and achieving different gain levels [2]. However, the gain, linearity and the return loss are no longer controllable parameters and the switch path may induce losses. Another popular method is splitting a portion of current from the amplifier [3-4]. However, in this technique, the return loss becomes worse and higher noise is introduced in low gain mode.

In this paper, a high frequency VGLNA employing a cascode current mirror which could eliminate the accuracy and voltage headroom trade-off to achieve gain control is presented. This work demonstrates a CMOS VGLNA working at 1.8 GHz frequency band, capable to achieve gain control as well as maintaining its input and output return loss in different mode (high gain and low gain modes) without degrading the noise performance.

2. VARIABLE GAIN LOW NOISE AMPLIFIER CIRCUIT DESIGN

Among the common structure of single-ended amplifiers, namely, resistive termination, 1/gm termination, shunt-series feedback and inductive source degeneration, the last one has the best noise performance. Here, a single stage cascode LNA with inductive source degeneration topology is used, as shown in Fig. 1. A single-stage topology is chosen to minimize the power dissipation and to improve third-order intercept point (IP3) performance.

In this paper, the proposed VGLNA can meet two merits, the unconditional stability in each stage and low power consumption. The LNA is the first functional block in a wireless receiver. At the early stage of a receiver, the noise figure (NF) of the LNA is the dominant issue as the received signal is very small. However, as the received signal becomes large, the IIP3 becomes an important parameter to prevent the

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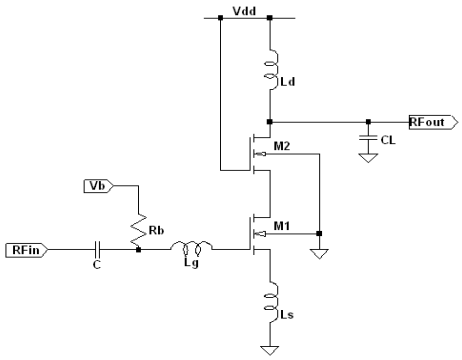

Fig.1: *Cascode Low Noise Amplifier (LNA) with Inductive Source Degeneration Structure.*

receiver from reaching saturation. Therefore, a cascode current mirror is added to act as the variable gain stage, completing the gain-adjustable mechanism [5].

2.1 Inductive Source Degenerated LNA

There are a few existing LNA papers which has been presented in the range of frequency between 1.6 - 3.0 GHz. An LNA microwave monolithic integrated circuit (MMIC) has been implemented in silicon-on-insulator (SOI) CMOS technology with just a drain voltage of 0.6 V, giving the Gain/Power quotient of 5.33 dB/mW [6]. This amplifier is matched internally using two spiral inductors and a capacitor. By inserting just a single inductor acting as an inter-stage matching network, a 2-GHz LNA can also be optimized [7]. On the other hand, a high-Q active inductor is introduced into a 1.75-GHz CMOS LNA to reduce the area of chip and the complexity [8]. The chip area which is often occupied with integrated passive inductor is usually large compared to other components. Hence, an active inductor implemented from a gyrator has been proposed. As for the multiband purpose, an LNA using positive feedback to improve its gain has been presented [9]. The use of positive feedback improves the gain compared to all of the other common-gate LNA topologies. Another LNA topology worth mentioning is the CMOS LNA operating at subthreshold region with one of the best overall figure of merit (FOM) [10]. All these LNAs were optimized for performance in terms of supply voltage, power consumption and NF. However, none has yet explore the possibility of providing gain variation to the existing structures of LNA like the source degenerated structure. This could save cost with the existing LNAs and with the gain variation; this could prevent saturation of the receivers if the input signal is too large.

Therefore the inductive source degenerated LNA topology as shown in Fig. 1 is adapted to be used as variable-gain LNA or VGLNA due to its minimum NF which uses a source degenerative inductor to realize input impedance matching [5]. The circuit is optimized to work at the resonance frequency of 1.8 GHz with the input impedance written as

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right) L_s \qquad (1)$$

where g_m is the device transconductance and C_{gs} is the gate-to-source capacitance. At the frequency of operation, value of L_s can be chosen in order for the real term to be made equal to 50 Ω bringing impedance matching to the input stage. For the power matched at resonance, the real part of input impedance need to be equalled to source resistance. For the noise factor (F) calculation, the size of the input transistor is chosen such that it minimizes the noise based on the following expression [5]:

$$F_{min} \cong 1 + \sqrt{\frac{4}{5}} \frac{\omega}{\omega_T} \sqrt{\gamma.\delta.(1 - |c^2|)} \qquad (2)$$

where $\omega_T = g_m/C_{gs}$, the unity gain frequency with gm is the transistor transconductance and C_{gs} is the gate source capacitor. $\gamma = 3/2$ is the channel thermal noise, c is the complex correlation term which is equal to j0.395, $\delta = 4/3$ is the coefficient of gate noise. As observed from (2), F_{min} is effective for $\omega < \omega_T$ and the noise factor increases with frequency. Owing to the down scale of CMOS process, the ω_T would raises, allowing circuits to operate at higher frequency while maintaining the minimum noise factor. It is noted that the noise parameters: γ, δ and c in the above calculation are considered independent of the bias voltage.

The key property of a current mirror is to allow precise copying of the current with no dependence on process and temperature. Therefore, to suppress these dependence like the channel-length modulation, a cascode current mirror as shown in Fig. 2 that have identical drain-source voltage and a high output resistance is proposed. These transistors are in saturation and proper rationing ensures that $VGS5 = V_{GS6}$. If

$$\begin{aligned} V_{con} &= V_{GS5} + (V_{GS3} - V_{TH3}) \\ &= V_{GS6} + (V_{GS4} - V_{TH4}) \end{aligned} \qquad (3)$$

then the cascode current source M4 and M6 consumes minimum headroom (the overdrive of M4 plus that of M6) while M3 and M4 sustain equal drain-source voltages, allowing accurate copying of I_{REF}. The voltage, V_{con} is the voltage that flows from the LNA stage to the cascode current mirror.

In this work, the cascode current mirror is used to achieve gain control function. Referring to Fig. 2, the cascode current mirror is comprised of transistors M3-M6, a reference current, I_{REF} and bias voltage,

V_b. These transistors are controlled through changes in the bias resistance, R_b which influences the current, I_b flowing through the transistors M5 and M6. At the source terminal of M3 and M4, voltage, V_{con} flows from the LNA stage with the DC signal blocked by a DC blocking capacitor C_{bl} while steering the RF signal into the current mirror. Thus, by changing R_b, taking a constant V_b divided by R_b, a set of current values, I_b is produced.

For this analysis, R_b remained constant and V_b is being varied from 1.0 to 1.8 V resulting in gain variation with the range of 9.56 dB. The advantage of this gain controlled mechanism is that the gain variation is achieved without degrading the noise performance since there are constructed from two different stages.

Comparing this structure with the traditional cascode current mirror in Fig. 3, the minimum allowable voltage is two overdrive voltage plus one threshold voltage as shown here,

$$V_{con} = V_{GS1} + V_{GS3} \tag{4}$$

Comparing (4) and (3), one threshold voltage is "wasted" in the voltage headroom of the current mirror [11]. Therefore, in this work, the proposed cascode mirror with two overdrive voltage headroom as shown in Fig. 2 is termed as "low-voltage cascode" and implemented as variable gain stage.

Combining the circuits of Fig. 1 and 2, a VGLNA based on inductive source degenerated structure is proposed as shown in Fig. 4. The VGLNA is designed to work at 1.8 GHz and it is simulated to meet the best desired requirements. However, there is a drawback with the need of using a higher biased voltage, V_{biased} at approximately 3.0 V for the variable gain stage. Nevertheless, the power consumption stays at 9.34 mW.

At the output, the inductor L_o and capacitor C_o are chosen to match the output impedance. This formed an output LC-tank circuit which is used to tune the VGLNA to the resonance frequency.

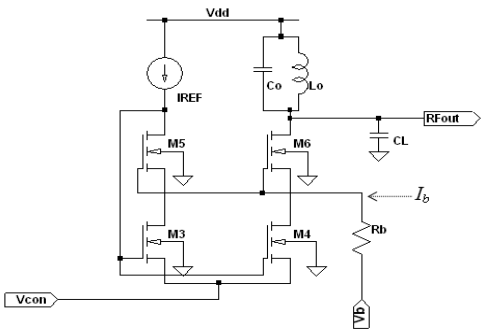

Fig.2: *Proposed Cascode Current Mirror as Variable Gain Stage.*

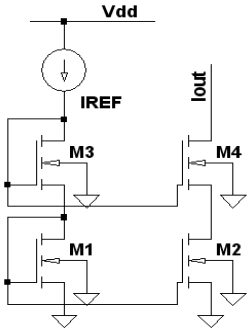

Fig.3: *Cascode Current Mirror with voltage headroom consumed.*

3. SIMULATION RESULTS

The complete VGLNA was simulated with parameters from a standard 0.18-μm CMOS process technology using Agilent's Advanced Design System (ADS). The transistors width, inductors and capacitors values are shown in Table I and the minimum length of the transistors is 0.22 μm. The control voltage of V_{b2} ranged from 1.0 to 1.8 V and the supply voltage V_{dd} is 1.8 V.

The Fig. 5 to 9 show the simulation results for S21, S11, S12 and S22 where the amplifier is tuned around 1.8 GHz at high gain mode (HGM) and low gain mode (LGM) respectively. HGM is achieved when the control voltage is applied at 1 V while the LGM is achieved when V_{b2} = 1.8 V. It can be seen that S21 is 17.29 dB at HGM and 7.73 dB at LGM. In the HGM, the input return loss or S11 is -16.67 dB while in the LGM, it is equalled to -14.78 dB. In Fig. 7, it shows that the reverse isolation S12 at the HGM is better than the LGM with the overall reverse isolation less than -38 dB. As for the output return loss, the S22 results are shown in Fig. 8. In Fig. 9, the NF is achieved at 0.92 dB regardless of operating in HGM or LGM. As for the two tones testing, two tones are located at 1.80 GHz and 1.82 GHz with the power level of -20 dBm. The third-order input intercept point (IIP3) simulated are 6.34 dBm and 5.59 dBm at HGM and LGM respectively. The power consumed by the VGLNA at power supply of 1.8 V is simulated to be 9.34 mW at both modes.

Table II shows the performance of this work and comparison with several 1.8 GHz LNA circuits published [12, 13]. However, the performances of the LNA in [6, 12] are measured values while in [13] the results are simulated values. To compare overall performance of the LNAs, the gain over power quotient and figure of merit (FOM) based on [10] has been used. It is observed that this work demonstrated the lowest NF and highest Gain/Power quotient. This VGLNA has the best FOM with the reasonable power consumption as compared to LNA in [6].

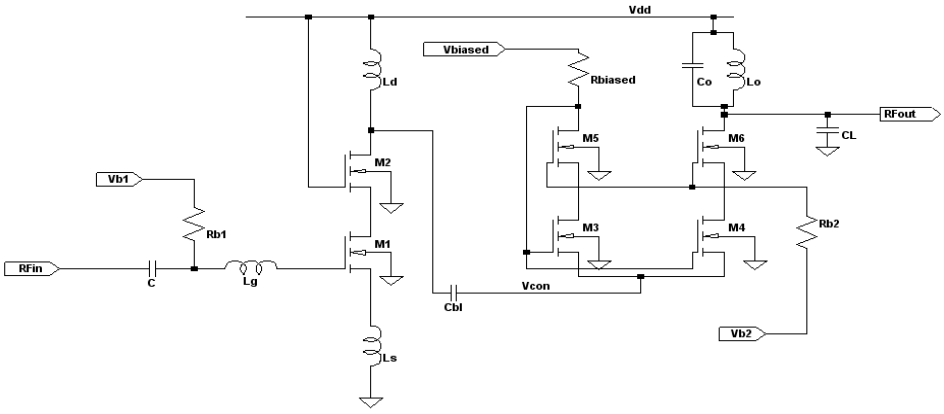

Fig.4: *Schematic of the Proposed VGLNA.*

Table 1: *Component values and device dimensions.*

Parameters	Value
W_{M1}	190μm
W_{M2}	60μm
W_{M3}	410μm
W_{M4}	20μm
$W_{M5,M6}$	500μm
L_g	10.8nH
L_s	0.9nH
L_d	14.8nH
L_o	1.8nH
C_o	3.8pH
$C_{L,in}$	0.5pH

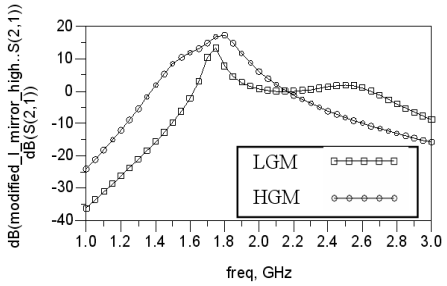

Fig.5: *Voltage Gains in the Low Gain Mode (LGM) and High Gain Mode (HGM).*

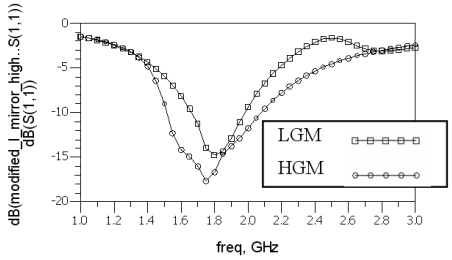

Fig.6: *S11 of the Proposed VGLNA in Low Gain Mode (LGM) and High Gain Mode (HGM).*

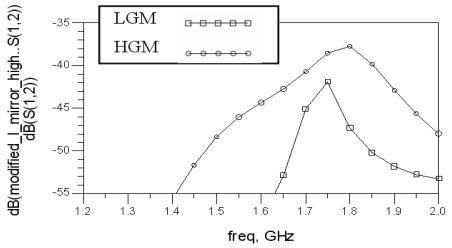

Fig.7: *S12 of the Proposed VGLNA in Low Gain Mode (LGM) and High Gain Mode (HGM).*

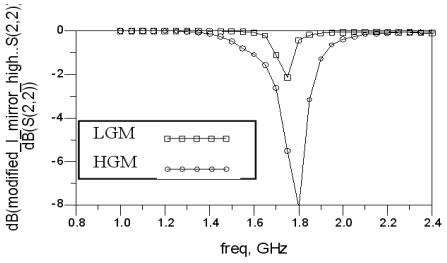

Fig.8: *S22 of the Proposed VGLNA in Low Gain Mode (LGM) and High Gain Mode (HGM).*

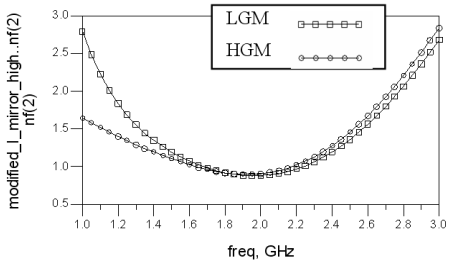

Fig.9: *Noise Figure (NF) of the Proposed VGLNA in Low Gain Mode (LGM) and High Gain Mode (HGM).*

Table 2: *Comparison of several 1.6 - 1.8 GHz LNAs.*

Descriptions	**This work**	**[6]**	**[12]**	**[13]**
Supply voltage (V)	1.8	0.6	1.5	3.0
Process(μm)	0.18	0.35	0.25	0.8
Operating frequency (GHz)	1.8	1.6	1.8	1.8
NF(dB)	0.92	4.2	5	2.1
Gain(dB)	17.29	10.8	14.1	18.0
IIP3(dBm)	6.34	12	-7.6	-5
S11(dB)	-16.67	-	-23.5	-
Power consumption (mW)	9.34	7.5	30	48
Gain/P_{dc}	1.85	1.44	0.47	0.375
FOM	22.83	14	-1.52	-2.78

4. CONCLUSIONS

A 1.8 GHz VGLNA has been designed in 0.18 m CMOS process for GSM application. The VGLNA uses a modified cascode current mirror technique to achieve gain control function. Only minimal voltage headroom is required in the cascode current mirror for the variable gain stage. Regardless of gain modes, the VGLNA achieves NF of less than 0.92 dB with input return loss of -16.67 and -14.78 in HGM and LGM respectively. Operating at 1.8 V supply voltage, the circuit provides a maximum gain of 17.29 dB and a minimum gain of 7.73 dB. In the linearity response, the VGLNA acquires IIP3 of 6.34 dBm in HGM. The proposed VGLNA offers a compromise between gain, NF and linearity. The simulated results fulfil the specifications for a 1.8 GHz LNA design. Thus, this VGLNA can be used to achieve amplification in a wireless receiver front-end which requires a fully integrated, low noise and low power consumption architectures.

5. ACKNOWLEDGEMENT

This research is supported by Ministry of Science, Technology and Innovation (MOSTI) of Malaysia through National Science Fellowship (NSF) and Silterra (M) Sdn. Bhd..

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