Low-offset BiCMOS Current Controlled Current Differencing Buffered Amplifier (CC-CDBA) and Applications

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ABSTRACT

This article presents the design for a basic current-mode building block for analog signal processing, called Current Controlled Current Differencing Buffered Amplifier (CC-CDBA). Its parasitic resistances at two current input ports can be controlled by an input bias current. The output current and voltage offset are quite low. The proposed element was realized in a BiCMOS technology and the voltage follower in the element is modified to achieve high performance properties. Its performances are examined through PSPICE simulations. In addition, examples as a current-mode multiplier/divider and current amplifier are included, compared to the conventional CC-CDBA implementation. They disclose performances of the proposed CC-CDBA superior to previous CC-CDBA.

Keywords: CC-CDBA, Current controlled, Current-mode, Multiplier, Divider, Current amplifier

1. INTRODUCTION

There has been much effort to reduce the supply voltage of electronic circuits in the last decade. This is due to the demand for portable and battery-powered equipment. Since a low-voltage operating circuit becomes necessary, the current-mode technique is ideally suited for this purpose more than the voltage-mode one. Consequently, there is a growing interest in synthesizing the current-mode circuits because of more their potential advantages such as larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry and low power consumption [1-2]. Many active elements able to function in current-mode such as OTA, current conveyor, current differencing buffered amplifier (CDBA) and current differencing transconductance amplifier (CDTA), have been introduced to response these demands.

The current differencing buffered amplifier is a reported active component especially suitable for a class of analog signal processing [3]. This device can operate in both current and voltage-modes, provides flexibility and enables a variety of circuit designs. In addition, it can offer advantageous features such as high-slew rate, free from parasitic capacitances, wide bandwidth and simple implementation [4]. However, the CDBA can not be controlled by the parasitic resistances at two current input ports so when it is used in a circuit, it must unavoidably require some external passive components, especially the resistors. This makes it not appropriate for IC implementation due to occupying more chip area, high power dissipation and cannot be electronic controllable. Recently, Maheshwari and Khan have proposed a modified-version CDBA whose parasitic resistances at two current input ports can be controlled by an input bias current and it is newly named current controlled current differencing buffered amplifier (CC-CDBA) [5]. Because the CC-CDBA in [5] was designed by using the BJT and a basic voltage follower, consequently, this structure has problem for the output offset errors because the BJT current mirrors in CC-CDBA provide errors due to practically internal factors more than a current mirror based on CMOS [6]. The offset output error from the basic voltage follower also affects the accuracies of circuits/systems. The offset problem is an important factor for circuit designers to be certain in practical implementations, especially in instrumentation and measurement systems.

The purpose of this paper is to design and synthesize a modified-version CC-CDBA. A BiCMOS technology is employed to develop this element. In addition, the voltage follower is also developed to reduce the offset output current and voltage. The performances of proposed BiCMOS CC-CDBA are illustrated by PSPICE simulations, they show good agreement as mentioned. The example applications as a multiplier/divider and current amplifier are com-

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prised, which are compared to the traditional CC-CDBA.

2. CIRCUIT CONFIGURATION

A. Basic Concept of CC-CDBA

CC-CDBA properties are similar to the conventional CDBA, except that input voltages of CC-CDBA are not zero and the CC-CDBA has finite input resistances R_p and R_n at the p and n input terminals, respectively. These parasitic resistances are equal and can be controlled by the bias current I_B as shown in Eqs. (1) and (2)

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 \\ 0 & R_n & 0 & 1 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix} \quad (1)$$

When

$$R_p = R_n = \frac{V_T}{2I_{B1}} \quad (2)$$

where V_T is the thermal voltage. The symbol and the equivalent circuit of the CC-CDBA are illustrated in Fig. 1(a) and (b), respectively.

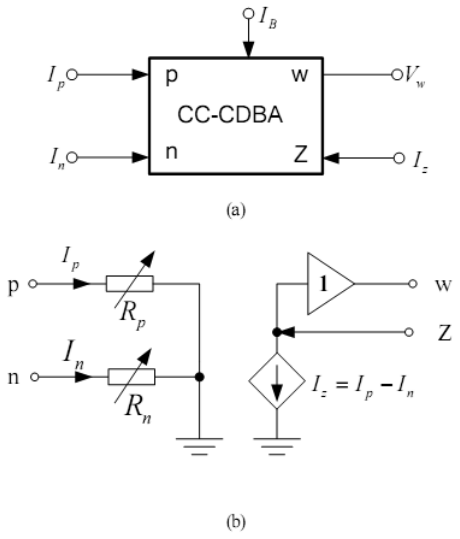


Fig.1: *The CC-CDBA (a) Symbol (b) Equivalent Circuit*

B. Simple BJT Current Mirror compared to MOS Current Mirror

Since the current mirror is the basic block to realize CC-CDBA, a comparison of the simple BJT and MOS current mirrors will be shown in this section. Fig. 2(a) displays the BJT current mirror. From routine analysis, the output current can be expressed to be [6]

$$I_{out} = \frac{\frac{I_{S2}}{I_{S1}} I_{in} \left(1 + \frac{V_{CE2} - V_{CE1}}{V_A}\right)}{1 + \frac{1-(I_{S2}/I_{S1})}{\beta_F}}. \quad (3)$$

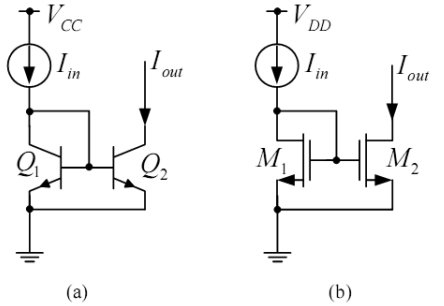


Fig.2: *Simple current mirrors based on (a) BJT (b) MOS*

If I_{S2}/I_{S1} is the ideal gain of the BJT current mirror and V_A is the Early voltage, the systematic gain error of the BJT current mirror (ε_{BJT}) can be found to be

$$\varepsilon_{BJT} = \frac{\left(1 + \frac{V_{CE2} - V_{CE1}}{V_A}\right)}{1 + \frac{1-(I_{S2}/I_{S1})}{\beta_F}} \cong \frac{V_{CE2} - V_{CE1}}{V_A} - \frac{1 - (I_{S2}/I_{S1})}{\beta_F}. \quad (4)$$

From Eq. (4), the first term is originated from finite output resistance and the second term comes from finite β_F. The MOS current mirror is illustrated in Fig. 2(b). By straightforward analysis, we will receive

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{in} \left(1 + \frac{V_{DS} - V_{DS1}}{V_A}\right). \quad (5)$$

If $(W/L)_2/(W/L)_1$ is the ideal gain of the MOS current mirror, the systematic gain error of the MOS current mirror (ε_{MOS}) can be expressed to be

$$\varepsilon_{MOS} = \frac{V_{DS2} - V_{DS1}}{V_A}. \quad (6)$$

From Eq. 6), the gain error of the MOS current mirror stems from only the finite output resistance implied from the Early voltage which differs from the gain error of the BJT. This result shows that the MOS current mirror has accuracy more than the BJT one. One reason is that the MOS generally provides higher Early voltage than the BJT does [6]. Consequently, CMOS is employed in the current mirrors to implement the proposed CC-CDBA.

C. A BiCMOS current differencing circuit which has finite input resistances

Fig. 3 displays a class AB translinear loop, which is used as input section. The BJT translinear is used to achieve linear adjustability of intrinsic resistances. When all transistors are considered to be matched elements and working in saturation-mode. The following currents can be obtained [7]

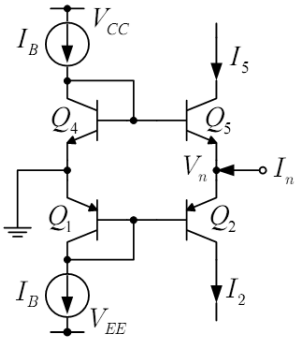


Fig.3: *Class AB translinear loop*

$$I_2 = I_B e^{(V_n/V_T)}, \tag{7}$$

and

$$I_5 = I_B e^{-(V_n/V_T)}. \tag{8}$$

Due to

$$I_n = I_2 - I_5. \tag{9}$$

Substituting Eqs. (7) and (8) into (9), it yields

$$I_n = 2I_B \sinh(V_n/V_T). \tag{10}$$

Since $(V_n/V_T) \cong V_n/V_T$, we will obtain

$$R_n = R_p = \frac{V_T}{2I_B}. \tag{11}$$

The BiCMOS current differencing circuit which has finite input resistances is shown in Fig. 4. The circuit implementation consists of mixed translinear loops (Q_1-Q_8). The mixed loops are DC biased by I_B using current mirrors (M_1-M_3 and M_8-M_9). The p and n terminal resistances can be obtained by Eq. (11). The z-terminal output that generates the current difference of p and n terminal is realized using transistors (M_4-M_7 and M_{10}-M_{13}).

From elementary small-signal circuit analysis, the output current I_Z of this circuit can be expressed as

$$I_Z = \alpha_p I_p - \alpha_n I_n + \varepsilon, \tag{12}$$

where α_p, α_n and ε are the current gains for the inputs from the terminals p, n and error term, respectively.

The expressions of each coefficient are shown to be

$$\alpha_p = \frac{g_{m6}g_{m6}g_{m13} + g_{m3}g_{m7}g_{m12}}{g_{m6}g_{m12}(g_{m6} + g_{m3} + g_{\pi3} + g_{\pi6})},$$

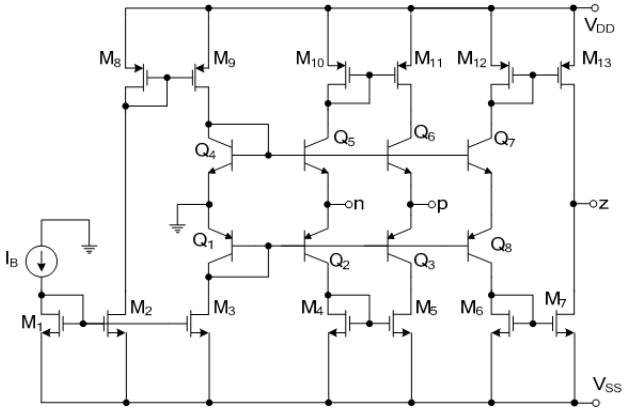


Fig.4: *A BiCMOS current differencing circuit which has finite input resistances*

$$\alpha_n = \frac{K_5 + K_4}{g_{m5} + g_{m2} + g_{\pi2} + g_{\pi5}}$$

$$\varepsilon = \frac{I_B}{g_{\pi4}\beta_4}(g_{m6}K_1 + K_4 + g_{m7}K_2 - K_6 - g_{m5}K_3) -$$

and $$\frac{I_B}{g_{\pi1}\beta_1}(g_{m3}K_1 + K_5 + g_{m8}K_2 - K_7 - g_{m2}K_3),$$

where
$$K_1 = \frac{g_{m6}g_{m6}g_{m13} + g_{m3}g_{m7}g_{m12}}{g_{m6}g_{m12}(g_{m6} + g_{m3} + g_{\pi3} + g_{\pi6})},$$

$$K_2 = \frac{g_{m6}g_{m13}g_{m7} + g_{m7}g_{m12}g_{m8}}{g_{m6}g_{m12}(g_{m7} + g_{m8} + g_{\pi7} + g_{\pi8})},$$

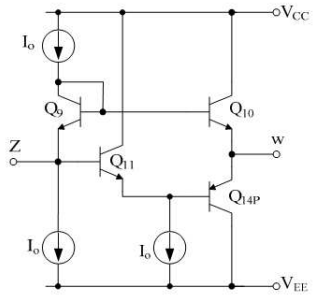
$$K_3 = \frac{K_5 + K_4}{g_{m5} + g_{m2} + g_{\pi2} + g_{\pi5}},$$

$$K_4 = \frac{g_{m5}g_{m13}g_{m11}}{g_{m12}(g_{m12} + g_{\pi11}},$$

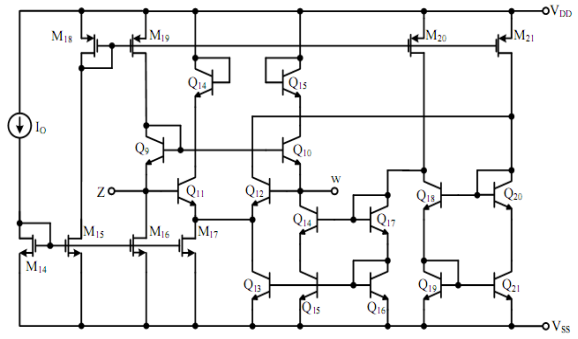
$$K_5 = \frac{g_{m2}g_{m5}g_{m7}}{g_{m6}(g_{m4} + g_{m5})},$$

$$K_6 = \frac{g_{m13}}{g_{m12}}(g_{m6} + g_{m7})$$

and
$$K_7 = \frac{g_{m7}}{g_m 6}(g_{m3} + g_{m8}).$$



(a)



(b)

Fig.5: *A BiCMOS buffered amplifier (a) basic topology (b) modified topology*

If transistors are well matched, which are $g_{m4} = g_{m5}$, $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_{m5} = g_{m6} = g_{m7} = g_{m8}$, $g_{m6} = g_{m7}$, $g_{m10} = g_{m11}$, and $g_{m12} = g_{m13}$. The current at Z terminal can be expressed as

$$I_z = I_p - I_n, \tag{13}$$

This confirms that the circuit in Fig. 4 can function as a current differencing circuit.

The output resistance looking into the z terminals can be expressed as

$$r_z = \frac{r_{ds}}{2}, \tag{14}$$

where r_{ds} is the drain-source resistance seen at the mentioned output terminal.

D. Modified BiCMOS Buffered Amplifier

Conventionally, the basic buffered amplifier can be realized by the circuit shown in Fig. 5(a). It consists of $Q_9 - Q_{11}$ and Q_{14p} which is the translinear loop. From elementary small-signal circuit analysis, the output voltage V_W of this circuit can be expressed as

$$\begin{aligned} V_w &= \left(\frac{g_{m10} + \frac{g_{m10}g_{m11}}{g_{m9}}}{g_{m10} + g_{m14p}} \right) V_z \\ &\quad + \frac{(g_{m11}g_{m10} - g_{m9}g_{m11})}{(g_{m9}g_{m14p} - g_{m11}g_{m10})} I_o. \end{aligned} \tag{15}$$

We can form Eq. (15) to be

E. Completed BiCMOS Current Controlled Current Differencing Buffered Amplifier

The proposed CC-CDBA consists of two principal blocks: a current differencing circuit which has finite input resistances and the modified voltage buffer, as explained. The proposed realization of the CC-CDBA in BiCMOS

$$V_w = \beta V_z + \varepsilon_b, \tag{16}$$

$$\begin{aligned} \text{where} \quad \beta &= \frac{g_{m10} + \frac{g_{m10}g_{m11}}{g_{m9}}}{g_{m10} + g_{m14p}}, \\ \varepsilon_b &= \left(\frac{g_{m11}g_{m10} - g_{m9}g_{m11}}{g_{m9}g_{m14p} - g_{m11}g_{m10}} \right) I_o. \end{aligned}$$

If transistors are well matched, which are $g_{m9} = g_{m10}$ and $g_{m11} = g_{m14p}$, the parameters $\beta \cong 1$ and $\varepsilon_b = 0$. .

However due to the dissymmetry between npn and pnp transistors, this circuit exhibits a high output offset voltage. This problem should be solved by using a novel buffer amplifier, as depicted in Fig. 5(b) [8]. By means of a standard BiCMOS technology, any attempt to design wideband voltage follower will have to avoid MOS and pnp transistors in signal paths. The modified topology is an alternative solution to simulate the traditional class AB voltage follower in a standard BiCMOS technology, in which high frequency pnp bipolar junction transistor is not available.

The output resistance looking into the w terminals is given by

$$r_w = \frac{V_T}{2I_o}. \tag{17}$$

The tunable output resistance of the modified circuit in Eq. (17) will be advantageous to implement low distortion voltage follower. Furthermore, this circuit includes a solution to simulate a pnp transistor in a translinear loop only using high speed npn transistors in signal paths (Q9-Q12). The translinear loop is DC biased by IO using current mirrors (M14-M21).

E. Completed BiCMOS Current Controlled Current Differencing Buffered Amplifier

The proposed CC-CDBA consists of two principal blocks: a current differencing circuit which has finite input resistances and the modified voltage buffer, as explained. The proposed realization of the CC-CDBA in BiCMOS technology is shown in Fig. 6. The circuit implementation consists of mixed translinear loops (Q1-Q6). The mixed loops are DC biased by IB using current mirrors (M1-M4 and M6-M9). The p and n terminal resistances can be obtained by Eq. (2). The output z-terminal that generates the current difference of p and n terminal is realized using CMOS (M5-M7 and M11-M13).

The buffered amplifier is realized using BJTs and CMOS ($Q9 - Q21$ and $M14 - M21$). It should be noted that only npn transistors are employed in this topology. Using a BiCMOS technology, which enables to implement both high speed npn and pnp. A traditional high frequency class AB voltage follower [1], providing better linearity than its equivalent class A structure [1], could be implemented. Unfortunately, such technology requires complex and costly additional mask levels that constrain several companies

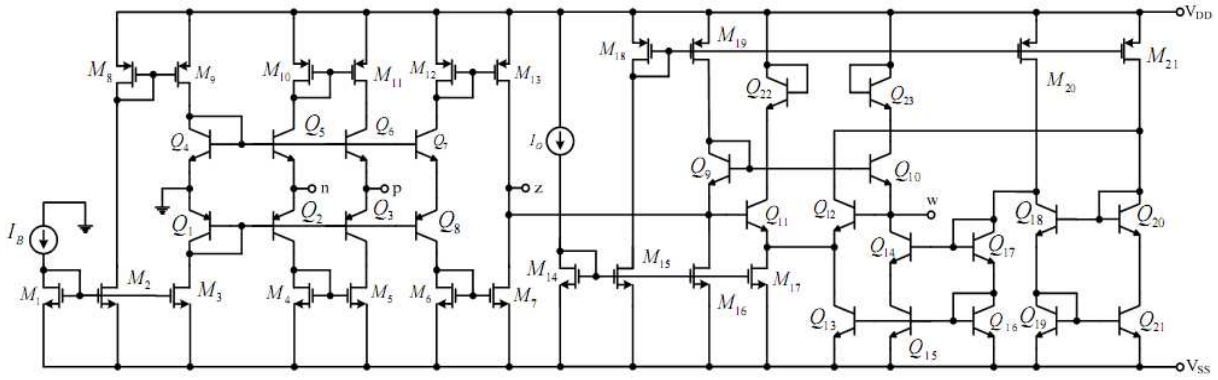


Fig.6: *Proposed BiCMOS current controlled current differencing buffered amplifier*

to use only "standard" BiCMOS technology, which high frequency pnp bipolar junction transistor is not available [8].

3. PERFORMANCE ANALYSIS

A. Area mismatch

From Section II.C, emitter area mismatch errors from transistors will mostly affect the operation of the translinear circuit. For this reason, symmetrical and common centroid layout techniques should be employed for the transistors within the translinear loop. Good layout techniques will also help reduce error due to process and thermal variations [1].

B. Finite output resistance

If the effects of base-width modulation are taken into account, the collector current of the transistor is changed to

$$I_c = I_s e^{V_{BE}/V_T}\left(1+\frac{V_{CE}}{V_A}\right) \tag{18}$$

Thus

$$V_{BE} = V_T \ln[I_C/kI_s], \tag{19}$$

where $k = 1 + V_{CE}/V_A$. The Early voltage effect appears like an area mismatch.

$$V_{BE} = V_T \ln[I_C/kI_s], \tag{20}$$

The intrinsic input resistances with considering the finite output resistances of the transistors are modified to

$$R_n = R_p = \frac{V_T}{2I_{B1}} + \frac{V_T}{I_n}\ln\left(\frac{I_{s4}k_4}{I_{s5}k_5}\right), \tag{21}$$

where $k_1 = 1+V_{CEi}/V_{Ai}$. From Eq. (21), it should be observed that the second term is the error originated from the Early voltage transistor mismatch compared to Eq. (11). Consequently, keeping values of $I_{s4}k_4$ and $I_{s5}k_5$ to be equaled must be strictly considered [1].

C. Finite beta

Errors due to finite β_F occur frequently in translinear circuits, since a bipolar transistor needs to be provided with base current. This base current is often taken directly from an input or output current source, and results in error terms in the circuit transfer function. These β_F errors are due to the circuit implementation, rather than being an inherent error in the translinear circuit principle. Any series base resistance R_{bb} also affects the operation of a transistor circuit, since it ruins the exponential current-voltage relation in such

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_s} + \frac{I_C R_{bb}}{\beta_F}\right). \tag{22}$$

In similar, the intrinsic input resistances with considering the finite beta of the transistors are changed to

$$R_n = R_p = \frac{V_T}{2I_{B1}} + \frac{I_{B1}}{I_{in}}\left(\frac{R_{bb4}}{\beta_{F4}} - \frac{R_{bb5}}{\beta_{F5}}\right), \tag{23}$$

where β_{Fi} is the DC current gain of ith transitor. From Eq. (22), it should be concluded that the second term is the error from finite beta transistor mismatch compared to Eq. (11). Thus, keeping ratio of R_{bb4}/β_{F4} and R_{bb5}/β_{F5} to be equaled is preferred. To simplify the analysis of translinear circuits, it is usual to neglect transistor base currents. However, a full circuit analysis including base current errors is often useful for comparing alternative circuit topologies [1].

4. SIMULATION RESULTS

To prove the performances of the proposed CC-CDBA, the PSPICE simulation program was used for the examination. The PNP and NPN transistors employed in the proposed circuit in Fig. 6

Table 1: *DIMENSIONS OF THE MOSTRANSISTORS*

MOS Transistors	$W(\mu m)/L(\mu m)$
M1-M5, M14-M17, M18-M19	5/0.5
M6-M7	8/1.5
M8-M11	15/0.5
M12-M13	20/0.5
M20-M21	10/0.5

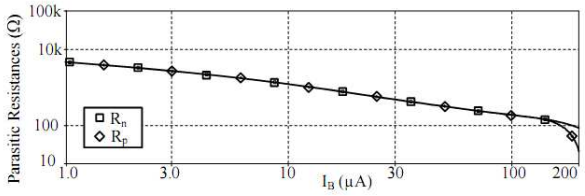


Fig.7: *Parasitic resistances at input terminal relative to I_B*

were simulated by respectively using the parameters of the PR200N and NR200N bipolar transistors of ALA400 transistor array from AT&T [9] The PMOS and NMOS transistors were simulated by using the parameters of a 0.35 μm TSMC CMOS technology [10] with $\pm$1.5V supply voltages and I_o was set to 150 μA. The aspect transistor ratios of PMOS and NMOS are listed in Table I. Fig. 7 depicts the parasitic resistances at p and n input terminals when I_B is varied, it is seen that the controllable parasitic resistances by adjusting I_B are about 1 μA-180 μA ranges.

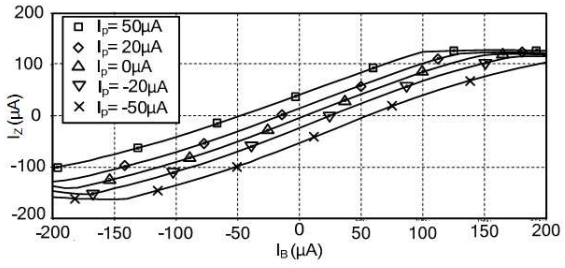


Fig.8: *DC transfer characteristics of BiCMOS CC-CDBA*

Fig. 8 displays DC transfer characteristics of the proposed BiCMOS CC-CDBA, when $I_B = 100\mu A$. So it is clearly seen that it is linear in $-100\mu A \leq I_n(I_p) \leq 100\mu A$ and can be adjusted. Fig. 9 shows compared results of the offset current errors between the proposed CC-CDBA and CC-CDBA from [5] with respect to the input bias current IB, when In and Ip are equal. It is seen that the proposed CC-CDBA provides much lower offset current error. Fig. 10 depicts compared results of the offset voltage errors. It is seen that the proposed BiCMOS CC-CDBA gives much lower voltage offset. Moreover, the bandwidths of output terminals are investigated as shown in Fig. 11. All results are achieved from same device technology implementations.

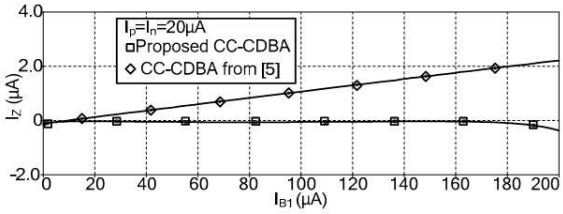


Fig.9: *Compared offset output current errors*

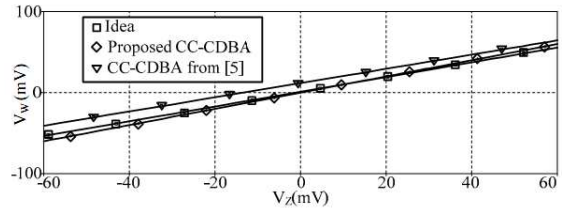


Fig.10: *Compared offset output voltage errors*

The summarized properties of the proposed CC-CDBA compared to the CC-CDBA from [5] can be seen from Table. II. From the results, it can be observed that the proposed CC-CDBA can provide high performance in offset errors. Even it consumes higher power and provides smaller range of frequency responses, this schematic is very suitable for usage in instrumentation and measurement systems. If these factors become necessary, they can be solved by using a modern BiCMOS technology, which is continually developed.

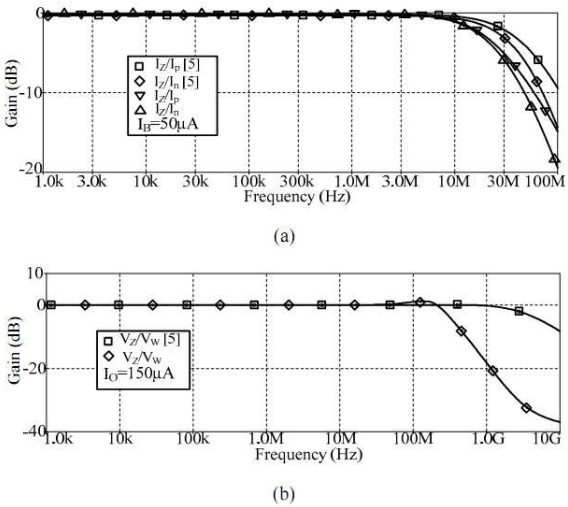


Fig.11: *Frequency responses at output terminals of the CC-CDBAs*

Table 2: *SUMMARIZED OF THE CC-CDBAS PARAMETERS*

Parameters	Proposed CC-CDBA	CC-CDBA from [5]
Power supply voltages	$\pm 1.5V$	$\pm 1.5V$
Power consumptions	5.50mW	3.01mW
-3dB Bandwidths	20.19MHz (Iz/Ip), 18.59MHz (Iz/In), 293.08MHz (Vw/Vz)	38.45MHz (Iz/Ip), 29.44MHz (Iz/In), 3.71GHz (Vw/Vz)
Input current linear ranges (I_B=100μA)	-100μA to 100μA	-110μA to 110μA
R_n and $R_p$ranges	121Ω-8.61kΩ	16.60Ω-13.57kΩ
Input bias current ranges for controlling R_n and R_p	1μA-180μA	1μA-1.4mA
Output offset currents at I_B=100 μA	22.80nA	1.52μA
Output offset voltages at I_O=200 μA	11.13mV	24.24mV
(I_B=100 μA)	64.28kΩ	8.46kΩ
(I_O=200 μA)	84.88Ω	169.34Ω
Switching time delays	40ns	15ns

5. APPLICATION EXAMPLES

A. Current-mode Multiplier/Divider

The multiplier/divider based on the CC-CDBA is shown in Fig. 12 to confirm the usability and to investigate the performances the proposed CC-CDBA and conventional CC-CDBA. From the circuit in Fig. 12, it employs only double CC-CDBA, which contrasts to ordinarily proposed dependence of these errors. As a result, good design of CC-CDBA should be strictly considered to alleviate the effects.

$$I_{z1} = I_A - i_p, \tag{24}$$

and

$$I_{z1} = i_p. \tag{25}$$

From Eq. (24), it result

$$I_{z1} = I_A/2. \tag{26}$$

The output voltage at W_1 terminal can be found as

$$V_{w1} = I_{z1}R_{p1} = I_A\frac{R_{p1}}{2R_{n2}}. \tag{27}$$

The output current can be found as

$$I_O = \frac{V_{w1}}{R_{n2}} = I_A\frac{R_{p1}}{2R_{n2}}. \tag{28}$$

If $R_{p1} = V_T 2I_B$ and $R_{n2} = V_T/2I_C$. The output current in Eq. (28) will be changed as

$$I_O = \frac{I_A I_C}{2I_B}. \tag{29}$$

From Eq. (29), it is clearly seen that IO is a result of either, multiplying of I_A and I_C, or dividing of I_A and I_B. Due to being a positive value of I_B and I_C, the circuit can be a 2 quadrant multiplier/divider.

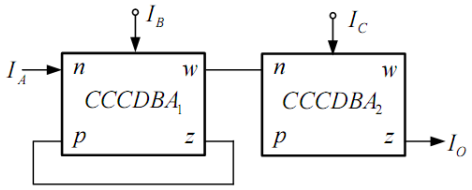


Fig.12: *Multiplier/divider based on the CC-CDBA*

Furthermore, the circuit is theoretically temperature-insensitive owing to the independence from V_T.

In practice, the CC-CDBA is possible to work with non-ideality. Its properties will change to

$$I_z = \alpha_p I_p - \alpha_n I_n + \varepsilon_z \tag{30}$$

and

$$V_w = \beta V_z + \varepsilon_b. \tag{31}$$

α_p, α_n and β are transferred error values deviated from one. While ε_z and ε_b are the offset currents at z and w terminals, respectively. In the case of non-ideal and brief consideration, the IO is changed to

$$I_O = \frac{\beta_{b1}\alpha_{n1}\alpha_{n2}}{1+\alpha_{p1}} \cdot \frac{I_A I_C}{I_B} + \frac{\beta_{b1}\alpha_{n2}\varepsilon_{z1}}{1+\alpha_{p1}} \cdot \frac{I_C}{I_B} + \frac{2I_C\alpha_{n2}\varepsilon_{b1}}{V_T} \tag{32}$$

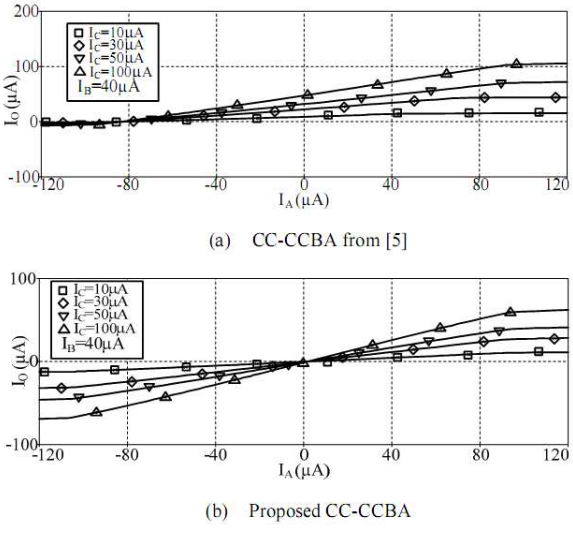


Fig.13: *Static characteristics of the multiplier*

From Eq. (32), we can see that the last two terms are offset currents. So, to reduce the offset currents, the CC-CDBA should be carefully designed to achieve these errors as low as possible. In addition, for the first term, these errors affect the magnitude

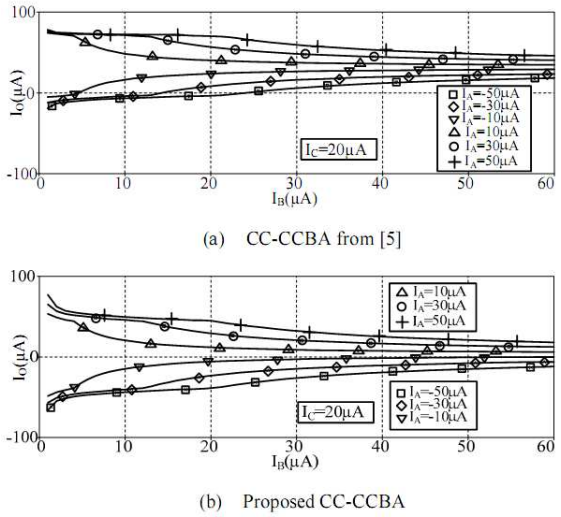


Fig.14: *Static characteristics of the divider*

of the output current. The magnitude output slightly depends on temperature due to temperature dependence of these errors. As a result, good design of CC-CDBA should be strictly considered to alleviate the effects.

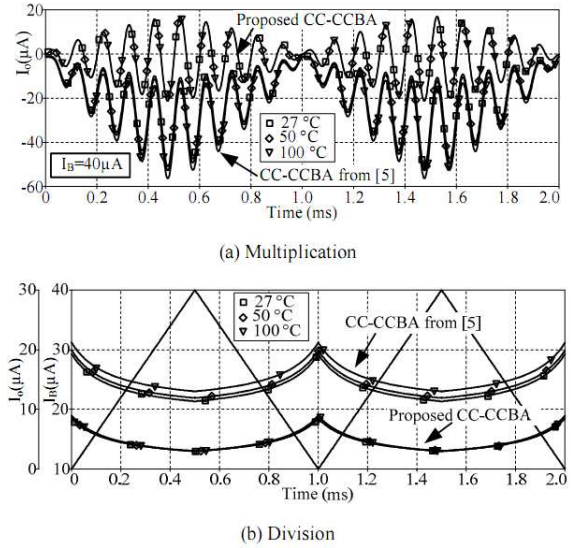


Fig.15: *Transient responses of the multiplier/divider implemented from proposed CC-CDBA and CC-CDBA from [5]*

Fig. 13 shows compared results of the DC response characteristics of multiplication for the CC-CDBA implemented in [5] and proposed CC-CDBA structure, where I_B=40μA. Fig. 14 show results of the DC response characteristics of division implemented by the proposed CC-CDBA and the CC-CDBA realized in [5], where I_C=20μA. From these results, it can be concluded here that, with the same configuration, the circuit implemented by the proposed CC-CDBA provides high performance in offset issue superior to

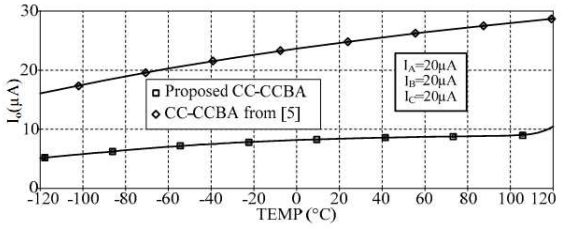


Fig.16: *Output current deviations due to temperature variations*

realization from conventional CC-CDBA.

Fig. 15(a) shows the transient responses of multiplier results realized by proposed CC-CDBA compared to those by CC-CDBA in [5], where I_A and I_C were set to be a sinusoidal signal 40μA_{p-p} with a 10kHz and triangular signal 50μA_p with a 1kHz frequency, respectively. Fig. 15(b) shows divider results of the circuit implemented by proposed CC-CDBA compared to those by CC-CDBA in [5], where I_A and I_C were set to be 20μA and 10μA and was a triangular signal with frequency of 1kHz. Furthermore, the claimed temperature-insensitivities of the multiplier/divider realized by the proposed element compared to those by CC-CDBA in [5] are confirmed by the results of Fig. 16. The results show that the circuit implemented by the proposed element provides good temperature stability and offset performances much better than those by the conventional CC-CDBA.

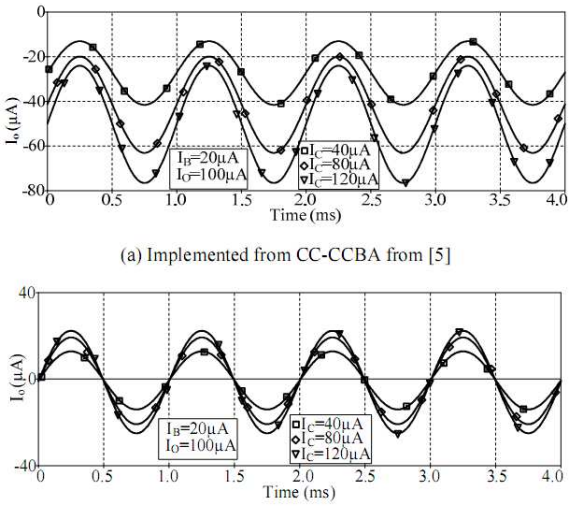


Fig.17: *Output currents for different IC of current amplifier*

B. Current Amplifier

From the circuit in Fig. 12, in addition, if IA is an input current, the circuit can work as a current amplifier, the magnitude of output current can be controlled by I_B and I_C. The compared results

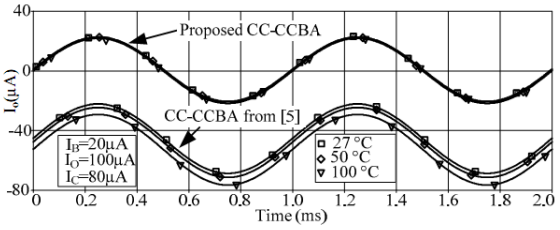


Fig.18: *Output currents for temperature variations*

in Fig. 17 clearly confirm that the current amplifier implemented from the proposed CC-CDBA achieves much less offset level than the circuit realized by CC-CDBA in [5]. The total harmonic distortions (THDs) obtained from the circuits implemented by the proposed element and element in [5] at 10MHz are 2.88% and 5.97%, respectively.

The compared results of output currents for temperature variations obtained from the current amplifier are depicted in Fig. 18. It can be clearly seen that the circuit implemented from proposed building block provides good temperature performances much better than implementation by the traditional building block.

6. CONCLUSIONS

The building block, called BiCMOS CC-CDBA, has been introduced via this paper. The usabilities have been proven by the simulation and application examples. From the obtained results, they provide good performances superior to implementations from traditional CC-CDBA, this is due to careful design of the proposed CC-CDBA, as explained in the papert. The proposed CC-CDBA provides low distortions, low output offset errors and good temperature performances. It is very appropriate to realize in commercially-purposed integrated circuit for employing in instrumentation/measurement systems, battery-powered, portable electronic equipments or wireless communication systems. Our future work is to present more useable applications of this element such as filter, precision rectifier, oscillator, etc.

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