Digital Robust Control for DC-DC Converter with Second-Order Differential Characteristics

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ABSTRACT

Robust DC-DC converter which can covers extensive load changes and also input voltage changes with one controller is needed. The demand to suppressing output voltage changes becomes still severer. We proposed an approximate 2DOF digital controller which realizes the startup response and dynamic load response independently. The controller makes the control bandwidth wider, and at the same time makes a variation of the output voltage small at sudden changes of loads and input voltages. In this paper, a new approximate 2DOF digital control system with additional zeros is proposed. Using additinal zeros second-order differential transfer characteristics between equivalent disturbances and an output voltage are realized. Therefore the new controller makes variations of the output voltage smalerl at sudden changes of loads and input voltages. This controller is actually implemented on a DSP and is connected to a DC-DC converter. Experimental studies demonstrate that this type of digital controller can satisfy given severe specifications.

Keywords: DC-DC converter, Approximate 2DOF, Second-order differential, Digital robust control

1. INTRODUCTION

In many applications of DC-DC converters, loads cannot be specified in advance, i.e., their amplitudes are suddenly changed from the zero to the maximum rating. Generally, design conditions are changed for each load and then each controller is re-designed. Then, a so-called robust DC-DC converter which can cover such extensive load changes and also input voltage changes with one controller is needed. Analog control IC is used usually for control of DC-DC converter. Simple integral control etc. are performed with the analog control IC. Moreover, the application of the digital controller to DC-DC converters designed by the PID or root locus method etc. has been recently considered[1], [2]. However, it is difficult to retain sufficient robustness of DC-DC converters by these techniques. Various robust control methods for improving start-up characteristics and load sudden change characteristics of DC-DC converters are proposed[3], [4], [5], [6], [7]. However, they take tens [ms] for the rise time of the startup responses, and hundreds [mV] output voltage regulations have arisen in the load sudden changes. The demand for suppressing output voltage change becomes still severer, and the further improvements to startup characteristics and load sudden change characteristics are required. The authors proposed the method of designing an approximate 2-degree-of-freedom (2DOF) controller of DC-DC converter[8], [9], [10], [11]. This controller realized first-order differential transfer characteristics between equivalent disturbances and an output voltage. Therefore, there is a limit in suppressing the output voltage variation, and the variation was not able to be made smaller.

In this paper, we propose a new approximate 2DOF digital controller which realizes second-order differential transfer characteristics[12], [13]. These characteristics are realized by introducing additional zeros into transfer functions between equivalent disturbances and the output. The new controller makes the variations of the output voltage smaller than the former controller[11] at sudden changes of resistive loads and input voltages. A new DC-DC converter equipped with the proposed controller in DSP is actually manufactured. Some simulations and experiments show that this new DC-DC converter can satisfy given severe specifications.

The DC-DC converter as shown in Fig.1 has been manufactured. In order to realize the approximate 2DOF digital controller which satisfies given specifications, we use the DSP(TI TMS320LF2801). This DSP has a builtin AD converter and a PWM switching signal generating part. The triangular wave carrier is adopted for the PWM switching signal. The switching frequency is set at 400[KHz] and the peak-to-peak amplitude C_m is 125[V]. The LC circuit is a filter for removing carrier and switching noises. where
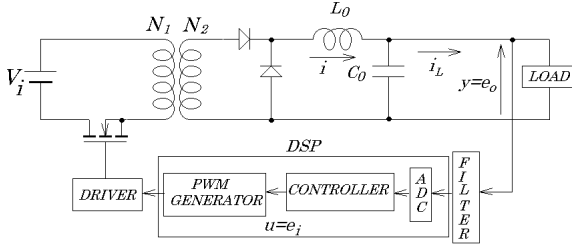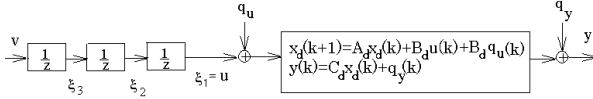
Fig.1: *DC-DC converter*

Fig.2: *Controlled object with 3 input delay elements*

C_0 is $300[\mu F]$ and L_0 is $0.46[\mu H]$. If the frequency of control signal u is smaller enough than that of the carrier, the state equation of the DC-DC converter at a resistive load in Fig.1 except the controller in DSP can be expressed from the state equalizing method[14] as follows:

$$\begin{cases} \dot{x} = A_c x + B_c u + B_c q_u \\ y = C_x + q_y \end{cases} \quad (1)$$

where

$$x = \begin{bmatrix} e_0 \\ i \end{bmatrix} \quad A_c = \begin{bmatrix} -\frac{1}{C_0 R_L} & \frac{1}{C_0} \\ -\frac{1}{L_0} & -\frac{R_1}{L_0} \end{bmatrix} \quad B_c = \begin{bmatrix} 0 \\ \frac{k_p}{L_0} \end{bmatrix}$$

$$c = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad u = e_i \quad y = e_0 \quad k_p = -\frac{V_i N_2}{C_m N_1}$$

and R_0 is the total resistance of coil and ON resistance of FET, etc., whose value is $0.015[\Omega]$. Then the discrete-time state equation of the system (1) with a zero-order hold is expressed as

$$\begin{cases} x_d(k+1) = A_d x_d(k) + B_d u(k) + B_d q_u(k) \\ y_k = C x_d(k) + q_y(k) \end{cases} \quad (2)$$

where

$$A_d = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} = e^{A_c T}, B_d = \begin{bmatrix} b_{11} \\ b_{21} \end{bmatrix} = \int_0^T e^{A_c \tau} B_c d_\tau$$

The transfer function of the system (2) is as follows:

$$G_p(z) = \frac{N_p(z)}{D_p(z)} \quad (3)$$

where
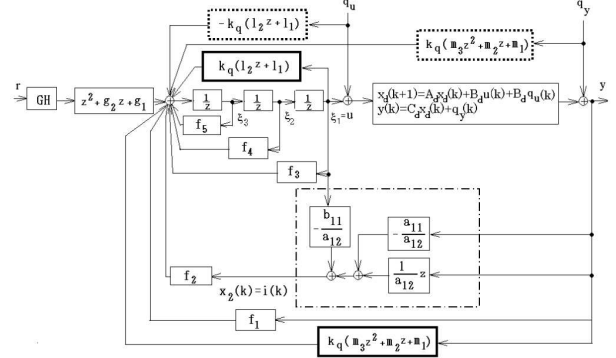
$$N_p(z) = b_{11} z + b_{21} a_{12} - a_{22} b_{11}$$

Fig.3: *Feedforward from equivalent disturbances q_u and q_y, and model matching with state feedback*
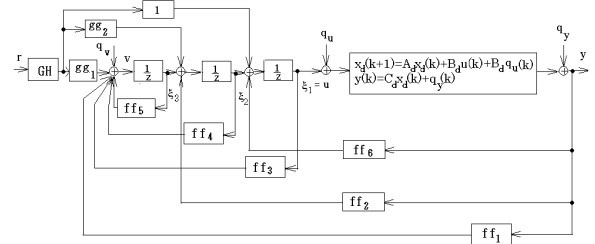

Fig.4: *Model matching system using only voltage (output) feedback*

$$D_p(z) = z^2 - (a_{11} + a_{22})z + a_{11} a_{22} - a_{21} a_{12}$$

For practical use of DC-DC converters, the characteristics of startup transient response, dynamic load responses and output responses at sudden input voltage changes are important. The DC-DC converter with the following specifications 1-7 is designed and manufactured:

1. Input voltage V_i is 48[V] and output voltage e_o is 3.3[V].
2. Startup transient responses are almost the same at resistive load and parallel load of resistance and capacity, where $0.16 \leq R_L < \infty[\Omega]$ and $0 \leq C_L \leq 300[\mu F]$.
3. The rising time of the startup transient response is smaller than $100[\mu s]$.
4. Against all the loads of spec.1, an over-shoot is not allowable in the startup transient response.
5. The dynamic load response is smaller than 25[mV] against 10[A] change of load current.
6. The specs. 2, 3, 4 and 5 are satisfied also to change of input voltage of $\pm 20\%$.
7. Regulation of output voltage is smaller than 25[mV] at the sudden change of input voltage within $\pm 20\%$.

Specs 2, 5 and 7 are new ones. These specs are more severe than $200[\mu F]$ and 50[mV] in references[11]. The load changes for the controlled object
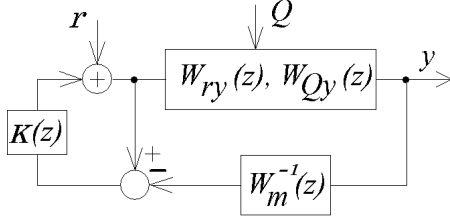
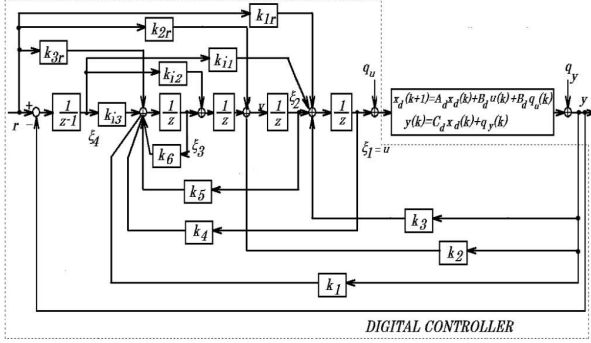**Fig.5:** *System reconstituted with inverse system and filter*

Fig.6: *Approximate 2DOF digital integral type control system*

and the input voltage change are considered as parameter changes in eq.(1). Such parameter changes can be transformed to equivalent disturbances q_u and q_y as shown in **Fig.2** and **Fig.3**[15] even in discrete-time systems. Therefore, what is necessary is just to constitute the control systems whose pulse transfer functions from equivalent disturbances q_u and q_y to the output y become as small as possible in their amplitudes, in order to robustize or suppress the influence of these parameter changes and input voltage changes.

2. DESIGN METHOD FOR APPROXIMATE 2DOF DIGITAL CONTROLLER WITH ADDITIONAL ZEROS

A. Addtional zeros method

The following equation is obtained by repeating the difference of the output of eq.(2):

$$Y = O^* xd(k) + U\bar{u}(k) + U\bar{q}_u + \bar{q}_y \qquad (4)$$

where

$$Y = \begin{bmatrix} y(k) \\ y(k+1) \\ y(k+2) \end{bmatrix} O^* = \begin{bmatrix} C \\ CA_d \\ CA_d^2 \end{bmatrix} U = \begin{bmatrix} 0 & 0 \\ CB_d & 0 \\ CA_dB_d & CB_d \end{bmatrix}$$

$$\bar{u} = \begin{bmatrix} u(k) \\ u(k+1) \end{bmatrix} \bar{q}_u = \begin{bmatrix} q_u(k) \\ q_u(k+1) \end{bmatrix} \bar{q}_y = \begin{bmatrix} q_y(k) \\ q_y(k+1) \\ q_y(k+1) \end{bmatrix}$$

If both sides of eq.(4) are mulutiplied by $\bar{I}_2$ from the left, x_d is obtained by the following equation:

$$
\begin{aligned}
x_d(k) &= (\bar{I}_2 O^*)^{-1}\bar{I}_2 Y - (\bar{I}_2 O^*)^{-1}\bar{I}_2 U\bar{u}(k) \\
&\quad - (\bar{I}_2 O^*)^{-1}\bar{I}_2 U\bar{q}_u - (\bar{I}_2 O^*)^{-1}\bar{I}_2\bar{q}y \quad (5)
\end{aligned}
$$

where

$$\bar{I}_2 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$$

By substituting the above equation into eq.(4), the following equation is obtained:

$$
\begin{aligned}
(I_3 - O^*(\bar{I}_2 O^*)^{-1}\bar{I}_2)U\bar{q}_u &+ (I_3 - O^*(\bar{I}_2 O^*)^{-1}\bar{I}_2)\bar{q}_y \\
= (I_3 - O^*(\bar{I}_2 O^*)^{-1}\bar{I}_2)Y &- (I_3 - O^*(\bar{I}_2 O^*)^{-1}\bar{I}_2)U\bar{u} \quad (6)
\end{aligned}
$$

where I3 is a 3×3 unit matrix. That is, $\bar{q}_u$ and $\bar{q}_y$ can be replaceed to Y and $\bar{u}(k)$. Eq.(6) is transformed as

$$
\begin{aligned}
&- (l_2 z + l_1)q_u(k) + (z^2 + m_2 z + m_1)q_y(k) \\
&= (l_2 z + l_1)u(k) + (z^2 + m_2 z + m_1)y(k) \quad (7)
\end{aligned}
$$

where

$$
\begin{aligned}
\begin{bmatrix} l_1 & l_2 \end{bmatrix} &= -(I_3 - O^*(\bar{I}_2 O^*)^{-1}\bar{I}_2)U \\
\begin{bmatrix} m_1 & m_2 & m_3 \end{bmatrix} &= (I_3 - O^*(\bar{I}_2 O^*)^{-1}\bar{I}_2) \quad (8)
\end{aligned}
$$

The system as depicted in Fig.2 is constituted in consideration of a delay time for AD conversion time etc., replacing current feedback and zeros addition. The state equation in Fig.2 can be expressed as

$$
\begin{cases}
x_{dw}(k+1) = A_{dw}x_{dw}(k) + B_{dw}v(k) \\
y(k) = C_{dw}x_{dw}(k)
\end{cases} \quad (9)
$$

where

$$x_{dw}(k) = \begin{bmatrix} x_d(k) \\ \xi_1(k) \\ \xi_2(k) \\ \xi_3(k) \end{bmatrix} A_{dw} = \begin{bmatrix} A_d & B_d & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

$$B_{dw} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix} C_{dw} = [C \ 0 \ 0 \ 0] \xi_1(k) = u(k)$$

Applying the following feedforwards from q_u, q_y and r, and state feedback from xdw for model matching to the system in eq.(9), the system shown in Fig.3 is obtained.

$$v(k) = -k_g(l_2z + l_1)q_u(k) + k_q(z^2 + m_2z + m_1)q_y(k)$$
$$+ (z^2 + g_2z + g_1)r(k) + [f_1\ f_2\ f_3\ f_4\ f_5\ f_6]\,x_dw(k) \quad (10)$$

In Fig.3, the parts surrounded by dotted lines are the feedforward coefficients from q_u and q_y and the part surrounded by a chain line is the estimated part of current. From eq.(7), the feedforwards of eq.(10) are changed as

$$v(k) = k_q(l_2z + l_1)u(k) + k_q(z^2 + m_2Z + m1)q_y(k)$$
$$+ (z^2 + g_2z + g_1)r(k) + [f_1\ f_2\ f_3\ f_4\ f_5\ f_6]x_{dw}(k) \quad (11)$$

That is, the parts surrounded by the dotted lines are replaced by the parts surrounded by solid lines from u and y. The system except the parts surrounded by the dotted lines in Fig.3 can be transformed equivalently as shown in **Fig.4**. In Fig.4,

$$ff_1 = f_1 - f_2(a_{11}/a_{12}) + k_qm_1 + f_5(k_qm_2 + f_2/a_{12})$$
$$+\ f_5^2k_qm_3 + (f_4 + k_ql_2)k_qm_3$$
$$ff_2 = k_qm_2 + f_2/a_{12} + f_5k_qm_3$$
$$ff_3 = f_3 - f_2(b_{11}/a_{12}) + k_ql_1$$
$$ff_4 = f_4 + k_ql_2$$
$$ff_5 = f_5$$
$$ff_6 = k_qm_3 \quad (12)$$

The transfer functions between r and y, q_u and y, and q_y and y in Fig.4 are described as

$$W_{ry}(z) = N_{ry}(z)/D(z) \quad (13)$$

$$W_{q_uy}(z) = N_{q_uy}(z)/D(z) \quad (14)$$

$$WW_{q_yy}(z) = N_{q_yy}(z)/D(z) \quad (15)$$

where

$$N_{ry}(z) = GH(z^2 + g_1z + g_0)(b_{11}z + b_{21}a_{12} - a_{22}b_{11})$$
$$N_{q_uy}(z) = N_{qz}N_p$$
$$N_{q_uy}(z) = N_{qz}D_p$$
$$N_{qz} = (a_{12}z^3 - a_{12}f_5z^2 + (a_{12}b_{11}k_q - a_{12}b_{11})z$$
$$-\ f_3a_{12} - f_2b_{11} - a_{12}a_{22}b_{11}k_q - a_{12}^2b_{21}k_q)$$
$$D(z) = z^5 + (-f_5 - a_{22} - a_{11})z^4 + (a_{11}f_5$$
$$+\ a_{11}a_{22} - a_{21}a_{12} + a_{22}f_5 - f_4)z^3$$
$$+\ (a_{21}a_{12}f_5 - f_3 + a_{11}f_4 - a_{11}a_{22}f_5$$
$$+\ a_{22}2f_4)z^2 + (a_{22}f_3 + a_{21}a_{12}f_4 + a_{11}f_3$$
$$-\ b_{11}f_1 - f_2b_{21} - a_{11}a_{22}f_4)z + f_2a_{11}b_{21}$$
$$-\ a_{21}f_2b_{11} + a_{21}a_{12}f_3 + f_1a_{22}b_{11}$$
$$-\ f_1a_{12}b_{21} - a_{11}a_{22}f_3$$

From $D(z)$, the poles of the overall system can be arranged arbitrarily by f_1, f_2, f_3, f_4 and f_5. From $N_{ry}(z)$, two zeros of r-y can be arranged arbitrarily by g0 and g1. Moreover, from common N_{qz} in N_{qz} (s) and $N_{q_yy}(s)$, one zeros of q_u-y and q_y - y can be arranged arbitrarily at the same place by k_q. That is, one zeros can be added arbitrarily to W_{Q_y}.

B. Design method

First, the transfer function between the reference input r and the output y is specified as

$$W_{ry}(z) = N_H(z)/D_H(z) \quad (16)$$

where

$$N_H(z) = (1 + H_1)(1 + H_2(1 + H_3)(z - n_1)(z - n_2)$$
$$\times (z + H_4)(z + H_5)$$
$$D_H(z) = (1 - n_1)(1 - n_2)(z + H_1)(z + H_2)(z + H_3)$$
$$\times (z + H_4)(z + H_5)$$

n_1 and n_2 are the zeros for the discrete-time controlled object (2). $[f_1f_2f_3f_4f_5]$, $[g_1g_2]$ and GH are determined so that $W_{ry}(z)$ becomes eq.(16). And the transfer function among the disturbance inputs q_u, q_y and the output y is specified as

$$W_{q_uy}(z) = (z - 1)\bar{N}_{qz}N_p/D_H(z) \quad (17)$$
$$W_{q_uy}(z) = (z - 1)\bar{N}_{qz}D_p/D_H(z) \quad (18)$$

Here the zeros are placed at 1 by setting k_q as the solution of $N_{qz}(1) = 0$. The parameter k_q becomes as follows:

$$k_q = \frac{-a_{12} + a_{12}f_5 + a_{12}f_4 + f_3a_{12} - f_2b_{11}}{a_{12}(b_{11} - a_{22}b_{11} + b_{21}a_{12})} \quad (19)$$

$\bar{N}_{qz}$ is the remaining zeros of N_{qz} which cannot be placed arbitrarily.

It shall be specified that the relation of H_1 and H_2, H_3 becomes $|H_1| \gg |Re(H_2)|$, $|H_1| \gg |Re(H_3)|$. Then $W_{ry}(z)$ can be approximated to the following first-order model:

$$W_{ry}(z) \approx W_m(z) = \frac{1 + H_1}{z + H_1} \quad (20)$$

This target characteristics $W_{ry}(z) \approx W_m(z)$ is specified so as to satisfy the specs.3 and 4.

The system added the inverse system and the filter to the system in Fig.4 is constituted as shown in **Fig.5**. In Fig.5, the transfer function $K(z)$ becomes

$$K_z = \frac{k_z}{z - 1 + k_z} \quad (21)$$

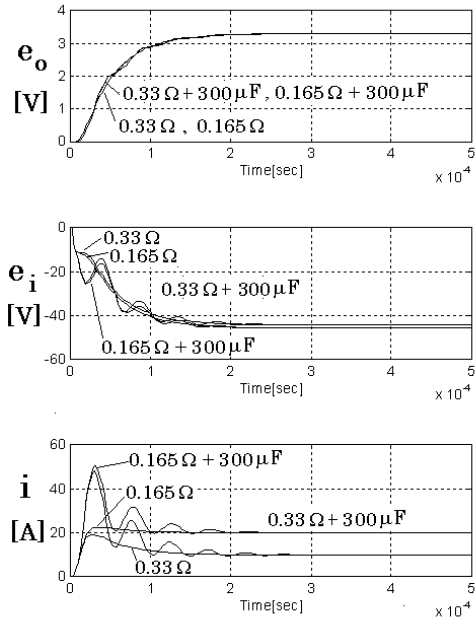The transfer functions between $r - y$, $q_u - y$ and $q_y - y$ of the system in Fig.5 are given by

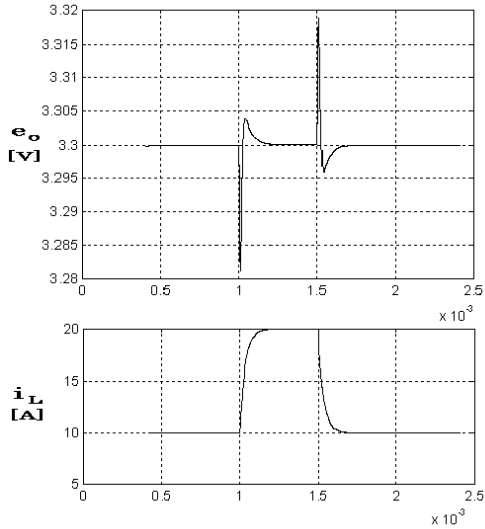**Fig.7:** *Simulation results of the startup responses at various loads*

Fig.8: *Simulation result of the dynamic load response at resistive load*

$$y \;\; = \;\; \frac{1+H_1}{z+H_1} \frac{z-1+k_z}{z-1+k_z W_s(z)} W_s(z) r \qquad (22)$$

$$y \;\; = \;\; \frac{(z-1)^2}{z-1+k_2} \frac{z-1+k_z}{z-1+k_z W_s(z)} \frac{\bar{N}_{qz} N_p}{D_H(z)} q_u \quad (23)$$

$$y \;\; = \;\; \frac{(z-1)^2}{z-1+k_2} \frac{z-1+k_z}{z-1+k_z W_s(z)} \frac{\bar{N}_{qz} D_p}{D_H(z)} q_u \quad (24)$$
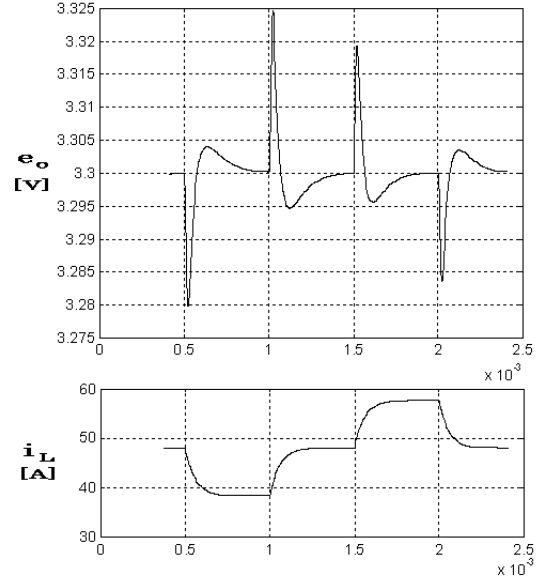

Fig.9: *Simulation result of the output response at resistive load when the input voltage changing suddenly*
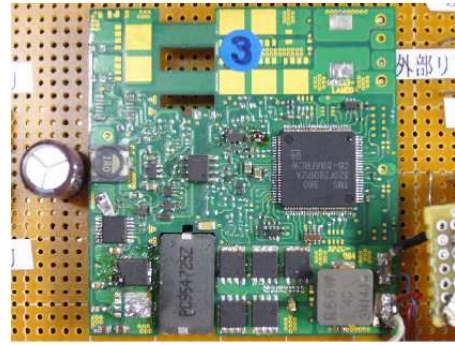

Fig.10: *The manufactured new quarter brick DC-DC converter*

where

$$W_s(z) = \frac{(1+H_2)(1+H_3)(z-n_1)(z-n_2)}{(z+H_2)(z+H_3)(1-n_1)(1-n_2)} \quad (25)$$

Here, if $W_s(z) \approx 1$, then eqs.(22), (23) and (24) become, respectively,

$$y \;\; \approx \;\; \frac{1+H_1}{z+H_1} r \qquad (26)$$

$$y \;\; \approx \;\; \frac{(z-1)^2}{z-1+k_z} \frac{\bar{N}_{qz} N_p}{D_H(z)} q_u \qquad (27)$$

$$y \;\; \approx \;\; \frac{(z-1)^2}{z-1+k_z} \frac{\bar{N}_{qz} D_p}{D_H(z)} q_y \qquad (28)$$

From eqs.(26), (27) and (28), it turns out that the characteristics from r to y can be specified with H_1, and the characteristics from q_u and q_y to y can be

independently specified with k_z. That is, the system in Fig.5 is an approximate 2DOF, and its sensitivity against disturbances becomes lower with the increase of k_z.

If an equivalent conversion of the controller in Fig.5 is carried out, the approximate 2DOF digital integral-type control systems will be obtained as shown in **Fig.6**. In Fig.6, the parameters of the controller are as follows:

$$
\begin{aligned}
k_1 &= (f_1 - f_2 a_{11}/a_{12} + k_q(-a_{11}^2 - a_{21}a_{12} + a_{12}a_{11} \\
&\quad + a_{12}a_{22})a_{11}/a_{12} + f_5(-k_q(a_{12}a_{11} \\
&\quad + a_{12}a_{22})/a_{12} + f_2/a_{12}) + f_5^2 k_q + (f_4 - k_q b_{11})k) \\
&\quad - GHk_z(g_0 + (g_1 + f_5)f_5 + f_4 - k_q b_{11})/(1+H2) \\
k_2 &= k_q - GHk_z/(1 + H2) \\
k_3 &= -k_q(a_{11}a_{12} + a_{12}a_{22})/a_{12} + f_2/a_{12} + f_5 k_q \\
&\quad - (g1 + f_5)GHk_z/(1 + H2) \\
k_4 &= f_3 - f_2 b_{11}/a_{12} + k_q((a_{12}a_{11} \\
&\quad + a_{12}a_{22})b_{11}/a_{12} - a_{11}b_{11} - b_{21}a_{12}) \\
k_5 &= f_4 - k_q b_{11} \\
k_6 &= f_5 \\
k_i 1 &= (g_0 + (g_1 + f_5)f_5 + f_4 - k_q b_{11})GHk_z \\
k_i 2 &= (g1 + f_5)GHk_z \\
k_i 3 &= GHk_z \\
k_1 r &= GH \\
k_2 r &= (g1 + f_5)GH \\
k_3 r &= (g0 + (g1 + f_5)f_5 + f_4 - k_{b11})GH
\end{aligned}
\tag{29}
$$

3. EXPERIMENTAL STUDIES

The sampling period T are set at $2.5[\mu s]$. The nominal value of R_L is $0.33[\Omega]$. We design a control system so that all the specifications are satisfied. First of all, in order to satisfy the specification on the rising time of the startup transient response, H_1, H_2, H_3, H_4 and H_5 are specified as

$$
\begin{aligned}
H_1 &= -0.94 H_2 = -0.18 + 0.2i H_3 = -0.18 - 0.2i \\
H_4 &= -0.2 + 0.3i H_5 = -0.2 - 0.3i
\end{aligned}
\tag{30}
$$

Then from eq.(19), $k_q = 548.31$. After that, k_z is set up with $k_z = 0.17$. Then the parameters of controller become as follows:

$$
\begin{aligned}
k_1 &= 861.86 \quad k_2 = 584.67 \quad k_3 = -1061.2 \\
k_4 &= 0.72688 \quad k_5 = 0.45193 \quad k_6 = -0.178811 \\
k_{i1} &= -1.4955 \quad k_{i2} = 1.2629 \quad k_{i3} = -2.1818
\end{aligned}
\tag{31}
$$

It must be better that k_{r1} and k_{r2} are set to 0, since the characteristics of the control system hardly changes in this case.
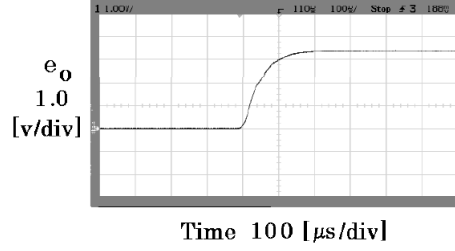

Fig.11: *Experimental result of the startup response at resistive load ($R_L = 0.33[\Omega]$)*
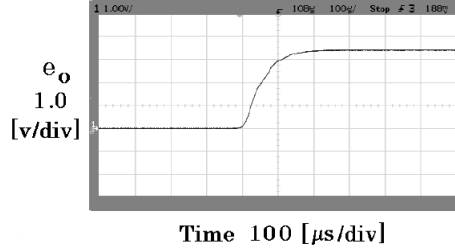

Fig.12: *Experimental result of the startup response at resistive load ($R_L = 0.165[\Omega]$)*

The simulation results of the startup responses are shown in **Fig.7**. From the output voltage $y = e_o$ in this figure, it turns out that the specifications are satisfied. It is checked that almost the same simulation results as in Fig.7 are obtained when the input voltage Vi is changed by $\pm 20\%$. The simulation result of the dynamic load responses is shown in **Fig.8**. Fig.8 shows the result at resistive load whose value is changed as $R_L = 0.33 \leftrightarrow 0.165[\Omega]$. It is checked that almost the same simulation result as in Fig.8 is obtained at parallel load of resistance ($RL = 0.33 \rightarrow 0.165[\Omega]$) and capacity ($CL = 300[\mu F]$). Fig.9 shows the output response at resistive load $R_L = 0.33[\Omega]$ when input voltage changed suddenly as $48 \rightarrow 38 \rightarrow 48 \rightarrow 58 \rightarrow 48[V]$. It turns out that all the specifications are satisfied.
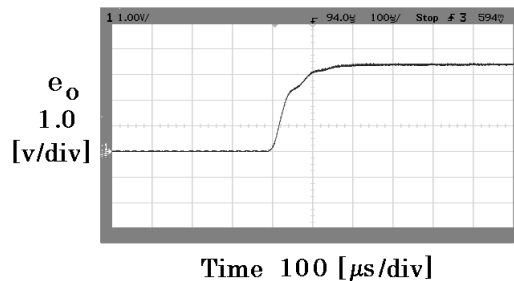

Fig.13: *Experimental result of the startup response at parallel load of resistance ($R_L = 0.33[\Omega]$) and capacity ($C_L = 300[\mu F]$)*
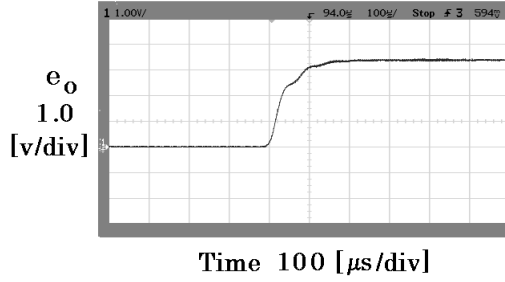
Fig.14: *Experimental result of the startup response at resistive load ($R_L = 0.33[\Omega]$, $C_L = 300[\mu F]$) when the input voltage is 58[V]*
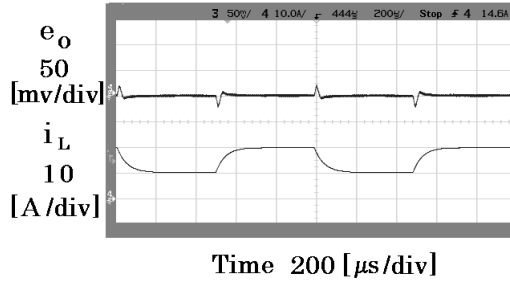

Fig.15: *Experimental result of the dynamic load response at resistive load ($RL = 0.33 \leftrightarrow 0.165[\Omega]$)*

The manufactured, new DC-DC converter built-in DSP is shown in **Fig.10**. This fits in a quarter brick size (37mm × 58mm × 8mm) one. Experimental results when the digital controller with the parameters of eq.(31) is equipped in the DSP shown in **Figs.11-18**. Fig.11 shows the startup response at the resistive load $R_L = 0.33[\Omega]$. Fig.12 shows the startup response at the resistive load $R_L = 0.165[\Omega]$. Fig.13 shows the startup response at parallel load of resistance $R_L = 0.33[\Omega]$ and capacity $CL = 300[\mu F]$. From y = eo in these figures, it turns out that almost the same experimental results as the simulation ones in Fig.7 are obtained and the specifications are satisfied. Fig.14 shows the startup response when the input voltage V_i is 58[V]. It is checked that the specifications are satisfied when the input voltage Vi is
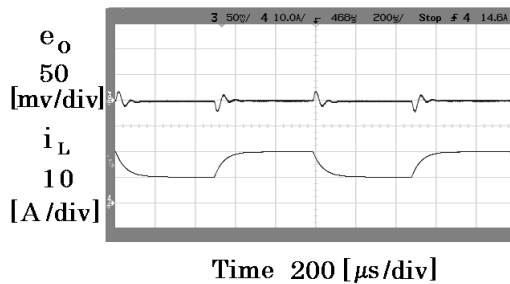

Fig.16: *Experimental result of the dynamic load response at resistive load ($R_L = 0.33 \leftrightarrow 0.165[\Omega]$, $C_L = 300[\mu F]$)*
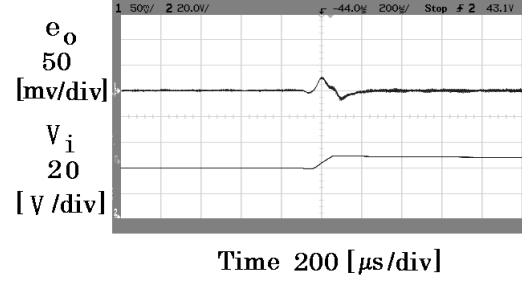

Fig.17: *Experimental result of the output repones at parallel load of resistance ($R_L = 0.33[\Omega]$) and capacity ($C_L = 300[\mu F]$) when input voltage changing suddenly from 38[V] to 48[V]*

Fig.18: *Experimental result of the output repones at parallel load of resistance ($R_L = 0.33[\Omega]$) and capacity ($CL = 300[\mu F]$) when input voltage changing suddenly from 48[V] to 58[V]*

changed by 20%. Fig.15 shows the dynamic load response at resistive load ($RL = 0.33 \leftrightarrow 0.165[\Omega]$). Fig.16 shows the dynamic load response at the parallel load of resistance ($RL = 0.33 \leftrightarrow 0.165[\Omega]$) and capacity ($CL = 300[\mu F]$). It turns out that almost the same experimental results as the simulation ones in Fig.8 are obtained. Although the load current changed suddenly from 20 [A] to 10 [A], and vice versa, the output voltage change is very small and is suppressed within about 25[mV]. Fig.17 shows the output response at parallel load of resistance ($R_L = 0.33[\Omega]$) and capacity ($C_L = 300[\mu 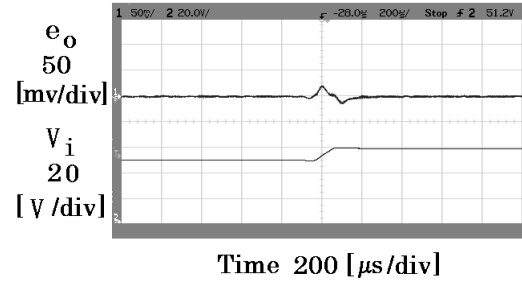F]$) when input voltage changed suddenly from 38[V] to 48[V]. Fig.18 shows the output response at parallel load of resistance ($RL = 0.33[\Omega]$) and capacity ($C_L = 300[\mu F]$) when the input voltage changed suddenly from 48[V] to 58[V]. It turns out that almost the same experimental results as the simulation ones in Fig.9 are obtained. It is checked that almost the same experimental results as Fig.9 are obtained when the input voltage changed suddenly from 48[V] to 58[V]. It turns out that the specifications are satisfied. We checked by experiments that all other specifications are satisfied.

4. CONCLUSIONS

In this paper, the concept of controller of DC-DC converters to attain good robustness against extensive load changes and input voltage changes was given. The proposed digital controller was implemented on the DSP(TI TMS320LF2801). The new DC-DC converter built-in this DSP was manufactured. It was shown from experiments that the sufficiently robust digital controller is realizable. The characteristics of the dynamic load responses and the output responses against sudden input voltage changes were improved by using our proposed method for approximate 2DOF digital controller with additional zeros. This fact demonstrates the usefulness and practicality of our method. The future work is to design a digital controller robust enough, when (LC+LC) circuits etc. are used as filters for removal of switching and carrier noises.

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