Automatic Multi-Operation Bumpless Mode Switching Type Digital Controller for PWM Power Amplifier Using Load Estimation

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ABSTRACT

Robust PWM power amplifiers whose transient response characteristics do not deteriorate against an extensive load change and/or direct-current power-supply voltage change are needed. A digital robust controller with bumpless mode switching for PWM power amplifiers which can satisfy such demands has been proposed. In this paper a multi-stage switching type digital controller is proposed for spreading capacitance load range more and improving transient characteristics for inductance load. In the previous proposed controller, the configuration of the controller is the same to all loads. At inductance load, there is a possibility that the transient characteristics may become bad and the specification may not be satisfied. Therefore, a load current is estimated at inductance load, and the controller which also uses load current for feedback is configured. A inductance is estimated and a controller is switched to this controller bumplessly. In order to extend the range of capacitance load, a controller is increased from two stage to three stage, and these are switched to each other bumplessly. A DSP is implemented to this digital controller. It is demonstrated from experiments that the multi-stage switching type digital controller is realizable and the given specifications are satisfied.

Keywords: DC-AC power amplifier, Automatic muliti-stage bumpless switching, Load estimation, Digital robust control

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1. INTRODUCTION

A PWM power amplifier used as a power supply or amplifier has good power conversion efficiency, small size and lightweight, it is widely used for common apparatus. We apply the PWM power amplifier to an AC power supply apparatus[1, 2]. The AC power supply apparatus output the same AC as the commercial power supply. Since, in the commercial power supply, the voltage may fall, the waveform may not be a precise sine-wave or the noise may be mixed, the AC power supply apparatus is used as a regulated power supply. Especially it is needed when performing precise electric measurement etc. And it has a function of frequency conversion or voltage conversion, so it is used when testing and producing of the goods of a foreign country, or when the power supply of the same power supply specification as the one of a foreign country must be supplied. Furthermore, the AC power supply apparatus is used as the power supply for a low frequency wave immunity test. The low frequency wave immunity test examines whether the electronic device operates normally in abnormal conditions, such as a fall of voltage and an instantaneous breaking off. Therefore, the AC power supply apparatus in which the transient response characteristics does not deteriorate for the various load characteristics from capacitivity to inductivity is needed. In the low frequency wave immunity test, it is necessary to make various waveforms, such as breaking off wave etc. which have rapid changes. Therefore, it is also required that output voltage should follow at high speed to a reference step input without overshooting. Then, a so-called robust PWM power amplifier which can attain those demands with one controller is needed. We proposed[3, 4] previously the different methods from other methods[5] for designing the robust digital controller for PWM power amplifiers. Furthermore, the digital controller which uses the bumpless mode switching was proposed in order to extend the range of load wider[6, 7].

In this paper a multi-stage switching type digital controller is proposed for spreading capacitance load and inductance load ranges more and improving the transient characteristics for inductance load[8, 9]. In

the previous proposed controller[6, 7], the configuration of the controller is the same to all loads. At inductance load, there is a possibility that the transient characteristics may become bad and the specification may not be satisfied. Therefore, a load current is estimated at inductance load, and the new controller which also uses load current for feedback is configured. A inductance is estimated and the controller for no load is switched to this new controller bumplessly. In order to extend the range of capacitance load, the controller is increased from two stage to three stage, and these are switched to each other bumplessly. The digital controller with the mulitistage bumpless mode switching function is actually realized by using DSP. It is demonstrated from experiments that the multi-stage switching type digital controller is realizable and the given larger specifications are satisfied smoothly.

2. PWM POWER AMPLIFIER

The power amplifier as shown in **Fig.1** is being manufactured. The triangular wave double carrier system is adopted as a PWM switching signal generating part. The amplitude c_m of the triangular wave is 10[V]. The range of the carrier frequency of triangular wave is $10 - 100$[kHz]. A power amplification part is a full-bridge type chopper circuit, and the voltage of direct-current power-supply E is 150[V]. The LC circuit is a filter for removing carrier and switching noises. The values L_0 and C_0 of LC circuit are determined so that control systems can make their sensitivity to load change low and reduce noise.

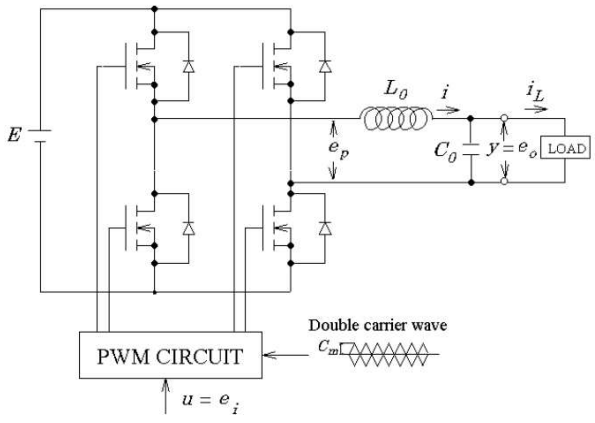

Fig.1: *PWM power amplifier*

If the frequency of input u is smaller enough than that of the carrier, the state equation of the PWM power amplifier at no load and inductance load in **Fig.1** can be expressed from the state equalizing method[2] as follows:

$$\begin{cases} \dot{\vec{x}} = A_c\vec{x} + B_c u \\ y = C\vec{x} \end{cases} \tag{1}$$

where at no load

$$\vec{x} = \begin{bmatrix} e_o \\ i \end{bmatrix} \quad A_c = \begin{bmatrix} 0 & \frac{1}{C_0} \\ -\frac{1}{L_0} & -\frac{R_0}{L_0} \end{bmatrix} \quad B_c = \begin{bmatrix} 0 \\ \frac{K_p}{L_0} \end{bmatrix}$$
$$C = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad u = e_i \quad y = e_0 \quad K_p = -\frac{E}{c_m}$$

and at inductance load

$$\vec{x} = \begin{bmatrix} e_o \\ i \\ i_L \end{bmatrix} A_c = \begin{bmatrix} 0 & \frac{1}{C_0} & -\frac{1}{C_0} \\ -\frac{1}{L_0} & -\frac{R_0}{L_0} & 0 \\ \frac{1}{L_L} & 0 & \frac{R_{LL}}{L_L} \end{bmatrix} B_c = \begin{bmatrix} 0 \\ \frac{K_p}{L_0} \\ 0 \end{bmatrix}$$
$$C = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}$$

and R_0 is the total resistance of coil, ON resistance of FET, etc. and R_{LL} is a resistance of inductance load.

When realizing a digital controller by a DSP, a delay time exists between the start point of sampling operation and the output point of control input due to the input computing time and AD/DA conversion times. This delay time is considered to be equivalent to the input dead time which exists in the controlled object as shown in **Fig.2**.

Then the state equation of the system of **Fig.2** is expressed as follows:

$$\begin{cases} x_d(\vec{k+1}) = A_d\vec{x_d(k)} + B_d v(k) \\ y(k) = C_d\vec{x_d(k)} \end{cases} \tag{2}$$

where

$$\vec{x_d} = \begin{bmatrix} \vec{x} \\ \xi \end{bmatrix} \quad \xi(k) = u(k) \quad C_d = \begin{bmatrix} C & 0 \end{bmatrix}$$
$$A_d = \begin{bmatrix} e^{A_c T} & e^{A_c(T-L_d)} \int_0^{L_d} e^{A_c\tau} B_c d\tau \\ 0 & 0 \end{bmatrix}$$
$$B_d = \begin{bmatrix} \int_0^{T-L_d} e^{A_c\tau} B_c d\tau \\ 1 \end{bmatrix}$$

Now, the power amplifier with the following specifications 1-3 is designed and manufactured by constituting digital control systems to the PWM power amplifier (controlled object) at no load. Though the ranges of capacitance load and inductance load in spec.1 of our previous results[3, 4, 6, 7] are 50[μF] or 70[μF] and 10[mH], those ranges have expanded to 100[μF] and 5[mH].

1. The band-width of control systems is higher than 2[kHz] to each load , i.e., no load, resistance load, capacitance load, parallel load with resistance and capacitance load, and inductance load, where $8.8 \leq R_L < \infty[\Omega]$, $0 \leq C_L \leq 100[\mu F]$, $5 \leq L_L < \infty$[mH].
2. Against all the loads of spec.1, an over-shoot is not allowable in a step response.
3. The specs. 1 and 2 are satisfied also to change of the direct-current power supply of $\pm 10\%$.

The load change for the controlled object and the direct-current power supply change are considered as parameter changes in eq.(2). The state diagram of Eq.(2) is shown in Fig. 3. The part connected with the dashed lines is a subsystem which shows inductance load. The parameter changes can be transformed to equivalent disturbances q_v, $q_{\bar{y}_1}$, $q_{\bar{y}_2}$and q_y as shown in **Fig.3**. Moreover, if the saturation in the input arises or the input frequency is not so small in comparison with the carrier frequency, the controlled object will be regarded as a class of nonlinear systems. Such characteristics changes can be also transformed to equivalent disturbances as shown in **Fig.3**. Therefore, what is necessary is just to constitute the control systems whose the pulse transfer functions from the equivalent disturbances q_v, $q_{\bar{y}_1}$, $q_{\bar{y}_2}$ and q_y to the output y become as small as possible in their amplitudes, in order to robustize or suppress the influence of these parameter changes, i.e., load change, and direct-current power-supply change. In the next section, an easy designing method which makes it possible to suppress the influence of such disturbances with the target characteristics held will be presented.

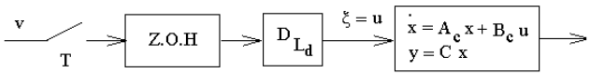

Fig.2: *Controlled object with input dead time $L_d(\leq T)$*

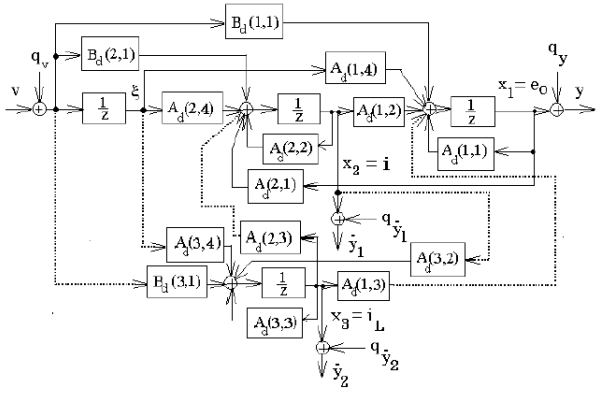

Fig.3: *Equivalent disturbances due to load variations (parameter variations)*

3. DESIGN OF EACH MODE CONTROLLER

First, the transfer function between the reference input r and the output y is specified at no load as follows:

$$W_{ry} = \frac{(1+H_1)(1+H_2)(1+H_3)(z-n_1)(z-n_2)}{(1-n_1)(1-n_2)(z+H_1)(z+H_2)(z+H_3)} \quad (3)$$

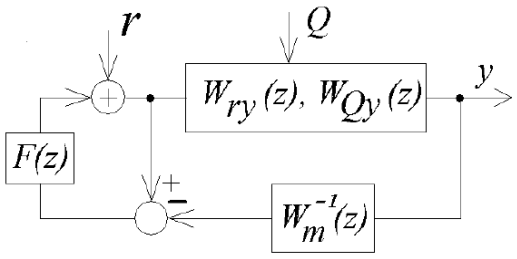

Fig.4: *System reconstituted with an inverse system and a filter*

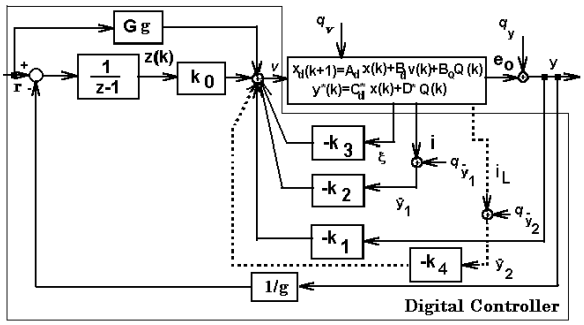

Fig.5: *Approximate 2-degree-of-freedom digital integral type control system*

Here, n_1 and n_2 are the zeros for discrete time control object (2). At inductance load one more specification pole increases. If this pole is specified to cancel the controlled object zeros, W_{ry} will become the same as eq.(3). It shall be specified that the relation of H_1 and H_2, H_3 becomes $H_1 \gg H_2 > 0, H_1 \gg H_3 > 0$. Then $W_{ry}(z)$ can be approximated by the following:

$$W_{ry}(z) \approx W_m(z) = \frac{1+H_1}{z+H_1} \quad (4)$$

We constitute a state feedback system using $u = Fx_d + Gr$ to the controlled object (2), and decide $F = [F(1,1)\ F(1,2)\ F(1,3)]$ (at inductance load $F = [F(1,1)\ F(1,2)\ F(1,3)\ F(1,4)]$) and G so that $W_{ry}(z)$ becomes eq.(3). The equivalent disturbance is defined as $Q = [q_v\ q_{\bar{y}_1}\ q_{\bar{y}_2}\ q_y]^T$ and the pulse transfer function between Q and the output y of the state feedback system is defined as $W_{Qy}(z)$. The system with an inverse system and a filter added to the state feedback system is constituted as shown in **Fig.4**.

In **Fig.4**, the pulse transfer function $F(z)$ is given by

$$F(z) = \frac{k_z}{z-1+k_z} \quad (5)$$

The transfer functions between r and y, Q and y of the systems in **Fig.4** are as follows:

$$y = \frac{1+H_1}{z+H_1} \times \frac{z-1+k_z}{z-1+k_z+k_z(-1+W_s(z))} W_s(z) r \quad (6)$$

$$y = \frac{z-1}{z-1+k_z}\frac{z-1+k_z}{z-1+k_zW_s(z)}W_{Qy}(z)Q \quad (7)$$

$$W_s(z) = \frac{(1+H_2)(1+H_3)(z-n_1)(z-n_2)}{(z+H_2)(z+H_3)(1-n_1)(1-n_2)}$$

Here, if $W_s(z) \approx 1$ in the wide range of frequency, eqs.(6) and (7) are as follows:

$$y \approx \frac{1+H_1}{z+H_1}r \quad (8)$$

$$y \approx \frac{z-1}{z-1+k_z}W_{Qy}(z)Q \quad (9)$$

It turns out from eqs.(8) and (9) that the characteristic $r-y$ can be specified with H_1 and the characteristic $Q-y$ can be independently specified with k_z. That is, the systems of **Fig.4** are of approximate 2-degree-of-freedom, and their sensitivity against the disturbance, i.e., load change becomes lower with the increase of k_z.

Now, if an equivalent conversion of the controller of **Fig.4** is carried out with introducing steady state gain g between $r-y$, the approximate 2-degree-of-freedom digital integral-type control systems will be obtained as shown in **Fig.5**. In Fig.5, The dashed line including k_4 is a new feedback introduced for current i_L at inductance load.

In **Fig.5**, the parameters of the controller at no load are as follows:

$$\begin{aligned} k_1 &= \frac{k_zG}{1+H_1} + F(1,1) \\ k_2 &= F(1,2) \quad k_3 = F(1,3) \quad k_0 = k_zGg \end{aligned} \quad (10)$$

At inductance load they are as follows:

$$\begin{aligned} k_1 &= \frac{k_zG}{1+H_1} + F(1,1) \quad k_2 = F(1,2) \\ k_3 &= F(1,4) \quad k_4 = F(1,3) \quad k_0 = k_zGg \end{aligned} \quad (11)$$

4. CONTROLLER SWITCHING METHOD

A. Load estimating method

From eq.(1), the capacitance is computed by the current in the coil and the derivative of output voltage such as

$$C_0 + C_L = \frac{i(t)}{\dot{e}_o(t)} \quad (12)$$

The capacitance can be estimated from eq.(12). In the case of the parallel load of capacitance and resistance, although the amount of feedbacks from $e_o(t)$ is added to $\dot{e}_o(t)$, if it is $\dot{e}_o(t) \gg e_o(t)$, the amount of addition can be ignored and the capacitance estimation can be carried out by eq.(12) even in this case. Eq.(12) can be expressed with discrete approximation as follows:

$$C_0 + C_L = \frac{T(i(k)+i(k-1))}{2(e_o(k)-e_o(k-1))} \quad (13)$$

Here, the current $i(k)$ uses the average value of $t=kT$ and $t=(k-1)T$. Noises, such as a carrier noise and a switching noise, are included in the output voltage of PWM power amplifier. When the change of output voltage is small, the S/N deteriorates, and it becomes impossible to estimate the capacitance. Therefore, only when the change of output voltage is large, the capacitance can be estimated. When the change is small, the function of holding the previously estimated value is needed.

Next, from eq.(1), the inductance is computed by the output voltage and the derivative of the load current such as

$$L_L = \frac{e_o(t)}{\dot{i}_L(t)} \quad (14)$$

Eq.(14) can be expressed with discrete approximation as follows:

$$L_L = \frac{T(e_o(k)+e_o(k-1))}{2(i_L(k)-i_L(k-1))} \quad (15)$$

Here, the output voltage $e_o(k)$ uses the average value of $t=kT$ and $t=(k-1)T$. Now, the load current i_L is required to compute L_L. Moreover, this load current is required also for load current feedback. A method of estimating load current is used without using a sensor. From eq.(1), the load current is computed by the coil current and the derivative of output voltage such as

$$i_L(t) = i - C_0\dot{e}_o(t) \quad (16)$$

Eq.(16) can be expressed with discrete approximation as follows:

$$\begin{aligned} i_L(k) &= (i(k)+i(k-1) \\ &- \frac{2C_0}{T}(e_o(k)-e_o(k-1)))/2 \end{aligned} \quad (17)$$

Here, the load current $i_L(k)$ uses the average value of $t=kT$ and $t=(k-1)T$.

Moreover, in order to use the derivatives of e_o and i_L, they have the gain characteristic of 20dB/dec, and have become sensitive to noise. In order to reduce thes influences, the following butterworth low-pass filters are inserted into the estimated values:

$$H(z) = \frac{a_0z^2+a_1z+a_2}{z^2+b_1z+b_2} \quad (18)$$

The parameters a_0, a_1, a_2, b_1, b_2 are the suitable values determined that the cutoff frequency of the filters become as about 5[KHz]. Eqs.(13), eq.(15), eq.(17) and eq.(18) are all implemented by DSP.

B. Controller switching method

The computing algorithm in 1 sampling period executed by DSP is shown in **Fig.6**. After estimating of the load current, inductance and capacitance, first it

is judged whether there is inductance, next the size of capacitance is judged, and the mode is switched. The switching method using estimated inductance and capacitance is shown in **Fig.7**. About inductance load, it judges whether there is any inductance beyond a certain value, and if it is, it will only switch to mode 4. About capacitance load, when the estimated capacitance value is beyond a certain value , or when it is below, the mode is switched. If the estimated value is changed due to noise etc. when the load capacitance is close to threshold of change, the problem the the mode switches frequently will arise. Therefore, the hysteresis characteristic with mode switching is established in Fig.7. The widths $TH_1 - TH_2$ and $TH_3 - TH_4$ used for hysteresis are sets up so that a change does not arise beyond necessity by experiment. As for the controller, the mode 1 is chosen at the start of DSP execution program. Even when an estimated value exceeds TH_1, it does not switch to the mode 2. Only when it exceeds TH_2, it switches to the mode 2. In the time of being conversely less than TH_1 a switch from the mode 2 to the mode 1 is performed.

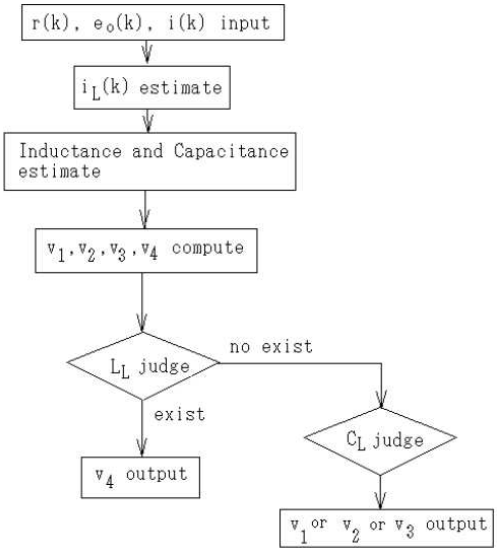

Fig.6: *The flow chart of computing algorithm in 1 sampling period*

C. Bumpless mode switching method

If the control variable is changed rapidly when the controller switches the mode, a bump will arise in an output. In order to suppress the bump, as shown in **Fig.8**, auxiliary feedback functions are implemented by a combination of mode i controller and mode j controller. Here $i = 1, 2, 3, 4$ and $j = 1, 2, 3, 4$ where $i \neq j$. In Fig.8, $X^\star$ is as in $X^\star = [y\ \bar{y_1}\ \xi]$, $k_{fi} = [k_{1i}\ k_{2i}\ k_{3i}]$ (at induccitive load $X^\star = [y\ \bar{y_1}\ \bar{y_2}\ \xi]$, $k_{fi} = [k_{1i}\ k_{2i}\ k_{3i}\ k_{4i}]$) and k_{0i} are the parameters of the mode i controller, $k_{fj} = [k_{1j}\ k_{2j}\ k_{3j}]$ (at induccitive load $k_{fj} = [k_{1j}\ k_{2j}\ k_{3j}\ k_{4j}]$) and k_{0j} is the parameters of the mode j controller. The parameter $k_{si} = 1/k_{0i}$ is the one for the bumpless switching function of the mode i controller and the parameter $k_{sj} = 1/k_{0j}$ is the one for the bumpless switching function of the mode j controller. According to these auxiliary function, at mode j, the control variable V_i of the mode i controller follows the control variable V_j of the controller j, and at mode i V_j follows V_i. Since V_j is mostly in agreement with V_j when the controllers are switched, they will be switched bumplessly. In addition, in Fig.8 the feedforward parameter Gg are omitted.

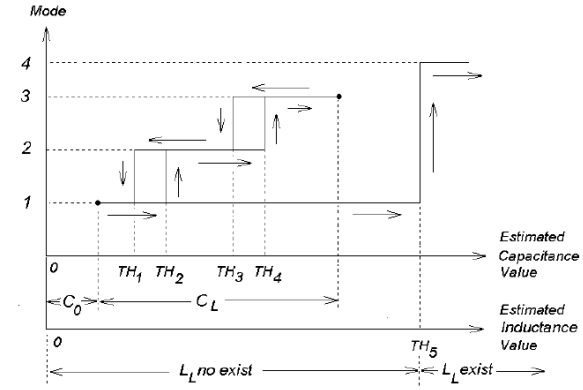

Fig.7: *Mode 1,2,3,4 switching method*

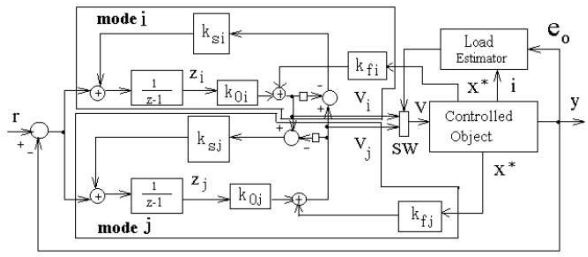

Fig.8: *Bumpless mode switching control system*

5. EXPERIMENTAL STUDIES

L_0 is decided as 180[μH], and R_0 is as 1.24[Ω]. Since the delay time becomes large when the digital controller is connected with the continuous-time controlled object, C_0 is decided on the balance with the sampling period. A DSP(TMS320C6416) from Texas Imstruments(TI) is used, which realizes the digital controller in Fig.8. The sampling period T and the carrier frequency f_c are set as 12[μs] and 83.3[kHz], respectively. The input dead time L_d is about 11.9[μs]. Then C_0, H_1, H_2, H_3, H_4 and k_z are decided such that all the specifications are satisfied and a phase margin becomes about 10[deg] or more. A voltage amplifier with the steady-state gain $g = 11.3$ is designed.

At capacitance load the setting value of C_0 is changed. And three controllers which satisfy speci-

Table 1: *Design parameters*

	H_1	H_2	H_3	H_4	k_z	$C_0(\mu F)$
mode 1	-0.89	-0.1	-0.11	×	0.4	25
mode 2	-0.89	-0.32	-0.2	×	0.42	40
mode 3	-0.89	-0.32	-0.2	×	0.48	60
mode 4	-0.89	-0.1	-0.11	-0.9995	0.4	25

fications in the following three kinds of range of capacitance are designed.
mode 1: $C_0 = 25[\mu\text{F}]$ and $0 \leq C_L \leq 25[\mu\text{F}]$
mode 2: $C_0 = 40[\mu\text{F}]$ and $0 \leq C_L \leq 40[\mu\text{F}]$
mode 3: $C_0 = 60[\mu\text{F}]$ and $0 \leq C_L \leq 65[\mu\text{F}]$
The values of C_0 of mode 2 and 3 are temporary for the design, and the actually used C_0 is $25[\mu\text{F}]$ in the mode 1. According to actual load capacity, these three controllers are switched as shown in Fig. 7. As a result, the capacitance range is as follows and satisfies specification.

$$0 \leq C_L \leq 100[\mu\text{F}] \tag{19}$$

The design parameters in the modes 1, 2 and 3 are shown in Table 1 and the controller parameters obtained are shown in Table 2.

Table 2: *Controller parameters*

	k_1	k_2	k_3	k_4	k_i
mode 1	-0.81187	-0.79198	0.78348	×	-0.90741
mode 2	-0.93332	-0.54970	0.48654	×	-1.0170
mode 3	-1.6071	-0.55951	0.49253	×	-1.7259
mode 4	-0.80739	-0.79008	0.78240	0.93733	-0.90749

At inductance load the new controller (mode 4) using load current feedback is designed. The design parameter in the mode 4 is shown in Table 1 and the controller parameter obtained is shown in Table 2.

The simulation results of the output voltage $y = e_o$, the input voltage $u = e_i$ and the current i at no load, resistance load($R_L = 8.8[\Omega]$), capacitance load($C_L = 25[\mu\text{F}]$), parallel load with resistance load($R_L = 8.8[\Omega]$) and capacitance load($C_L = 25[\mu\text{F}]$), and inductance load ($L_L = 5[\text{mH}]$) are shown in **Fig.9** using mode 1 controller. It turns out that all the specifications except for inductance load are satisfied within $0 \leq C_L \leq 25[\mu\text{F}]$. Since load current feedback is not used at induccitive load, the output voltage e_o does not reach the reference value easily. Moreover, it turns out that the specification is not satisfied at $C_0 + C_L = 75[\mu\text{F}]$. The simulation results of the output voltage $y = e_o$, the input

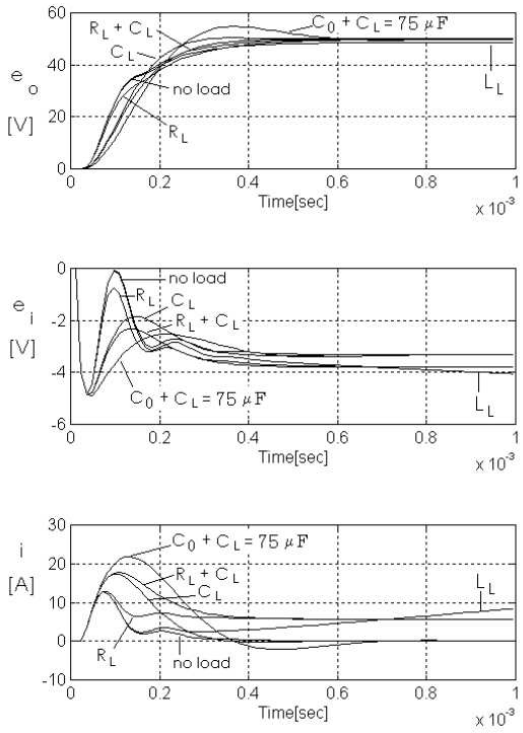

Fig.9: *Simulation results of step responses at various loads ($R_L = 8.8[\Omega]$,$C_0 = 25[\mu\text{F}]$,$C_L = 25[\mu\text{F}]$,$L_L = 5[\text{mH}]$*

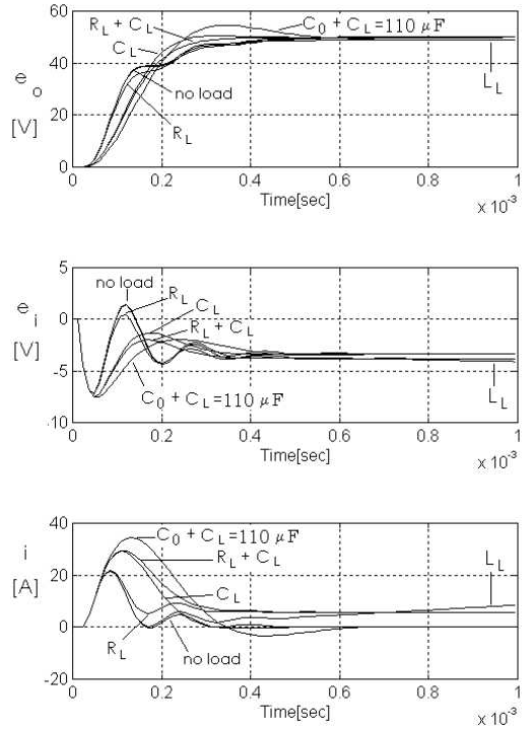

Fig.10: *Simulation results of step responses at various loads ($R_L = 8.8[\Omega]$, $C_0 = 40[\mu\text{F}]$, $C_L = 40[\mu\text{F}]$, $L_L = 5[\text{mH}]$) using only mode 2*

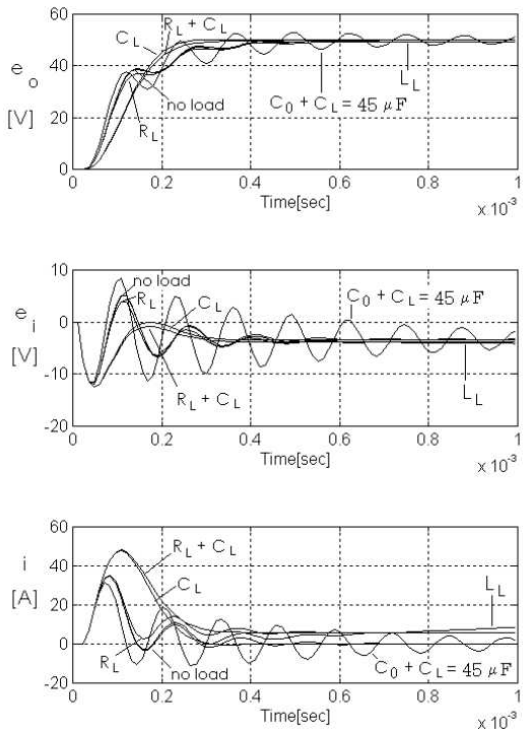

Fig.11: *Simulation results of step responses at various loads ($R_L = 8.8[\Omega]$, $C_0 = 60[\mu\text{F}]$, $C_L = 65[\mu\text{F}]$, $L_L = 5[\text{mH}]$) using only mode 3*

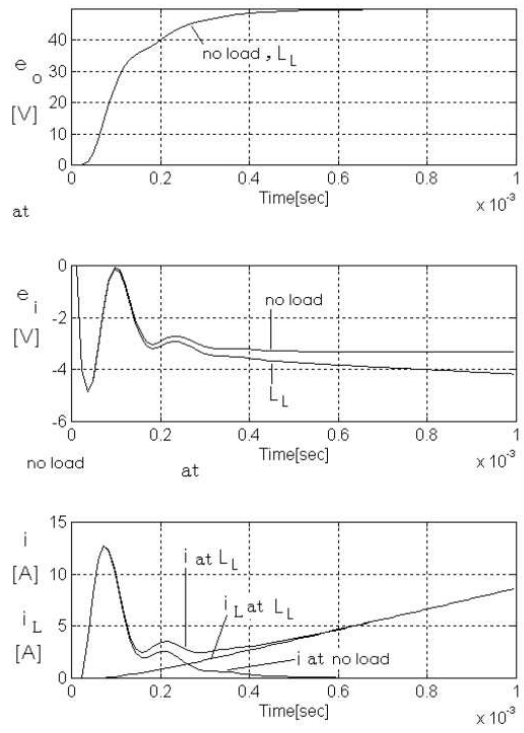

Fig.12: *Simulation results of step responses at inductance load ($L_L = 5[\text{mH}]$) using only mode 4*

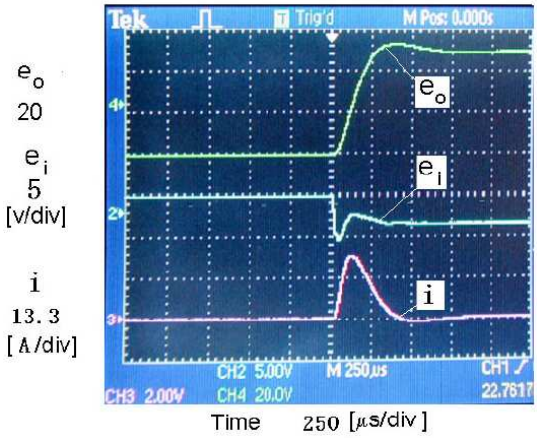

Fig.13: *Experimental result of step response at capacitance load($C_0 = 25[\mu\text{F}], C_L = 50[\mu\text{F}]$) using only mode 1*

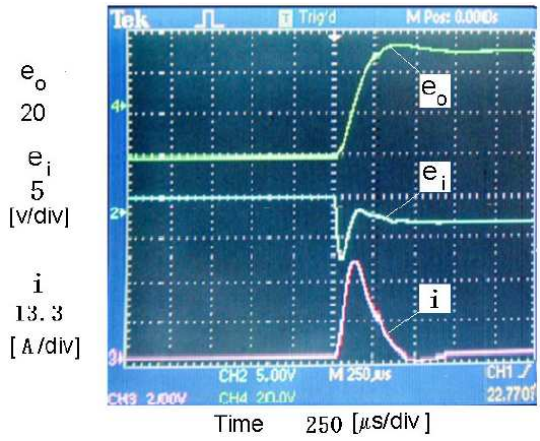

Fig.14: *Experimental result of step response at capacitance load($C_0 = 25[\mu\text{F}], C_L = 85[\mu\text{F}]$) using only mode 2*

voltage $u = e_i$ and the current i at no load, resistance load($R_L = 8.8[\Omega]$), capacitance load($C_L = 40[\mu\text{F}]$), parallel load with resistance load($R_L = 8.8[\Omega]$) and capacitance load($C_L = 40[\mu\text{F}]$), and inductance load($L_L = 5[\text{mH}]$) are shown in **Fig.10** using mode 2 controller. It turns out that all the specifications except for inductance load are satisfied within $0 \leq C_L \leq 40[\mu\text{F}]$. Moreover, it turns out that the specification is not satisfied at $C_0 + C_L = 110[\mu\text{F}]$, i.e., at the load of L-mode. The simulation results of the output voltage $y = e_o$, the input voltage $u = e_i$ and the current i at no load, resistance load($R_L = 8.8[\Omega]$), capacitance load($C_L = 65[\mu\text{F}]$), parallel load with resistance load($R_L = 8.8[\Omega]$) and capacitance load($C_L = 65[\mu\text{F}]$), and inductance load ($L_L = 5[\text{mH}]$) are shown in **Fig.11** using mode 3 controller. It turns out that all the specifications except for inductance load are satisfied within $0 \leq C_L \leq 65[\mu\text{F}]$. Moreover, it turns out that the specification is not satisfied at

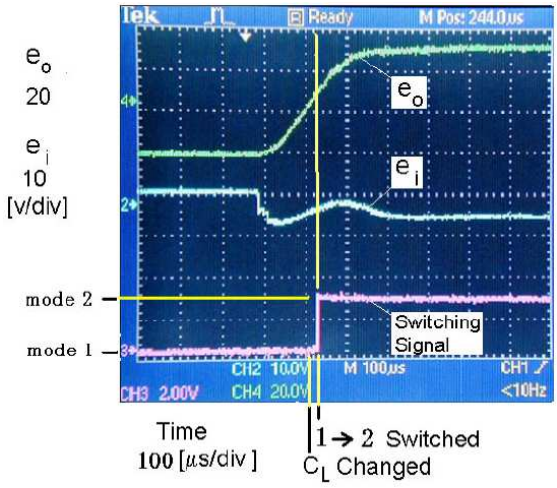

Fig.15: *Experimental result of step response using automatic bumpless switching from mode 1 to mode 2 and to mode 3 according to change of capacitance load from* $C_0 + C_L = 25[\mu\text{F}]$ *to* $C_0 + C_L = 125[\mu\text{F}]$ $(C_0 = 25[\mu\text{F}])$

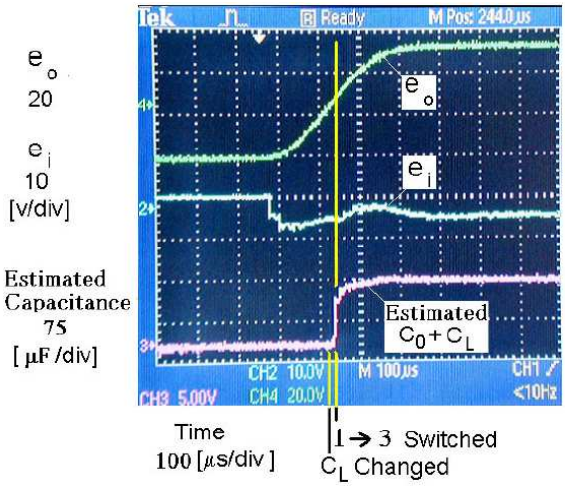

Fig.16: *Experimental result of step response using automatic bumpless switching from mode 1 to mode 2 and to mode 3 according to change of capacitance load from* $C_0 + C_L = 25[\mu\text{F}]$ *to* $C_0 + C_L = 125[\mu\text{F}]$ $(C_0 = 25[\mu\text{F}])$

$C_0 + C_L = 45[\mu\text{F}]$. The simulation results of the output voltage $y = e_o$, the input voltage $u = e_i$ and the current i at no load and inductance load $(L_L = 5[\text{mH}])$ are shown in **Fig.12** using mode 4 new controller. It turns out that the output voltage e_o at inductance load reachs to the reference value as well as at no load and the specification are satisfied.

According to the estimated value, the mode is switched from mode i to j. We set as $TH_1 = 42[\mu\text{F}]$, $TH_2 = 47[\mu\text{F}]$, $TH_3 = 74[\mu\text{F}]$ and $TH_4 = 77[\mu\text{F}]$. When $C_0 + C_L = 77[\mu\text{F}]$ at mode 1, the parameters are switched from mode 1 to mode 2 and to mode 3. If it switches from mode 1 to mode 2 and to mode 3, the

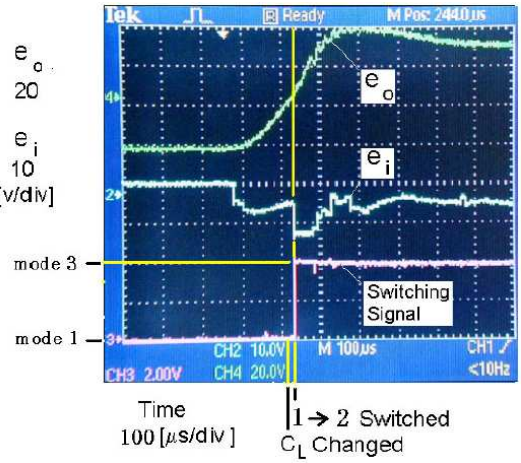

Fig.17: *Experimental result of step response at capacitance load*$(C_0 = 25[\mu\text{F}], C_L = 100[\mu\text{F}])$ *using automatic switching from mode 1 to mode 2 and to mode 3 without bumpless*

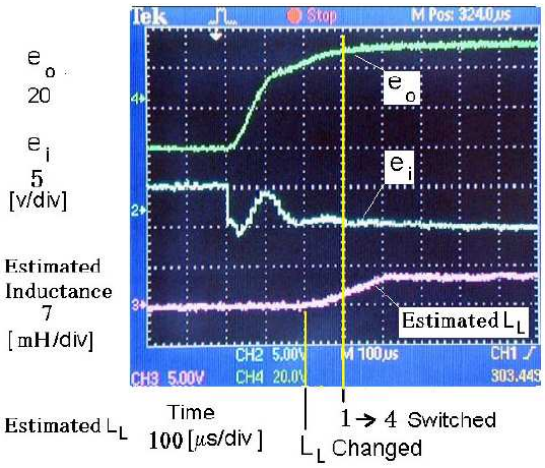

Fig.18: *Experimental result of step response using automatic bumpless switching from mode 1 to mode 4 according to change of inductance load from* $L_L = 0[\text{mH}]$ *to* $L_L = 5[\text{mH}]$ $(C_0 = 25[\mu\text{F}])$

range of C_L is extended as eq.(19) to $C_0 = 25[\mu\text{F}]$. We set as $TH_5 = 2[\text{mH}]$. When $TH_5 = 2[\text{mH}]$ at mode 1, the parameters are switched from mode 1 to mode 4, and all the specifications are satisfied.

Experimental results when realizing the digital controller with switchable parameters of Table 2 by using the DSP, and connecting with the controlled object in Fig.1 are shown in **Figs.13-19**. Fig.13 shows the step response when performing only mode 1 at capacitance load $C_L = 50[\mu\text{F}]$. It turns out that it does not satisfy the specification because of over-shoot. Fig.14 shows the step response when performing only mode 2 at capacitance load $C_0 + C_L = 110[\mu\text{F}]$. It turns out that it does not satisfy the specification because of over-shoot. Fig.15 shows the step responses of e_o and e_i and the indicating signal using the au-

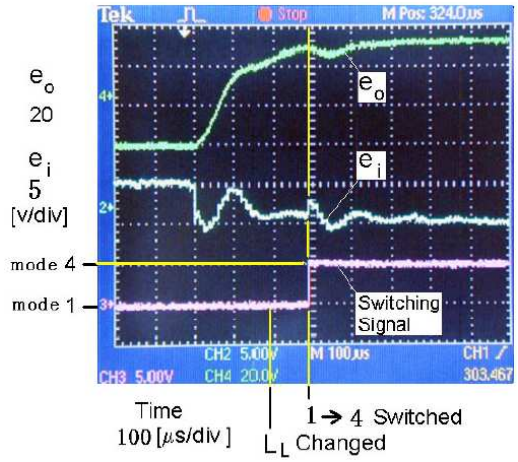

Fig.19: *Experimental result of step response at inducitive load($L_L = 5$[mH]) using automatic switching from mode 1 to mode 4 without bumpless*

tomatic bumpless mode switching from mode 1 to mode 2 and mode 3 at $C_L = 100[\mu\text{F}]$. Fig.16 shows the step responses of e_o and e_i and estimated capacitance using the automatic bumpless mode switching from mode 1 to mode 2 and mode 3 at $C_L = 100[\mu\text{F}]$. Fig.17 shows the step response using the automatic mode switching without bumpless from mode 1 to mode 2 and to mode 3 at $C_L = 100[\mu\text{F}]$. From Fig.15 and 16, it turns out that the parameters of the controller have switched from mode 1 to mode 2 and to mode 3 bumplessly during the transient response and all the specifications are satisfied. This experimental result shows that the bumpless mode switching can spread the range of the value of capacitance load. From Fig.17, it turns out that if the controller is switched without bumpless, a control input is changed seriously and saturation is caused and it does not satisfy the specification because of overshoot. Fig.18 shows the step responses of e_o and e_i and the estimated inductance using the automatic bumpless mode switching from mode 1 to mode 4 at $L_L = 2$[mH]. Fig.19 shows the step response using the automatic mode switching without bumpless from mode 1 to mode 4 at $TH_5 = 2$[mH]. From Fig.18, it turns out that the parameters of the controller have switched from mode 1 to mode 4 bumplessly and the specifications at inductance load is satisfied because of bumpless switching and using the new controller improving the transient response. From Fig.19, it turns out that if the controller is switched without bumpless, a control input is changed seriously and bump is caused and it does not satisfy the specification. Besides, we checked that even if loads are changed at the steady sate, the output voltage regulations are suppressed small.

6. CONCLUSION

In this paper, the concept of controller with multi-stage bumpless mode switching to attain the robustness to various loads and extensive load changes was given. The digital controller with multi-stage bumpless mode switching was realized by using a DSP implemented to the controlled object(PWM power amplifier which consists of a PWM signal generating part, an electric power conversion part and an LC filter). It is shown from an experiment that a sufficiently robust digital controller is realizable. The range of capacitance load and inductance load colud be extended and the transient characteristics was improved by performing the multi-stage bumpless mode switching and improving the transient response at inductance load using the new controller. These facts demonstrated the usefulness of our method using the multi-stage bumpless mode switching.

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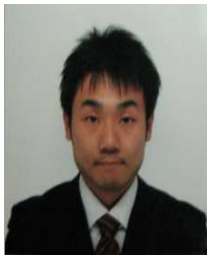

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