Synthesis and Analysis of a Versatile DC-DC Converter Designed by Using Switched-Capacitor Techniques

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ABSTRACT

Aimed at mobile applications such as back-lighting applications, battery applications, and so on, a switched-capacitor (SC) DC-DC converter which offers a $(N - s + 1)/(N - s) \times$ mode ($(N = 2, 3, \dots)$ and $(s = 0, 1, 2, \dots)$) as well as a step-down mode of operation is presented in this paper. Compared with conventional versatile converters, the proposed converter can realize high efficiency and flexibility of output voltages. The characteristics of the proposed converter are investigated by SPICE simulations and theoretical analyses. Concerning the power efficiency and the optimal duty factor, theoretical results are well in agreement with simulated results. Under conditions where input voltage V_{in} =3.7 V, output load $R_L = 30\,\Omega$, and output voltage $V_{out} = 3.3 \sim 5.3$ V, the proposed converter can improve the power efficiency more than 20 % from that of the conventional circuit. Furthermore, the validity of circuit design is confirmed by using experimental circuit which is built with commercially available transistors.

Keywords: DC-DC Converters, Switched-Capacitor Circuits, Back-Lighting Applications, Versatile Converters, Discrete-Time Circuits

1. INTRODUCTION

Recently, according to the down-scaling of portable electronic products, power converters designed by using switched-capacitor (SC) techniques [1]-[22] attract much attention. Since no magnetic elements are required to design SC power converters, they can realize thin circuit composition, light-weight and low-noise. For this reason, the SC power converter is used as a driver circuit of white LEDs for display back-lighting, a building block of battery management systems, and so on. For example, in mobile back-lighting applications, the stepped-up voltage such as $4.75 \sim 6.5$ V (Typ. =5 V) is required to drive some LEDs at up to 25 mA. On the other hand, to extend the battery runtime, a versatile SC converter which can provide step-up/step-down voltages is necessary.

To adjust the output voltage, on-resistance control scheme [9], [12], [13], [16] or pulse width modulation (PWM) scheme [10], [11] is usually employed in the SC DC-DC converter, because the ratio of voltage conversion is predetermined by circuit structure. The power efficiency of SC power converters gets worse by the regulation of the output voltage. Particularly, in the case of the conventional versatile converter [14]-[18] based on a doubler circuit, the efficiency decreases greatly when the low output voltage is required, because the output voltage must be regulated strongly [1] .

In this paper, aimed at back-lighting applications, battery management applications, and so on, a versatile SC DC-DC converter is proposed to provide stepped-up/ stepped-down voltages, and handy theoretical formulas are given concerning the power efficiency and the optimal duty factor. Compared with conventional versatile converters based on doubler circuits [14]-[18], the proposed converter can realize high efficiency and flexibility of output voltages, because it offers a $(N - s + 1)/(N - s) \times$ mode ($(N = 2, 3, \dots)$ and $(s = 0, 1, 2, \dots)$) as well as a step-down mode of operation.

The characteristics of the proposed converter are analyzed through theoretical analyses and SPICE simulations. Furthermore, to confirm the validity of the circuit design, the experimental circuit is fabricated with commercially available transistors.

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For example, in the case of back-lighting applications, the stepped-up voltage such as $4.75 \sim 6.5$ V (Typ. =5 V) must be generated from the converted voltage 7.4 V ($= 2 \times V_{in}$ (=3.7 V)). Therefore the output voltage is regulated strongly in the conventional converter.

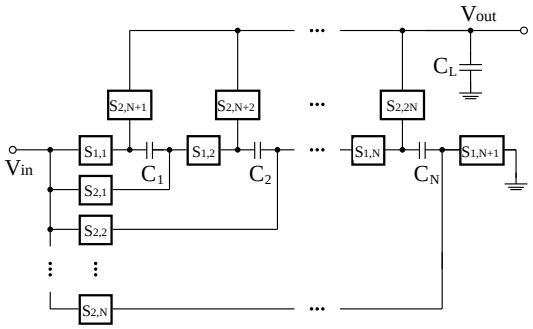


Fig.1: *Proposed SC DC-DC converter.*

2. CIRCUIT STRUCTURE

Figure 1 shows a $(N-s+1)/(N-s)\times$ mode DC-DC converter ($(N=2,3,\dots)$ and $(s=0,1,\dots)$) designed by using the SC technique [1]-[22] The proposed converter consists of $3N+1$ power switches and $N+1$ capacitors. In Fig.1, power switches $S_{1,i}$ and $S_{2,j}$ ($(i=1,\dots,N+1)$ and $(j=1,\dots,2N)$) are driven by 2-phase pulses $\Phi_{1,i}$ and $\Phi_{2,j}$, respectively. The interval of $\Phi_{1,i}$ and $\Phi_{2,j}$ is set to

$$\begin{aligned} T &= T1+T2, \\ T1 &= DT, \\ \text{and} \quad T2 &= (1-D)T, \end{aligned} \tag{1}$$

where T is a period of clock pulses and D denotes a duty factor. By controlling power switches $S_{1,i}$ and $S_{2,j}$, the proposed converter performs a DC-DC conversion.

The control scheme and circuit properties will be described in the following section.

3. THEORETICAL ANALYSIS

3.1 Step-Up Mode

First, an equivalent circuit when a step-up mode is analyzed. In the theoretical analysis, we assume that 1. parasitic elements are not effective and 2. the time constant is much larger than the period of clock pulses.

Figures 2 and 3 show instantaneous equivalent circuits when $s=0$ and $s\neq 0$, respectively. In the steady state, the differential value of electric charges in C_k $(k=1,\dots,N)$ satisfies

$$\Delta q_{T1}^{k} + \Delta q_{T2}^{k} = 0, \tag{2}$$

where Δq_{T1}^{k} and Δq_{T2}^{k} denote electric charges when $State-T1$ and $State-T2$, respectively. In the case of $State-T1$, the differential values of electric charges in input and output terminals, $\Delta q_{T1,V_{in}}$ and $\Delta q_{T1,V_{out}}$, are given by

$$\begin{aligned} &\Delta q_{T1,V_{in}} = \Delta q_{T1}^{s+1} = \cdots = \Delta q_{T1}^{N} \\ \text{and} \quad &\Delta q_{T1,V_{out}} = \Delta q_{T1}^{L}. \end{aligned} \tag{3}$$

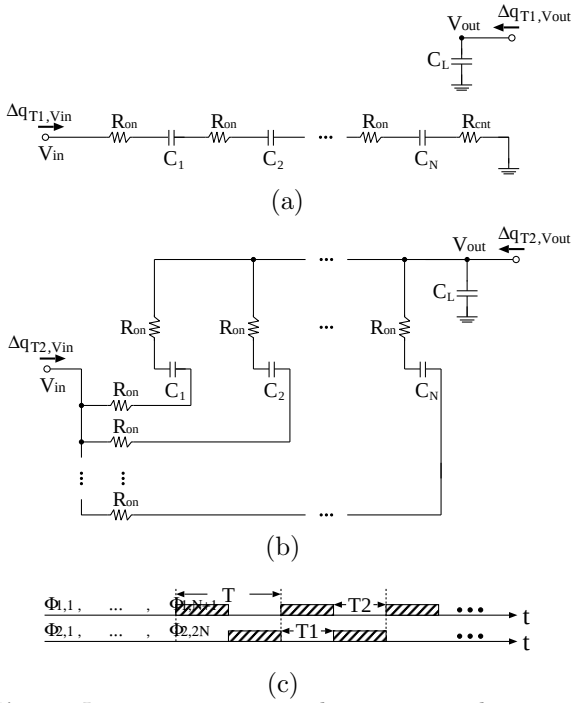


Fig.2: *Instantaneous equivalent circuits when $s=0$. (a) $State-T1$. (b) $State-T2$. (c) Timing of pulses.*

On the other hand, in the case of $State-T2$, the differential values of electric charges in input and output terminals, $\Delta q_{T2,V_{in}}$ and $\Delta q_{T2,V_{out}}$, are given by

$$\begin{aligned} \Delta q_{T2,V_{in}} &= -\sum_{p=s+1}^{N} \Delta q_{T2}^{p} \\ \text{and} \quad \Delta q_{T2,V_{out}} &= \sum_{p=s+1}^{N} \Delta q_{T2}^{p} + \Delta q_{T2}^{L}. \end{aligned} \tag{4}$$

Here, the averaged currents of input and output terminals are given by

$$\begin{aligned} \overline{I_{in}} &= (\Delta q_{T1,V_{in}} + \Delta q_{T2,V_{in}})/T \\ &= \Delta q_{V_{in}}/T \\ \text{and} \quad \overline{I_{out}} &= (\Delta q_{T1,V_{out}} + \Delta q_{T2,V_{out}})/T \\ &= \Delta q_{V_{out}}/T, \end{aligned} \tag{5}$$

where $\Delta q_{V_{in}}$ and $\Delta q_{V_{out}}$ are electric charges in input and output terminals, respectively. From Eqs.(2) $\sim$ (5), the relation between the input current and the output current is obtained by

$$\overline{I_{in}} = -\left(\frac{N-s+1}{N-s}\right)\overline{I_{out}}. \tag{6}$$

In Figs. 2 and 3, the energy consumed by resistors in one period, W_T, can be expressed by

$$W_T = W_{T1} + W_{T2}, \tag{7}$$

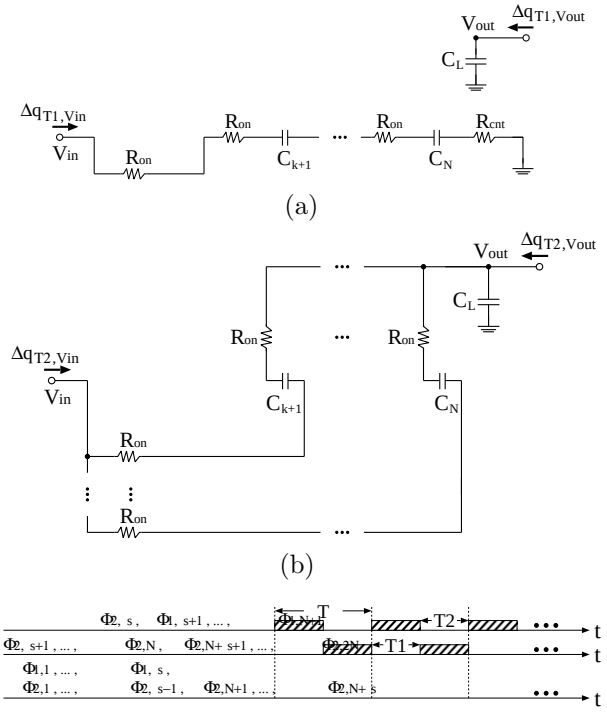


Fig.3: *Instantaneous equivalent circuits when $s \neq 0$. (a) State$-T1$. (b) State$-T2$. (c) Timing of pulses.*

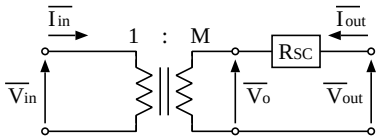


Fig.4: *General form of equivalent circuit.*

where

$$W_{T1} = \frac{R_{on}}{T1}(\Delta q_{T1}^{s+1})^2 \cdot u(s) + (N-s)\frac{R_{on}}{T1}(\Delta q_{T1}^{s+1})^2 + \frac{R_{cnt}}{T1}(\Delta q_{T1}^{s+1})^2$$

and

$$W_{T2} = \frac{2R_{on}}{T2}\sum_{p=s+1}^{N}(\Delta q_{T2}^{p})^2.$$

In Eq.(7), $u(s)$ is a unit step function. From Eqs.(1) $\sim$ (5), Eq.(7) can be rewritten as

$$W_{T1} = \frac{(N-s+1)R_{on}}{(N-s)^2 DT}(\Delta q_{V_{out}})^2 + \frac{R_{cnt}}{(N-s)^2 DT}(\Delta q_{V_{out}})^2$$

and

$$W_{T2} = \frac{2R_{on}}{(N-s)(1-D)T}(\Delta q_{V_{out}})^2. \quad (8)$$

Here, a general equivalent circuit of SC power converters [3], [4], [9], [12], [19], [22] can be given by the circuit shown in Fig.4, where R_{SC} is called the SC resistance, M is the ratio of the ideal transformer, and $\overline{V_{in}}$ and $\overline{V_{out}}$ denote an averaged input voltage and an averaged output voltage, respectively. The consumed energy W_T of Fig.4 is defined by

$$\begin{aligned} W_T &= W_{T1} + W_{T2} \\ &\equiv (\frac{\Delta q_{V_{out}}}{T})^2 \cdot R_{SC} \cdot T. \end{aligned} \quad (9)$$

By substituting Eq.(8) into Eq.(9), the SC resistance when the step-up mode, $R_{SC,up}$, is given by

$$\begin{aligned} R_{SC,up} &= \frac{1}{D(N-s)^2} \cdot R_{on} \cdot u(s) \\ &\quad + \frac{1+D}{D(1-D)(N-s)} \cdot R_{on} \\ &\quad + \frac{1}{D(N-s)^2} \cdot R_{cnt}. \end{aligned} \quad (10)$$

The equivalent circuit shown in Fig.4 can be expressed by the determinant using a Kettenmatrix. Therefore, by using Eqs.(6) and (10), the equivalent circuit of the proposed converter is given by the following determinant:

$$\begin{bmatrix} \overline{V_{in}} \\ \overline{I_{in}} \end{bmatrix} = \begin{bmatrix} \frac{N-s}{N-s+1} & 0 \\ 0 & \frac{N-s+1}{N-s} \end{bmatrix} \begin{bmatrix} 1 & R_{SC,up} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{out}} \\ -\overline{I_{out}} \end{bmatrix} \quad (11)$$

As Eq.(11) shows, the output voltage of the proposed circuit becomes $V_{in} \times (N-s+1)/(N-s)$ when $R_{SC,up} \ll R_L$.

From Eq.(11), the averaged output voltage $\overline{V_{out}}$ is expressed by

$$\overline{V_{out}} = \frac{R_L}{R_L + R_{SC,up}} \cdot (\frac{N-s+1}{N-s}) \cdot \overline{V_{in}}. \quad (12)$$

Furthermore, power efficiency η_{up} [2] can be obtained by

$$\begin{aligned} \eta_{up} &= \frac{R_L \overline{I_{out}}^2}{R_L \overline{I_{out}}^2 + R_{SC,up}\overline{I_{out}}^2} \\ &= \frac{R_L}{R_L + R_{SC,up}}, \end{aligned} \quad (13)$$

where $R_{SC,up}$ depends on resistance R_{cnt} shown in Eq.(10). As Eq.(13) shows, $\overline{V_{out}}$ can be regulated by controlling R_{cnt} which corresponds to the on-resistance of $S_{1,N+1}$ (see in Figs. 2 and 3). In other words, the regulation is performed by controlling the gate voltage of $S_{1,N+1}$.

As Eq.(13) shows, the increase of $R_{SC,up}$ causes the decrease of efficiency η_{up}. In other words, the maximum power efficiency is obtained when $R_{cnt} =$

[2] Of course, the consumed energy of peripheral circuits such as pulse generators, comparators, etc. is disregarded in the power efficiency of Eq.(13).

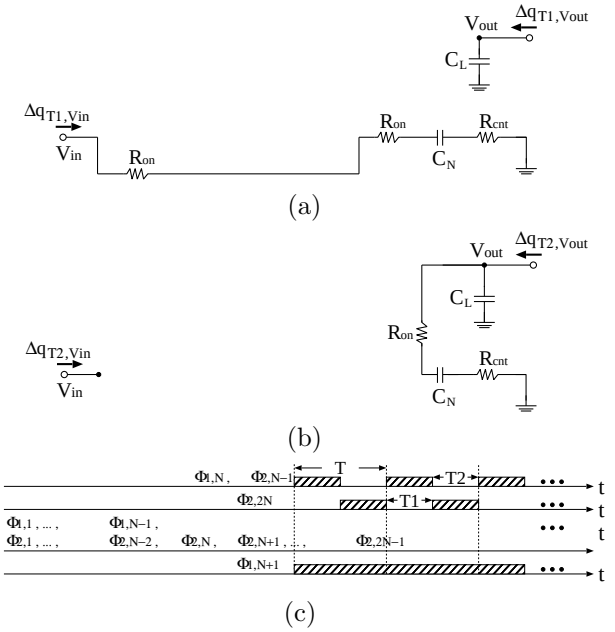


Fig.5: *Instantaneous equivalent circuits when step-down mode. (a) State − T1. (b) State − T2. (c) Timing of pulses.*

R_{on}. From Eq.(10), the minimum on-resistance $\min(R_{SC,up})$ can be expressed by

$$\min(R_{SC,up}) = \{\frac{(N-1)D+(N+1)+(1-D)u(s)}{D(1-D)(N-s)^2}\}R_{on}. \quad (14)$$

In Eq.(14), the optimum value of parameter D is obtained when

$$\frac{d\min(R_{SC,up})}{dD} = 0 \quad \text{and} \quad 0 < D < 1. \quad (15)$$

Concretely, from Eqs.(14) and (15), the optimal duty factor is $D \simeq 0.45$ [3] when $N = 3$ and $s = 0$.

3.2 1 × Mode

Figure 5 shows instantaneous equivalent circuits in the case of the step-down mode. In Fig.5 (a), the differential values of electric charges, $\Delta q_{T1,V_{in}}$ and $\Delta q_{T1,V_{out}}$, are given by

$$\Delta q_{T1,V_{in}} = \Delta q^N_{T1} \quad \text{and} \quad \Delta q_{T1,V_{out}} = \Delta q^L_{T1}. \quad (16)$$

In Fig.5 (b), the differential values of electric charges, $\Delta q_{T2,V_{in}}$ and $\Delta q_{T2,V_{out}}$, are given by

$$\Delta q_{T2,V_{in}} = 0 \quad \text{and} \quad \Delta q_{T2,V_{out}} = \Delta q^N_{T2} + \Delta q^L_{T2}. \quad (17)$$

From Eqs.(2), (5), (16), and (17), the relation between input and output currents is derived as

$$\overline{I_{in}} = -\overline{I_{out}}. \quad (18)$$

In Figs.5 (a) and (b), W_{T1} and W_{T2} can be expressed by

$$W_{T1} = \frac{2R_{on}}{T1}(\Delta q^N_{T1})^2 + \frac{R_{cnt}}{T1}(\Delta q^N_{T1})^2$$
$$\text{and} \quad W_{T2} = \frac{R_{on}}{T2}(\Delta q^N_{T2})^2 + \frac{R_{cnt}}{T2}(\Delta q^N_{T2})^2, \quad (19)$$

respectively. By substituting Eqs.(1), (2), (5), (16), (17), (19) into Eq.(9), the SC resistance when the step-down mode, $R_{SC,dw}$, can be expressed by

$$R_{SC,dw} = \frac{R_{on}(2-D)+R_{cnt}}{D(1-D)}. \quad (20)$$

Therefore, by using Eqs.(18) and (20), the equivalent circuit can be expressed by the following determinant:

$$\begin{bmatrix} \overline{V_{in}} \\ \overline{I_{in}} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & R_{SC,dw} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{out}} \\ -\overline{I_{out}} \end{bmatrix}. \quad (21)$$

As Eq.(21) shows, the output voltage of the proposed circuit becomes V_{in} when $R_{SC,dw} \ll R_L$.

From Eq.(21), the averaged output voltage $\overline{V_{out}}$ is obtained by

$$\overline{V_{out}} = \frac{R_L}{R_L + R_{SC,dw}} \cdot \overline{V_{in}}. \quad (22)$$

As Eqs.(20) and (22) show, the step-down conversion can be realized by controlling R_{cnt} (see in Fig.5).

From Eq.(21), power efficiency η_{dw} can be given by

$$\eta_{dw} = \frac{R_L}{R_L + R_{SC,dw}}. \quad (23)$$

From Eqs.(20) and (23), the maximum efficiency is obtained when $D \simeq 0.55$, because

$$\min(R_{SC,dw}) = \frac{R_{on}(3-D)}{D(1-D)}. \quad (24)$$

4. SIMULATION

To confirm the validity of circuit design and theoretical analyses, SPICE simulations were performed under conditions where input voltage $V_{in} = 3.7\,\mathrm{V}$, $N = 3$, $C_1 = C_2 = C_3 = 1\,\mu F$, $T = 1\,\mu s$ and on-resistance $R_{on} = 0.4\,\Omega$. As an example of the proposed converter, the converter shown in Fig.6 were used in the SPICE simulations.

Figure 7 shows the power efficiency of the proposed converter as a function of parameter D. The theoretical results in Fig.7 were obtained by Eqs.(10), (13), (20), and (23), where $R_{cnt} = R_{on} = 0.4\,\Omega$ and $R_L = 30\,\Omega$. In the case of 2 ×, 1.5 ×, 1.33 ×, and 1 ×

When $N = 3$ and $s = 0$, the proposed converter offers a 1.33 × mode of operation. In other words, the power efficiency becomes the maximum value when $D \simeq 0.45$.

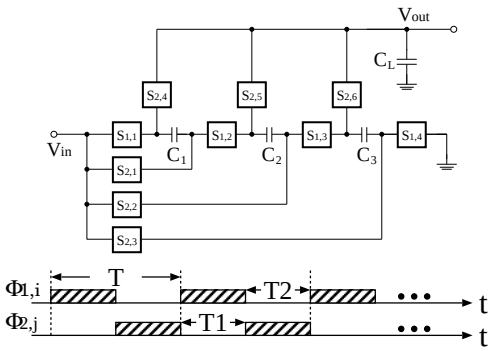


Fig.6: *Example of proposed converter when $N = 3$.*

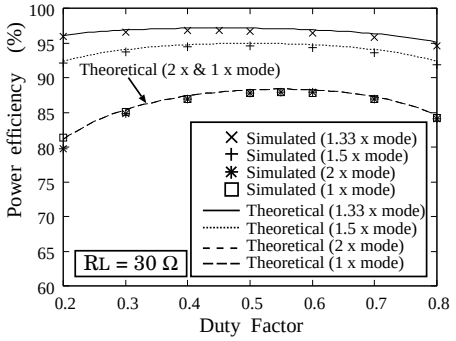


Fig.7: *Power efficiency as function of parameter D.*

modes, the converter can achieve the best efficiency by setting the duty factor to 0.55, 0.5, 0.45, and 0.55, respectively. As Fig.7 shows, the results of theoretical analyses agree well with the simulated results.

Figure 8 shows output voltage V_{out} with different conversion ratios. As Fig.8 shows, the proposed converter can realize $2 \times / 1.5 \times / 1.33 \times / 1 \times$ modes, and the theoretical results are well in agreement with the simulated results in the steady state. The theoretical results in Fig.8 were obtained by Eqs.(10), (12), (20), and (22), where $R_{cnt} = R_{on} = 0.4\,\Omega$ and $R_L = 30\,\Omega$.

Figure 9 shows the power efficiency of the proposed converter as a function of output load R_L. Of course, the power efficiency of the proposed converter can be improved by using power-switches with small on-resistance. As Fig.9 shows, the theoretical results obtained by Eqs.(10), (13), (20), and (23) agree well with the simulated results.

Figure 10 shows the comparison of the power efficiency between the proposed converter and the conventional converter [18] as a function of output voltage V_{out}. In Fig.10, the regulation of the output voltage was achieved by using an on-resistance control scheme [9], [12], [13], [16]. As Fig.10 shows, the proposed converter can improve the power efficiency in the range of $1.5 \times$ / $1.33 \times$ modes.

5. EXPERIMENT

To confirm the validity of circuit design, experiments were performed regarding to the proposed circuit with parameter $N = 2$. The experimental circuit was built with commercially available transistors 2SK2493 on a bread board.

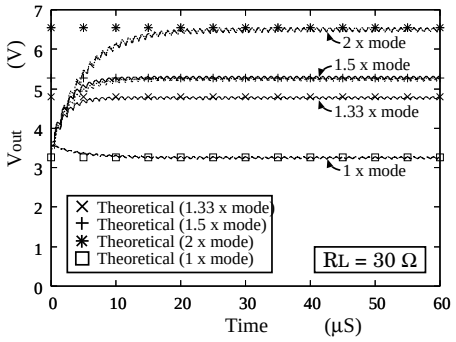


Fig.8: *Output voltage with different conversion ratios.*

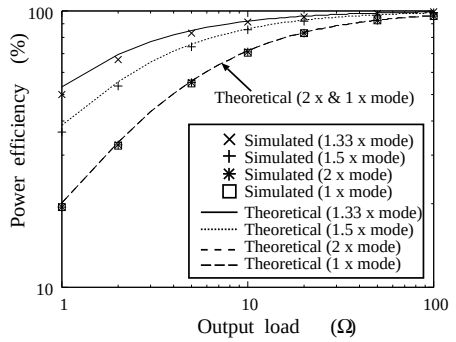


Fig.9: *Power efficiency as function of output load R_L.*

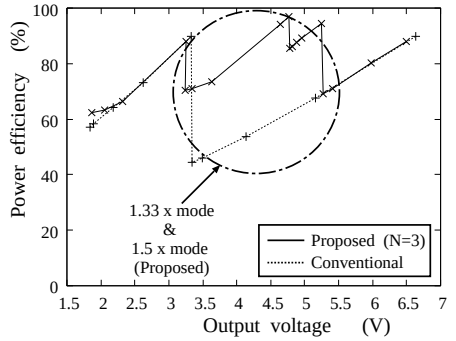
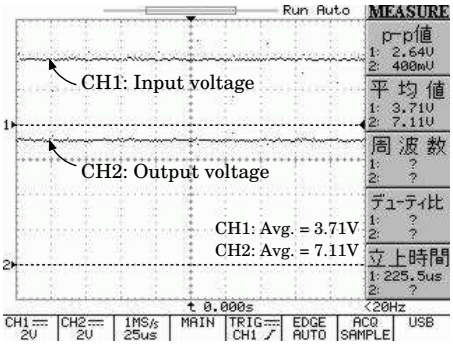


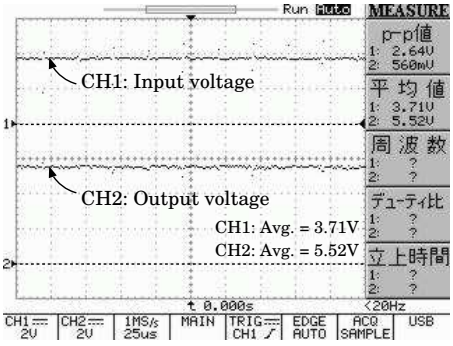
Fig.10: *Power efficiency as function of output voltage V_{out}.*

Figure 11 shows the results of DC-DC conversion obtained by the experimental circuit. In Fig.11, the experiment was performed under conditions where input voltage $V_{in} = 3.7\,\mathrm{V}$, clock frequency $1/T = 20\,\mathrm{kHz}$, capacitors $C_1 = C_2 = 1\,\mu\mathrm{F}$, $C_L = 10\,\mu\mathrm{F}$, and output load $R_L = 1\,\mathrm{k}\Omega$. As Fig.11 shows, the experimental circuit can achieve two or more conversion modes such as $2 \times / 1.5 \times / 1 \times$ modes [4] .

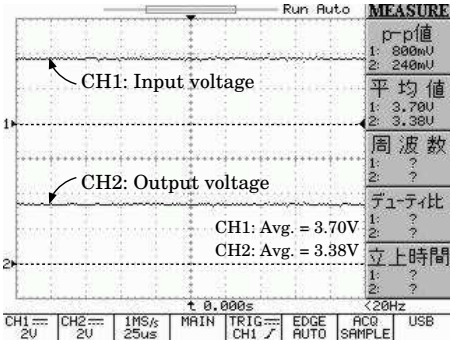
In the experiment, circuit properties such as power efficiency, ripple noise, etc. were not examined, because the experimental circuit was built with commercially available transistors on the bread board. For example, in transistor 2SK2493, the source



(a)



(b)



(c)

Fig.11: *Experimental results. (a) 2 × mode. (b) 1.5 × mode. (c) 1 × mode.*

6. CONCLUSION

For mobile applications, an SC DC-DC converter which offers a $(N-s+1)/(N-s)$ mode as well as a step-down mode of operation has been proposed in this paper. The validity of the circuit design was confirmed by theoretical analyses, SPICE simulations, and experiments.

Concerning the power efficiency and the optimal duty factor, the derived theoretical formulas will be helpful to estimate circuit characteristics, because theoretical results were well in agreement with simulated results. The SPICE simulations showed that the proposed converter can realize a $(N-s+1)/(N-s)$ mode of operation. Under conditions where input voltage V_{in} =3.7 V, output load $R_L = 30\,\Omega$, and output voltage $V_{out} = 3.3 \sim 5.3$ V, the proposed converter can improve the power efficiency more than 20 % from that of the conventional circuit. Furthermore, the validity of circuit design was confirmed through experiments.

The further improvement of efficiency is left to a future study.

terminal is connected to the drain terminal beforehand through a diode. Therefore, only the circuit design was verified in this experiment. The IC implementation and experiments are left to a future study.

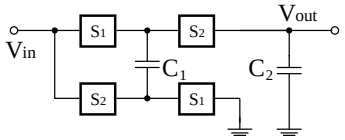
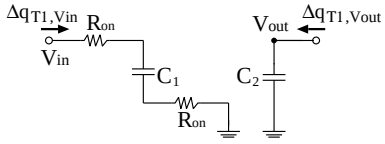
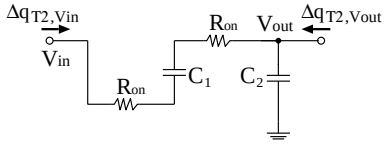


Fig.12: *Conventional converter.*



(a)



(b)

Fig.13: *Instantaneous equivalent circuits of Fig.12. (a) State−T1 ($S_1 = On$ and $S_2 = Off$). (b) State−T2 ($S_1 = Off$ and $S_2 = On$).*

7. ACKNOWLEDGEMENTS

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8. APPENDIX

In this section, the characteristics of the voltage doubler circuit are analyzed.

Figure 12 shows the conventional converter described in [14], [16]-[18]. In Fig.12, the switches S_1 and S_2 are driven by non-overlapped 2-phase clock pulses.

Figure 13 shows the instantaneous equivalent circuits of the converter. In the case of $State - T1$, capacitor C_1 is charged by input voltage V_{in} via S_1's. Therefore, the voltage of C_1 becomes V_{in}. In this timing, the output voltage is provided by C_2. On the other hand, in the case of $State - T2$, input voltage V_{in} and capacitor C_1 are connected in series via S_2's.

Therefore, a stepped-up voltage $2V_{in}$ is obtained in the output terminal under no load condition. The properties of the conventional converter can be obtained as follows:

In the steady state, the differential value of electric charges in C_k $(k = 1, 2)$ satisfies

$$\Delta q^k_{T1} + \Delta q^k_{T2} = 0. \quad (25)$$

In the case of $State-T1$, $\Delta q_{T1,V_{in}}$ and $\Delta q_{T1,V_{out}}$ are given by

$$\begin{aligned} \Delta q_{T1,V_{in}} &= \Delta q^1_{T1} \\ \text{and} \quad \Delta q_{T1,V_{out}} &= \Delta q^2_{T1}. \end{aligned} \quad (26)$$

On the other hand, in the case of $State-T2$, $\Delta q_{T2,V_{in}}$ and $\Delta q_{T2,V_{out}}$ are given by

$$\begin{aligned} &\Delta q_{T2,V_{in}} = -\Delta q^1_{T2} \\ \text{and} \quad &\Delta q_{T2,V_{out}} = \Delta q^1_{T2} + \Delta q^2_{T2}. \end{aligned} \quad (27)$$

From Eqs.(25) $\sim$ (27), the averaged currents of the input and the output are given by

$$\begin{aligned} \overline{I_{in}} &= (\Delta q_{T1,V_{in}} + \Delta q_{T2,V_{in}})/T \\ &= 2\Delta q^1_{T1}/T \\ \text{and} \quad \overline{I_{out}} &= (\Delta q_{T1,V_{out}} + \Delta q_{T2,V_{out}})/T \\ &= -\Delta q^1_{T1}/T. \end{aligned} \quad (28)$$

Therefore, the following equation is obtained by

$$\overline{I_{in}} = -2\overline{I_{out}}. \quad (29)$$

In Fig.13, the energy consumed by resistors in one period, W_T, can be expressed by

$$W_T = W_{T1} + W_{T2}, \quad (30)$$

where

$$\begin{aligned} W_{T1} &= \frac{2R_{on}}{T1}(\Delta q^1_{T1})^2 \\ \text{and} \quad W_{T2} &= \frac{2R_{on}}{T2}(\Delta q^1_{T2})^2. \end{aligned}$$

From Eqs.(25) $\sim$ (28), Eq.(30) can be rewritten as

$$\begin{aligned} &W_{T1} = \frac{2R_{on}}{DT}(\Delta q_{V_{out}})^2 \\ \text{and} \quad &W_{T2} = \frac{2R_{on}}{(1-D)T}(\Delta q_{V_{out}})^2. \end{aligned} \quad (31)$$

By substituting Eq.(31) into Eq.(30), the SC resistance of the doubler circuit, R_{SCC}, can be obtained by

$$R_{SCC} = \frac{2}{D(1-D)} \cdot R_{on}. \quad (32)$$

In Eq.(32), the optimal duty factor is $D = 0.5$. From Eqs.(29) and (32), the equivalent circuit of the conventional converter is expressed by the following determinant:

$$\begin{bmatrix} \overline{V_{in}} \\ \overline{I_{in}} \end{bmatrix} = \begin{bmatrix} 2 & 0 \\ 0 & 1/2 \end{bmatrix} \begin{bmatrix} 1 & R_{SCC} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{out}} \\ -\overline{I_{out}} \end{bmatrix}. \quad (33)$$

From Eq.(33), power efficiency η_C of the conventional converter can be given by

$$\begin{aligned} \eta_C &= \frac{R_L\overline{I_{out}}^2}{R_L\overline{I_{out}}^2 + R_{SCC}\overline{I_{out}}^2} \\ &= \frac{R_L}{R_L + R_{SCC}}. \end{aligned} \quad (34)$$

From Eqs.(10) and (32), in the case of the $2\times$ mode, the SC resistance of the proposed converter is a little larger than that of the conventional converter. For example, the difference between Eqs.(10) and (32) is R_{cnt}/D when the parameter $N = 3$ and $s = 2$. However, as Fig.10 shows, the difference between the proposed converter and the conventional converter in the efficiency of the $2\times$ mode is very small. On the other hand, in the conventional converter, the power efficiency decreases strongly by the regulation, because the conventional converter cannot provide other step-up modes.

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