

An On-Chip Analog Mixed-Signal Testing Compliant with IEEE 1149.4 Standard Using Fault Signature Characterization Technique

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ABSTRACT

An on-chip analog mixed-signal testing, compliant with IEEE 1149.4 standard is presented. The testing technique is based on sinusoidal output response characterizations, yielding a complete detection of AC and DC fault signatures without a need for simulation-before-test process. The testing system is an extension of IEEE 1149.4 standard, and affords functionalities for both pre-screening on-chip and high-quality off-chip testing. A 4th-order low-pass Gm-C filter was employed as a circuit-under-test, and implemented with the proposed testing approach in a physical level using 0.18- μ m CMOS technology, and simulated using Hspice. The maximum operating frequency of the testing circuit is 260MHz. Both catastrophic and parametric faults are potentially detectable with low performance degradation. The fault coverage of faults associated in CMOS and capacitors are relatively high at 94% and 100%, respectively.

Keywords: On-Chip Analog Mixed-Signal Testing, IEEE 1149.4 Standard, Fault Signature Characterizations

1. INTRODUCTION

The emergence of modern system-on-chip (SOC) technology has led to a continuous increase in quantity and diversity of integrated components. Consequently, testing in both product development and mass-production phases of SOC has become more challenging, and now constitutes a major portion of overall cost. On-chip testability features have received considerable attention as a means of reducing testing time and eliminating the necessity for external Automatic Testing Equipment (ATE). Several early on-chip testing techniques have been applied successfully in digital circuits in which standard stuck-at fault models are utilized [1]. However, on-chip testing in analog mixed-signal systems is relatively complicated owing to performance degradation and in-

decipherable fault models. Accordingly, testing design approaches taken in analog mixed-signal systems have recently been of much interest to research efforts. These design approaches can be considered in two aspects, i.e. testing technique and system implementation.

One design aspect is the testing technique. Two major testing techniques are current and voltage sensing techniques. On the one hand, the current sensing technique, commonly referred to as IDDQ and IDDT current sensors [2-3], is relatively simple and suitable for detecting bridging faults. However, a Circuit-Under-Test (CUT) may suffer from power supply variation, and inappropriate setting of reference currents may affect the precision of fault detection. On the other hand, the voltage sensing techniques support non-intrusive implementation, and offer suitability with acceptable fault coverage for most types of circuits. This voltage sensing techniques can be classified into DC voltage sensing such as the built-in voltage sensor [4] and the VDDQ scheme [5], and AC output response characterizations such as sub-sampling [6], absolute value difference [1], on-chip spectrum analyser [7], and $\Sigma\Delta$ modulator [8]. However, input stimulus is necessary and some hard-to-detect faults may imperceptible at output voltages.

Another design aspect is the testing system implementation, involving off-chip and on-chip realizations. The techniques in [4,5,6,7,8] realize on-chip fault signature sensing circuitries, but fault analysis and detection are accomplished off-chip using measurement devices and digital signal processing. In addition, the IEEE 1149.4 standard also provides the internal circuit accessibility for enhancing the off-chip testing through analog access ports and internal test buses [10-11]. On the other hand, the testing techniques in [1,9] are based on built-in self-test (BIST), in which both stimulus generation and response verification are accomplished entirely on-chip through built-in hardware. Despite the fact that no external measurement devices are needed, large area overhead encountered in BIST for the registration of test pattern generation and fault-free bit streams presents a major difficulty.

Consideration of these two design aspects points to a demand for testing techniques with acceptable fault coverage and low performance penalties, implemented in a system that offers both on-chip testing

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for pre-screening of defective chips and off-chip for high-quality testing of some critical analog circuits. Therefore, this paper presents a new on-chip analog mixed-signal testing approach. The proposed testing technique is based on a fault signature characterization, offering a complete detection of AC and DC fault signatures. The testing system implementation, providing both on-chip and off-chip testing, is standardised through an extension of the IEEE 1149.4 mixed-signal test bus standard by modifying an analog boundary module, and utilizing all existing facilities. A complete testing system for a base-band Gm-C filter is demonstrated through physical-level implementations using 0.18- μm CMOS technology and simulations using Hspice.

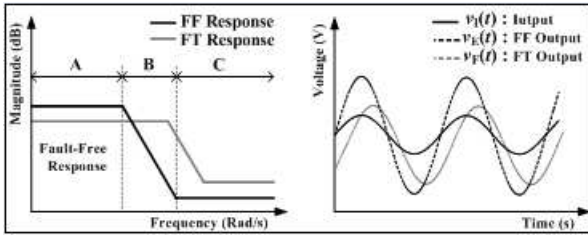


Fig.1: Illustrations of frequency responses and transient waveforms of fault-free (FF) and faulty (FT) CUTs.

2. PROPOSED ON-CHIP FAULT SIGNATURE CHARACTERIZATION TECHNIQUE

The proposed test technique has been designed for the on-chip testing of analog integrated circuits in mixed-signal systems, incorporating the IEEE 1149.4 analog boundary scan standard. This technique employs a sinusoidal signal, which is a common operating signal in most types of analog circuits, as an input test stimulus. The output response that may contain a fault signature, i.e. a circuit response to the presence of faults, is subsequently characterized in time domain for fault detection. The details of test approach, including an input stimulus and output response characterization, are presented in this section.

2.1 Sinusoidal Test Stimulus and Output Responses

The sinusoidal input test stimulus, denoted as $v_I(t)$, is typically expressed as

$$v_I(t) = V_i + v_i \sin(\omega_i t + \Phi_i) \quad (1)$$

where V_i is DC offset level in Volts, v_i is amplitude in Volts, ω_i is frequency in Radians, and Φ_i is phase shift in Degrees. The setting of sinusoidal parameters of the input stimulus $v_I(t)$ in (1) depends on the actual functions of CUTs. The DC level V_i and

the amplitude v_i are generally determined based on circuit performances and operations. However, the input frequency ω_i plays an important role in fault detection capability, and the setting of input test frequency is therefore particularly investigated.

Fig.1 illustrates the frequency responses and the transient waveforms of faulty and fault-free CUTs, which are particularly demonstrated as a low-pass characteristic. As shown in Fig.1 a, faults that exist in the CUT may cause changes in frequency responses. The fault-free frequency response is divided into three regions for the approximate investigation, including the low frequency region (A), the transition region (B), and the high frequency region (C). Setting the frequency of an input test stimulus in regions A and B are suitable since the output amplitude is sufficient for fault monitoring. In particular, region B is suitable for parametric fault detection since parameter variations may cause changes in corner frequency and phase shift. Region C may not appropriate for testing process due to relatively low output amplitude. This work therefore realists the test frequency in two regions A and B. Noted that complex frequency response can be divided into any number of regions, depending on the actual transfer functions of CUTs, and multiple frequency tests can also be made for high fault coverage.

As shown in Fig.1 (b), when applying $v_I(t)$ to a fault-free CUT, the expected output signal, denoted as $v_E(t)$, generally remains a sinusoid, i.e.

$$v_E(t) = V_e + v_e \sin(\omega_e t + \Phi_e) \quad (2)$$

This $v_E(t)$ may differ from $v_I(t)$ in terms of signal parameters (V_e , v_e , ω_e , and Φ_e), depending on specific operating conditions such as amplitude amplification or frequency filtering. However, when applying $v_I(t)$ to a faulty CUT, the presence of faults cause changes in $v_E(t)$. Parametric faults, including gate-oxide shorts and process variations, cause output parameter deviation that exceeds acceptable tolerances. In addition, catastrophic faults, including mainly resistive shorts and potential opens, cause circuit operation failures by generating extremely deformed sinusoids or DC outputs. As a result of the presence of faults, a general form of fault signatures denoted as $v_F(t)$ can be expressed as

$$V_F(t) = v_f + v_f \sin(\omega t + \Phi_f) + \sum v_f^n \sin(n\omega_f t + \Phi_{f,n}) \quad (3)$$

Three major components are a DC offset voltage V_f , a major tone signal, i.e. $v_f \sin(\omega_f t + \Phi_f)$, and distortion components, i.e. $\sum v_f^n \sin(n\omega_f t + \Phi_{f,n})$. Characteristics of this $v_F(t)$ differ from $v_E(t)$ by exhibiting some changes in parameters, ranging from small variations to DC outputs. Therefore, this work realizes the comparison between the signals $v_E(t)$ and $v_F(t)$ for fault detection.

2.2 Fault Signature Characterization Technique

This testing technique detects faults through the changes of $v_F(t)$ with reference to $v_E(t)$. Two threshold voltages V_H and V_L are proposed and utilized for fault signature characterizations. All possible characteristics of fault signatures are initially analyzed, offering high fault observability and eliminating the need for pre-simulation of actual fault signatures. Fault detection is performed by monitoring the values of crossing time difference between signals $v_E(t)$ and $v_F(t)$ at V_H , i.e. $\Delta t_H = |t_a - t_c|$, and V_L , i.e. $\Delta t_L = |t_b - t_d|$, where t_a and t_b are time when $v_E(t)$ crosses over V_H and V_L , respectively, and t_c and t_d are time when $v_F(t)$ crosses over V_H and V_L , respectively.

The setting of V_H and V_L depends on the DC level and amplitude of the input test stimulus so that the time differences can be observable. Setting the value V_H and V_L to approximately 60% to 70% of the positive and negative peaks of the input stimulus, respectively, has found to be suitable for detecting the time differences. The characterization procedure classifies fault signatures into two cases, depending on the amplitude of $v_F(t)$. Case 1 is a small parameter variation, which is defined as occurring when the maximum and minimum amplitudes of $v_F(t)$ cross over both V_H and V_L . Case 2 is any occurring of amplitude reduction when there is no amplitude crossing V_H , V_L , or both of these V_H and V_L .

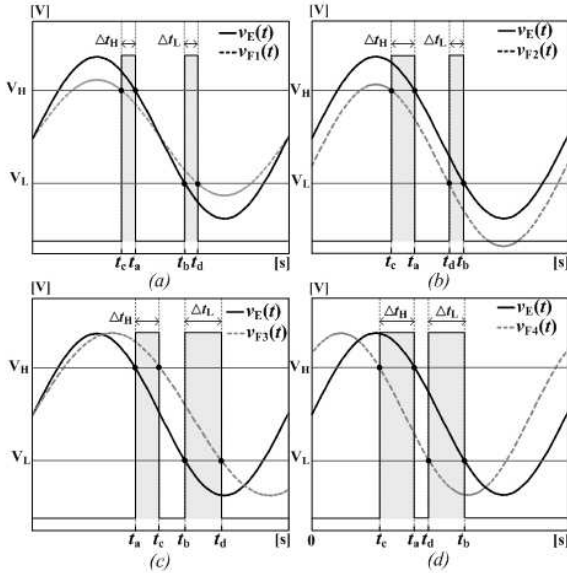


Fig.2: Characterization process for fault signatures in Case 1: Sinusoidal parameter variations.

Fig.2 shows the characterization procedure of fault signatures in Case 1. Four parameters are measured, including DC level, amplitude, frequency, and phase shift. For the sake of simplicity, the monitoring is demonstrated in the region of $T/4$ to $3T/4$ where T

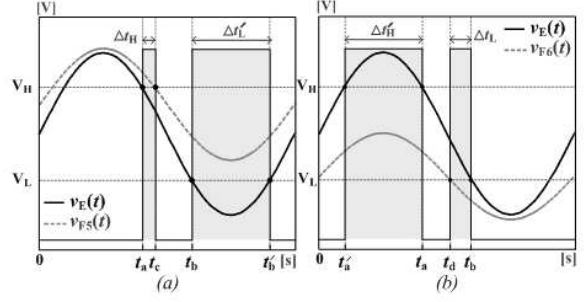


Fig.3: Characterization process for fault signatures in Case 2: Amplitude reduction.

is a signal period. Fig.2 (a) shows the signal $v_{F1}(t)$ with a decrease in amplitude and shows that the values of Δt_H and Δt_L are equal. Increases in amplitude also exhibit similar characteristics. Fig.2 (b) shows the signal $v_{F2}(t)$ with a decrease in DC offset level and reveals that Δt_H is greater than Δt_L . In cases where the DC offset increases, Δt_H is smaller than Δt_L . Fig.2 (c) shows the signal $v_{F3}(t)$ with a decrease in frequency, and shows that Δt_H is less than Δt_L . In cases where the frequency is higher, Δt_H is greater than Δt_L . Fig.2 (d) shows the signal $v_{F4}(t)$ with phase lagging behaviour and shows that Δt_H and Δt_L are equal. Phase leading behaviour also exhibits similar characteristics. Noted that distorted signals can also be detected in the same manner to these variations in the four parameters.

Fig.3 shows two examples of characterization procedures of fault signatures in Case 2. The time differences are investigated throughout the signal period. Fig.3 (a) shows the signal $v_{F5}(t)$ with no amplitude crossing over V_L . The time difference Δt_H is detectable as demonstrated in Fig.2 (a).

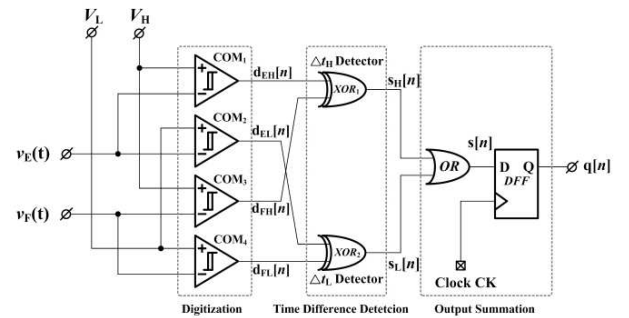


Fig.4: Circuit diagram of the test circuit based on the fault signature characterization technique.

Although the time t_c cannot be obtained, the additional Δt_L can be detected between time t_b and the subsequent t_b' . Fig.3 (b) demonstrates the signal $v_{F6}(t)$ with no amplitude crossing over V_H . The time difference Δt_L is also detectable as demonstrated in Fig.2 (a). The additional Δt_H is also introduced be-

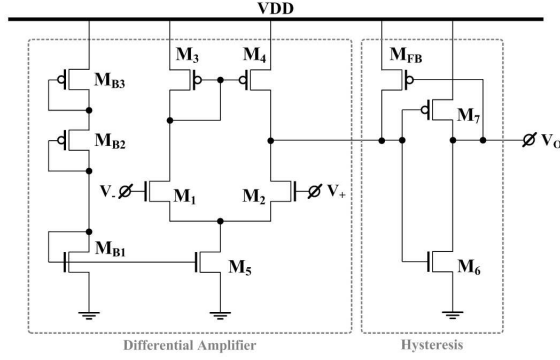


Fig.5: Circuit configuration of the comparator with hysteresis.

tween time t_a and the preceding t_a' . In addition to this two demonstrating cases, some faults may exhibit tremendous changes in sinusoidal characteristics such as a noise-like shape, a DC offset, stuck-at-ground, and stuck-at- V_{DD} . These faults can potentially be detected throughout the signal period since there is no crossing over both V_H and V_L .

Fig.4 shows the circuit diagram of the testing circuit implemented based on the fault signature characterization technique. As shown in Fig.4, fault detection procedures are performed consecutively in three processes, including the digitization, the time difference detection and the output summation. Initially, the signals $v_E(t)$ and $v_F(t)$ are digitized through four comparators COM1 to COM4, which are operating as simple 1-bit digitizers. The signal $v_E(t)$ is digitized against V_H through COM_1 and COM_2 , providing two sets of digital output signals $d_{EH}[n]$ and $d_{EL}[n]$, respectively. The signal $v_F(t)$ is also digitized against V_L through COM_3 and COM_4 , providing two sets of digital output signal $d_{FH}[n]$ and $d_{FL}[n]$, respectively. Subsequently, comparison is performed for detecting the values of Δt_H and Δt_L through two XOR gates X_1 and X_2 , respectively. This detection simply monitors the difference between logics 1 and 0, and reports the outputs as 1 when the two inputs have difference logic values. In this process, the comparison of $d_{EH}[n]$ and $d_{FH}[n]$ yields Δt_H , reporting as $s_H[n]$, while comparison of $d_{EL}[n]$ and $d_{FL}[n]$ yields Δt_L , reporting as $s_L[n]$. Finally, the summation of two fault signatures, including $s_H[n]$ and $s_L[n]$ are carried through OR gate out in order to report a single test output $s[n]$. This test output signal $s[n]$ is conveyed to the DFF in order to report a digital output $q[n]$ that cooperates the clock system. Fig.5 shows the circuit configuration of the comparator with hysteresis employed in Fig.4. This comparator is implemented by a simple differential amplifier, consisting of transistors M_1 to M_5 , and a hysteresis, consisting of M_6 and M_7 , and a long-channel M_{FB} . The biasing circuit is formed by transistor M_{B1} , M_{B2} and M_{B3} . In addition, the digital logic gates in Fig.4 were im-

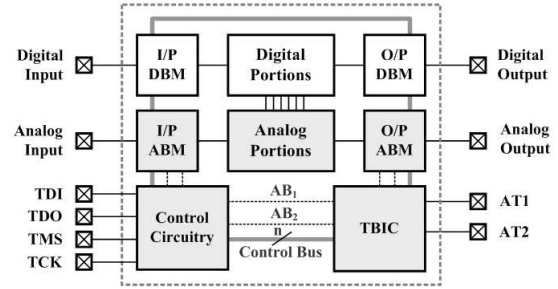


Fig.6: Block diagram of an analog mixed-signal system with IEEE 1149.4 test bus standard.

plemented by standard cells.

3. IEEE 1149.4 STANDARD-BASED TESTING SYSTEM IMPLEMENTATION

Fig. 6 shows the block diagram of the existing IEEE 1149.4 standard architecture, affording four components for testing a mixed-signal system as follows. First, a Digital Boundary Module (DBM) scans targeting digital CUTs, and shifts test data serially. Second, an Analog Boundary Module (ABM) provides internal bus connections to targeting analog CUTs. Third, a Test Bus Interface Circuit (TBIC) connected to two analog access ports (AT1 and AT2) distributes analog test signals to ABMs via two internal buses (AB1 and AB2). Last, a control circuitry controls the operation of the overall test system by means of four control signals; Test-Data-In (TDI), Test-Data-Out (TDO), Test-Clock (TCK), and Test-Mode-Select (TMS). Despite the fact that these existing ABM and TBIC potentially enable the accessibility to internal nodes for an external test operation (EXTTEST), several restrictions in analog mixed-signal testing still remain, involving the requirement for duplicated ABMs at all pins, the lack of multiple pin accessibility at one time, and particularly the lack of an internal test operation (INTEST). Consequently, the extensions to IEEE 1149.4 standard have recently been proposed as for a solution of these restrictions. The bridge-for-testability technique [10] was developed for reducing the number of duplicated ABMs. The modified ABM in [11] provides the multiple pin accessibility as well as INTEST capability, specifically for bridging fault testing. It has also been reported that the output of built-in V_{DDQ} and I_{DDQ} monitoring can be scanned out in compliant with the IEEE 1149.4 standard [5]. However, no complete parametric and dynamic INTEST capability with increased observability for both AC and DC fault signatures has been investigated. Consequently, this work aims to resolve this restriction through the extension of the IEEE 1149.4 architecture, and find a suitable testing circuit that can exploit existing facilities including DC voltages, internal test buses and access

ports.

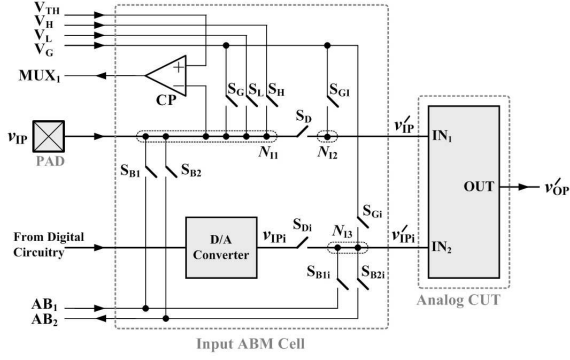


Fig.7: Circuit configuration of the input ABM cell.

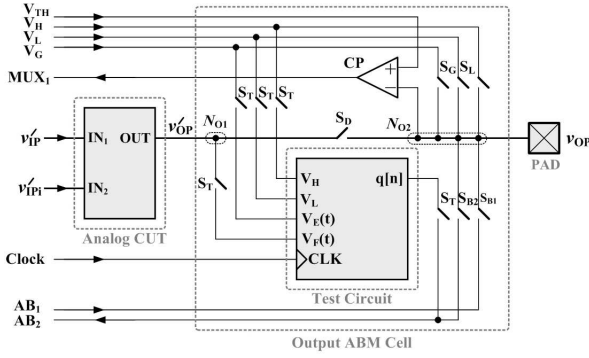


Fig.8: Circuit configuration of the output ABM cell.

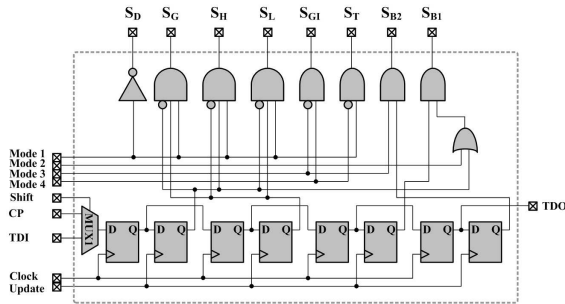


Fig.9: Circuit configuration of the control circuitry.

Fig. 7 shows the circuit configuration the input ABM cell. The analog CUT in Fig.7 is an analog functional block synthesized from mixed-signal systems, such as amplifiers and filters, where primary inputs can be either an external input v_{IP} or an internal v_{IPi} obtained from a D/A converter. The input ABM is located at the input pin, comprising mainly the voltage comparator CP and the switches S_D , S_G , S_L , S_H , S_{B1} , S_{B2} , and S_{GI} . In addition, an internal switching network located between the outputs of an internal A/D converter is also included and composed by switches S_{Di} , S_{B1i} , S_{B2i} , and S_{GII} , offering of testing accessibility in the case where v_{IPi} is realized. As

will be seen later, this input ABM cooperates with three modes, except Mode4.

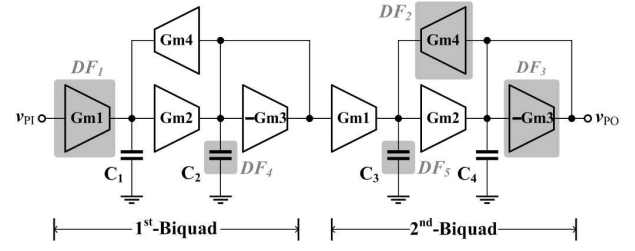


Fig.10: Block diagram of the 4th-order Gm-C filter.

Fig. 8 shows the circuit configuration the output ABM cell with extended functionality for on-chip and off-chip testing capability. The output ABM is located at the output pin and composed by the same components utilized in the input ABM except for the switch S_{GII} , and the testing circuit described in Fig.4 with seven control switches S_T . These ABMs is capable of four modes of operations as follows. Mode 1 is a traditional digital scan mode where the switches S_D , S_G , S_L , S_H of both input and output ABMs are operating, corresponding to TDI signals, while other switches are opened. This Mode 1 allows the ABM to operate as the DBM by detecting bridging faults at the output terminal through the comparator CP and shifting to the serial digital test bus.

Mode 2 is a traditional external analog test mode where the switches S_{B1} of the input ABM and S_{B2} of the output ABM are closed, while other switches are opened. The input signal stimulus sourced at the port AT_1 is contributed to the CUT through the bus AB_1 . The output response from the CUT is provided at the bus AB_2 and subsequently conveyed to the port AT_2 for the external testing. Mode 3 is an extended external analog test mode improved from [10] where the switch S_{GI} of the input ABM is closed and the alternative input is sourced at V_G terminal. This mode 3 provides the multiple-pin accessibility at one time by means of the direct access to the CUT and the disconnection of input ABM and internal test buses. The corresponding output can be monitored separately at the output pin by closing the switch S_D of the output ABM.

Mode 4 is an extended on-chip testing mode using the proposed signal characterization technique where the switches S_D and S_{B1} of the input ABM are closed and all switches S_T of the output ABM are closed, and others are opened. The input signal stimulus $v_I(t)$ sourced at the port AT_1 is contributed to the CUT through AB_1 . The fault signature $v_F(t)$ obtained from the CUT at node N_{O1} and the expected signal $v_E(t)$ sourced at the port V_G are conveyed to the testing circuit. Subsequently, the test circuit processes signal characterizations and provides the test output to the output node N_{O2} . As the test circuit

reports the faultiness by logic 1, the comparator CP₂ subsequently captures the voltage at node N_{O2} is then loaded in to the serial interface in order to complete a boundary scan throughout the system. This test output also visible at the port AT₂ conveyed by the bus AB₂. Fig.9 shows the circuit diagram of the control circuitry. As utilized in the exiting IEEE 1149.4 standard, control and update shift registers, are utilized for loading control instruction and test data.

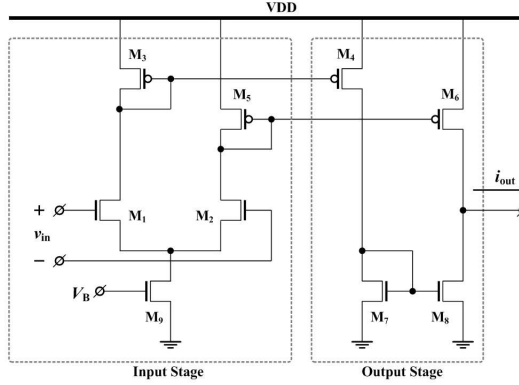


Fig.11: Circuit diagram of the OTA.

However, the decoding logic is specially designed for accomplishing the four modes of operations. The decoded signals are exploited for controlling all the switches.

4. DEMONSTRATIONS AND SIMULATION RESULTS

The proposed circuits and the extended IEEE1149.4 standard architecture were implemented in a physical level using 0.18- μ m standard CMOS technology in Cadence environments, and simulated using Hspice. For purpose of demonstrations, the demonstrating CUT is a low-pass G_m -C filter. This G_m -C low-pass filters have extensively been utilized in base-band sections of RF receivers, and generally implemented by means of CMOS LSI chips owing to the capability to operate at higher frequency compared to passive RC filters. Fig. 10 shows the block diagram of the 4th-order low-pass G_m -C filter, comprising a cascade connection of two identical 2nd-order G_m -C biquads. The values of G_{m1} , G_{m2} and G_{m4} are equal, while the value of G_{m3} is twice, i.e. $2G_{m3} = G_{m1} = G_{m2} = G_{m4}$. The values of capacitors C_1 and C_2 are equal. The values of capacitors C_3 and C_4 are also equal. These capacitors were implemented by linear on-chip capacitors.

Fig. 11 shows the circuit configuration of a CMOS operational transconductance amplifier (OTA) [12], which is utilized as the G_m block in the CUT. The OTA comprises three major components, i.e. (1) an nMOS differential pair formed by transistors M₁ and M₂, (2) two pMOS current mirrors formed by transistors M₃ to M₆, and (3) an nMOS current mirror

formed by transistors M₇ to M₈. This OTA employs a single power supply voltage V_{DD} . Input and output signals are a voltage signal v_{in} and a current i_{OUT} , respectively.

Fig.12 shows the physical layout design of the CUT. There are eight sets of CUTs, including two fault-free CUTs without ABM (FF-CUT_{EXC}), one fault-free CUT with ABM (FF-CUT_{INC}), and five faulty CUTs with ABM (FT-CUT_{INC}). In these five sets of FT-CUT_{INC}, realistic faults were randomly injected into the layout.

Three examples are defects in MOS transistors of OTAs considered from critical areas in the designed layout,

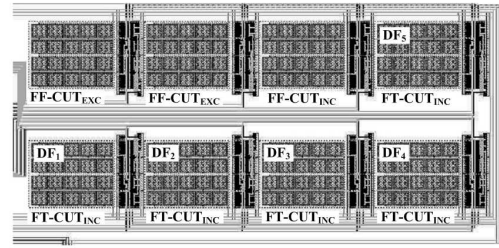


Fig.12: Physical layout design of the CUTs.

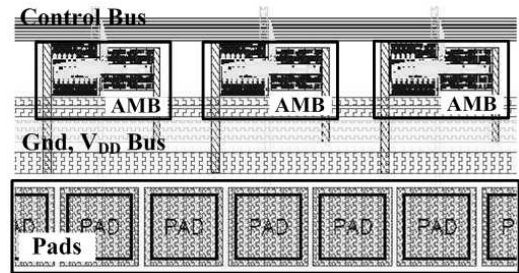


Fig.13: Physical layout design of ABM, demonstrating the contributions of ABM at the pads.

including an internal metal layer bridge (DF₁) at G_{m1} , a metal crack (DF₂) G_{m4} , and a floating gate (DF₃) at G_{m3} . Other two examples are capacitance variation (DF₄) at C_2 and the potential open (DF₅) at C_3 . Fig.13 shows the physical layout design of ABM where the contributions of three ABMs at the output pads are particularly illustrated.

Table 1 summarizes the performances of the testing circuit previously shown in Fig.4. As shown in Table 1, the comparators are capable for a wide comparison region of 0.2 V to 1.6V with a relatively low offset error of 0.042V throughout the entire region. Consequently, the voltages V_H and V_L can be widely adjustable through this comparison region, depending on the actual amplitude of a sinusoidal test stimulus. The maximum operating frequency of the testing circuit is 260 MHz. By using the low-frequency test stimulus $v_I(t) = 0.9 + 0.5 \sin(2\pi 1000t)$, the minimum

value of sinusoidal parameter variations that were detectable was found at 0.5%. Therefore, parametric faults in the tolerance band of $\pm 5\%$ are potentially detectable.

Table 2 shows the comparison of performances between two cases of fault-free CUTs, i.e. a primitive CUT (FF-CUT_{EXC}) and a CUT with the inclusion of the IEEE1149.4 standard testing system (FF-CUT_{INC}). This comparison was performed in order to validate testing operations, and investigate performance penalties. As shown in Table 2, the FF-CUT_{EXC} has the cut-off frequency and DC gain at 11MHz and 4 dB, respectively. Although the performances deviation are expected to be introduced by additional stray capacitances and on-resistances of switches, the deviations in percentage are relatively low, i.e. the deviations of the DC gain and the linearity of input-output signal transfer curve were found at 0.0025% and 0.895%, respectively. No deviation of the cut-off frequency was evident. It can be concluded that the proposed testing system affects low impacts on primitive CUTs.

Table 1: Summary of performances of the testing circuit shown in Fig.4.

Testing Circuit Performances		Values	Units
Comparator Performances	Maximum value of V_H	1.6	V
	Minimum value of V_L	0.2	V
	Offset Error	0.042	V
Minimum Detectable Variation		>0.5	%
Maximum Operating Frequency		260	MHz

Table 2: Comparisons between a primitive CUT and a CUT with IEEE1149.4 standard.

CUT Performances	Simulated Performances			
	FF-CUT _{EXC}	FF-CUT _{INC}	Dev. (%)	Units
Cutoff Frequency	11	11	-	MHz
DC Gain	4	3.99	0.0025	dB
Linearity	0.0067	0.00664	0.895	%

Table 3: Summary of number of faults, detected and undetected faults, and fault coverage.

Fault Types	No. of Faults	Fault Simulation Results			
		At $f_i = 1$ kHz		At $f_i = 11.2$ MHz	
		Detected	Fault Coverage	Detected	Fault Coverage
(a) OTA (Catastrophic)	352	331	94.03%	334	94.87%
(b) Capacitors (Catastrophic)	8	8	100%	8	100%
(c) Capacitors ($\pm 15\%$ Var.)	8	8	100%	8	100%

Fault injections were realized at the transistor level by the insertion of resistor technique in order to simulate the electrical behaviour of shorts and opens. Shorts were modelled by connecting a small resistor of 1Ω between each pair of terminals, including Gate-Drain Short, Gate-Source Short, and Drain-Source Short. Additionally, opens were modelled by inserting a parallel combination of a large resistor of $10M\Omega$ and a small capacitor of 1 pF in series into each terminal, including Drain Open and Source Open. The Gate Open was specially modelled by means of grounded $10-M\Omega$ resistors and 1-pF capacitors at the two disconnecting terminals in order to eliminate the voltage discontinuity in appropriate simulation in Hspice. The capacitor shorts and opens were also modelled in the similar manner to transistors. In the test procedure, the layout of fault-free CUT was initially extracted to obtain the transistor-level netlist.

Table 3 summarizes number of faults, detected and undetected faults, and fault coverage in percentages. The simulation of fault injections, only one fault was injected in the CUT while other circuit elements and parameters are kept at their designed values. As the cut-off frequency of the filter is at 11 MHz, two test frequencies, i.e. a low frequency of 1KHz and a high frequency of 11.2 MHz, were realised. As seen from Table 3, the fault coverage of faults associated in OTA is relatively high at approximately 94% for both frequencies. Some undetected faults in OTAs were considered as hard-to-detect faults, such as transistor gate opens, which do not produce fault signatures at the output waveforms. The CUTs that have these hard-to-detect faults can be considered as non-defective CUT in the pre-screening process of fault detection. Catastrophic faults and parameter variation of 15% of capacitors were completely detected, yielding fault coverage of 100%. In addition, those five realistic faults described in Figs. 10 and 12 (DF₁ to DF₅) were also detected.

5. CONCLUSIONS

A new on-chip analog mixed-signal testing compliant with IEEE 1149.4 standard has been presented. The testing technique based on sinusoidal output response characterizations yields a complete detection of AC and DC fault signatures. The testing system extended from IEEE 1149.4 standard affords functionalities for both pre-screening on-chip and high-quality off-chip testing. A demonstrating a 4th-order low-pass Gm-C filter, with the proposed testing approach is fully implemented in a physical level using 0.18- μm CMOS technology, and simulated using Hspice. The maximum operating frequency of the testing circuit is 260MHz. Both catastrophic and parametric faults are potentially detectable with low performance degradation. The fault coverage of faults associated in CMOS and capacitors are relatively high at 94% and 100%, respectively.

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