

# A Low-Cost High-Speed Pulse Response Based Built-In Self Test For Analog Integrated Circuits

Wimol San-Um<sup>1</sup> and Tachibana Masayoshi<sup>2</sup>, Non-members

## ABSTRACT

This paper presents a pulse response-based built-in self test technique and implementation for the testing of analog integrated circuits in mixed-signal systems. This BIST technique employs two narrow width pulses as input stimuli, and monitors two voltage samples on pulse response waveform for fault detection through allowable tolerances. The BIST system implementation realizes a programmable delay line for generating pulse stimuli, and a sample-and-hold circuit with comparators for fault detection process. Demonstrations of the testing for a Sallen-Key low-pass filter using 0.18- $\mu$ m CMOS technology yields relatively high fault coverage. The fault coverage of catastrophic faults is 100%, and the fault coverage of capacitor and resistor variations are 93.75% and 87.5%, respectively. The proposed BIST technique uses low testing time within two short pulse response waveforms, and offers low implementation cost since on-chip sinusoidal stimuli, test algorithms, and external digital processing unit are not necessary.

**Keywords:** Built-In Self Test, Analog Testing Technique, Narrow Width Pulse Stimulus, Pulse Response Sampling

## 1. INTRODUCTION

The emergence of modern System-On-Chip (SOC) technology has led to a continuous increase in quantity and diversity of integrated components. As the complexity of this SOC technology has grown, testing in both product development and mass-production phases have become more challenging, and now constitutes a major portion of overall cost. Although the testing process has been commercialized by means of an Automatic Testing Equipment (ATE), this process is expensive and time-consuming. In particular, testing cost of embedded analog circuits in SOC technology is relatively high compared to total analog circuit manufacturing costs. Therefore, there is

a demand for cost-effective test techniques with low testing time.

On-chip testing capability of integrated circuits has received considerable attention as a means of reducing testing time and eliminating the necessity for external ATEs. Several on-chip testing techniques have been applied successfully in digital circuits in which each level of abstraction, ranging from a behavioral description to logic layout, is verified against the immediate preceding levels. With the support of rigorous mathematical expression such as Boolean expressions or high-level programming language constructs, single stuck-fault models are commonly utilized, and test-pattern algorithms have been developed comprehensively with acceptable fault coverage. As opposed to testing in digital circuits, testing in analog circuits is complicated owing to not only instantaneous continuous-time analog response of signal values, but also non-linear characteristics and broad variations in circuit parameters. This complicated characteristics lead to difficulties in analog circuit testing, including vulnerability to performance degradation and indecipherable standard fault models.

Accordingly, the on-chip testing techniques for analog circuits in mixed-signal systems have recently been attractive for research efforts. Therefore, this paper presents a Built-In Self Test (BIST) technique as a new alternative for the pre-screening test of defective analog integrated circuits in mixed-signal systems. This paper is organized into eight sections as follows. Section 2 provides a review on existing on-chip testing techniques and system implementations. Section 3 describes fault models and shows preliminary evaluations of fault influences. Section 4 proposes the pulse response-based BIST technique. Section 5 presents the BIST system implementation and circuit realizations. Post-layout simulation results are provided in Section 6. Comparison and conclusion are finally provided in Sections 7 and 8, respectively.

## 2. EXISTING ON-CHIP TESTING TECHNIQUES AND SYSTEM IMPLEMENTATIONS

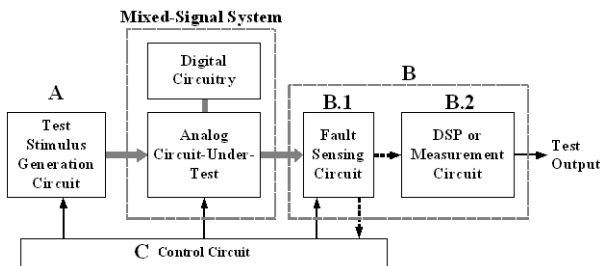
Fig.1 depicts a generalized testing scheme of analog integrated circuits in mixed-signal systems. This scheme consists of three major blocks, i.e. the test stimulus generation circuit (A), the output response

Manuscript received on July 14, 2009 ; revised on October 23, 2009.

<sup>1,2</sup> The authors are with The Electronic and Photonic System Engineering, Kochi University of Technology (KUT), Tosayamada-Cho, Kami-City, Kochi, 782-8502, Japan. Tel: (+81)-887-57-2212, E-mail: 118002m@gs.kochi-tech.ac.jp and tachibana.masayoshi@kochi-tech.ac.jp

analysis circuit (B), including the fault sensing circuit (B.1) and the Digital Signal Processing (DSP) or measurement circuits (B.2), and the test control circuit (C). The development of testing system design approaches based on this scheme can be considered in two aspects, i.e. testing technique and testing system implementation.

One design aspect is the testing technique, which relates to fault signature sensing and fault extraction methods for the design of fault-sensing circuit block B.1. These testing techniques can be classified into either current or voltage sensing techniques. The current sensing



**Fig.1:** A generalized testing scheme of integrated analog circuits in mixed signal systems.

techniques [1-3], commonly referred to as IDDQ current sensors, are relatively simple as no test stimulus block A is required, and suitable for detecting bridging faults. However, a Circuit-Under-Test (CUT) may suffer from power supply variations caused by a shunt resistive component connected between the CUT and power supply (or ground), and inappropriate setting of reference currents may also affect the precision of fault detection owing to a broad range of faulty currents [4]. On the other hand, the voltage sensing techniques include the DC voltage sensing such as the built-in voltage sensor [5] and the VDDQ scheme [6], and the AC output response sensing such as sub-sampling [7], absolute value difference [8], on-chip spectrum analyzer [9], and  $\Sigma\Delta$  modulator [10]. These voltage sensing techniques support non-intrusive implementation, and offer suitability for most types of circuits as fault signatures are obtained from observation nodes with no modification of the existing CUT. Nevertheless, some faults are imperceptible at output voltages, and the test stimulus generation circuit block A is necessary excepted in the oscillation-based test [11].

Another design aspect is the testing system implementation of the testing techniques mentioned earlier, involving a Design-For-Testability (DFT) that provides an early on-chip fault sensing functionality for the external fault detection, and the BIST that provides a complete on-chip testing functionality. The techniques in [1-6] are based on the DFT in which the fault signature sensing circuitry block B.1 is realized on-chip, but the test stimulus block A and the

fault detection block B.2 are accomplished externally. Despite the fact that this DFT provides a testing capability with low area overhead, external test stimuli and response analyzers are necessary and therefore a complete self-testing process cannot be achieved. On the other hand, the testing techniques in [7-10] are based on the BIST in which all the blocks A, B.1, B.2 and C are accomplished entirely on-chip through built-in hardware. Neither external test stimulus generator nor external DSP unit is required for the BIST. In addition, self-testing capability of the BIST uses lower testing time than the external measurements as encountered in the DFT. However, large area overhead presents a major difficulty as test stimuli and fault-free bit streams are registered in extra memory units.

As a consequence of the consideration of these two design aspects, this work specifically focuses on the voltage sensing testing technique and the BIST implementation through the use of narrow width pulse stimulation and pulse response characterization. In general, the pulse stimulation testing enables a compact and controllable on-chip pulse generation, compiling with the central control circuitry, and provides fault signatures for fault detection in both time and frequency domains. Regarding this pulse stimulation-based testing, the pulse sequences with random widths obtained from a Linear Feedback Shift Register (LFSR) [12] and the pseudo-random pulse sequences [13] have earlier been employed for the implementation of low-cost BISTs. However, the LFSR-based technique requires complicated LFSR generation, synchronization and compaction circuits, while the technique based on pseudo-random pulse sequence requires a complex on-chip cross-correlation analysis prior to the fault detection process using the external DSP.

Recently, the simple pulse generation circuit based on a differentiator has been proposed in [14] for alleviating the complexity in on-chip pattern generations and cross-correlation operations. However, fault detection is performed statistically by means of linear regression analysis that necessitates specific algorithms and external software. In addition, the measurement of the voltage samples of analog responses using a microcontroller has also been proposed in [15] for low-cost BIST of embedded analog circuits in mixed-signal systems. This technique offers efficient fault diagnosis and localization with the necessity of microcontroller. Therefore, this work aims to develop a high-speed testing technique using a small number of pulse input stimulus while maintaining high fault coverage. In addition, this work also attempts to implement a BIST system with low implementation cost without the use of complex devices. The BIST implementation is expected to be compatible with mixed-signal systems by exploiting clocks and control signals from digital portion, and providing test output

in digital forms.

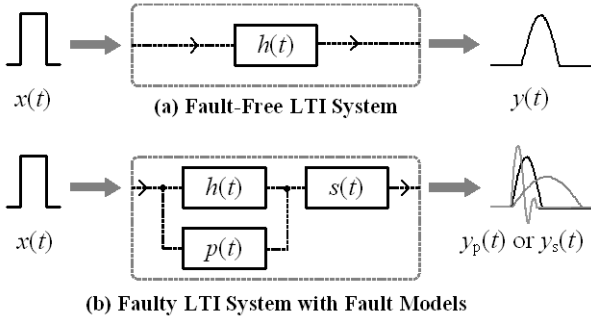
### 3. EVALUATIONS OF FAULT INFLUENCES ON LTI CIRCUITS

#### 3.1 Targeting Circuits and Fault Models

The proposed BIST technique deals with on-chip fault detection of a Linear-Time-Invariant (LTI) system. This LTI system, denoted as  $h(t)$ , was designated as a class of analog circuits in which the transfer function in frequency domain can be expressed as

$$H(s) = \frac{a_0 + a_1s + \dots + a_ns^n}{b_0 + b_1s + \dots + b_ns^n} \quad (1)$$

where  $n \leq m$  and the coefficients  $a_i$  and  $b_j$  are functions of circuit parameters,  $i = 1, 2, \dots, n$  and  $j = 1, 2, \dots, m$ . Examples of targeting analog circuits that possesses the transfer function described in (1) are analog amplifiers and filters in baseband receivers. Typically, LTI systems can be characterized entirely through a specific input function such as pulse or ramp input signals. This work realizes a narrow width pulse signal as an input stimulus due to the simple implementation using digital logic gates.



**Fig. 2:** Block diagrams of LTI systems; (a) fault-free LTI system, (b) faulty LTI system with fault models.

In order to describe the fault influences on pulse response waveforms, Fig.2 demonstrates the block diagrams of two LTI systems, including the fault-free LTI system and the faulty LTI system with parallel and serial fault models.

As shown in Fig.2 (a), the fault-free LTI system is characterized by the very narrow width pulse input signal  $x(t)$ , providing the output response signal  $y(t)$ . This output signal  $y(t)$  can be described mathematically through the convolution operation in time domain, i.e.  $y(t) = x(t) * h(t)$ , and expressed as

$$y(t) = \int_{-\infty}^{\infty} x(\tau)h(t - \tau)d\tau \quad (2)$$

where  $\tau$  is a dummy variable for integration. For a specific  $h(t)$  with a stationary input  $x(t)$ , this output  $y(t)$  described in (2) generally possesses a certain shape of pulse response waveforms over a limited time period.

Nonetheless, circuit operation failures resulting from catastrophic faults and performance degradation resulting from parametric faults may change the transfer function of the existing  $h(t)$ . As shown in Fig.2 (b), the faulty LTI system can be modeled by adding a parallel fault model  $p(t)$  and a serial fault model  $s(t)$  to the existing  $h(t)$  [13]. These fault models  $p(t)$  and  $s(t)$  can be considered in various aspects such as a constant value and a higher-order transfer function, depending on types of realistic defects in CUTs. Based on associative and distributive properties of the convolution operation, the faulty LTI system in Fig.2 (b) provides two cases of output signals, i.e.  $y_p(t)$  and  $y_s(t)$ , when a single fault model is considered. The output  $y_p(t) = x(t) * (h(t) + p(t))$  is provided by a system resulting from a parallel connection of  $h(t)$  and  $p(t)$ , and is given by

$$y_p(t) = \int_{-\infty}^{\infty} x(t)(h(t - \tau) + p(t - \tau))d\tau \quad (3)$$

The output  $y_s(t) = x(t) * h(t) * s(t)$  is provided by a system resulting from a serial connection of  $h(t)$  and  $s(t)$ , and is given by

$$y_s(t) = \int_{-\infty}^{\infty} \left( \int_{-\infty}^{\infty} x_{xh}(\tau)h_{hs}(\tau_{hs} - \tau_{xh})d\tau_{xh} \right) s(t - \tau_{hs})d\tau_{hs} \quad (4)$$

where  $x_{xh}$  is a pulse input signal considered in the convolution of  $x(t)$  and  $h(t)$ ,  $h_{hs}$  is a system function considered in the convolution of  $h(t)$  and  $s(t)$ ,  $\tau_{xh}$  is a dummy variable for integration associated with the convolution of  $x(t)$  and  $h(t)$ , and  $\tau_{hs}$  is a dummy variable for integration associated with the convolution of  $h(t)$  and  $s(t)$ . These two outputs in (3) and (4) are different from the fault-free output in (2) owing to the inclusion of fault models. Therefore, fault detection can be made possible through the outputs  $y_p(t)$  and  $y_s(t)$ .

Fault detection procedures through the outputs  $y_p(t)$  and  $y_s(t)$  can be made in either frequency or time domains. Fault detection in frequency domain generally employs de-convolution or cross-correlation techniques for extracting the actual fault functions of  $p(t)$  and  $s(t)$ . The CUT is considered as defective when the actual functions of  $p(t)$  and  $s(t)$  are found from the extraction process. Nonetheless, DSP unit with specific extraction algorithms is necessary, and the on-chip implementation requires large chip area for digital circuits and memories. This work therefore oppositely realizes fault detection in time domain. No extraction process for the actual fault models  $p(t)$  and  $s(t)$  is necessary. The fault detection procedure is based on the comparison of voltage samples obtained from pulse response waveforms between the fault-free output  $y(t)$  and faulty outputs  $y_p(t)$  and  $y_s(t)$ . The circuits is considered as defective when the voltage samples exceed the allowable tolerance ranges. Fault

monitoring in time domain enables the instantaneous detection process, yielding low testing time, and offers low-cost BIST with full on-chip implementation with a small number of simple components.

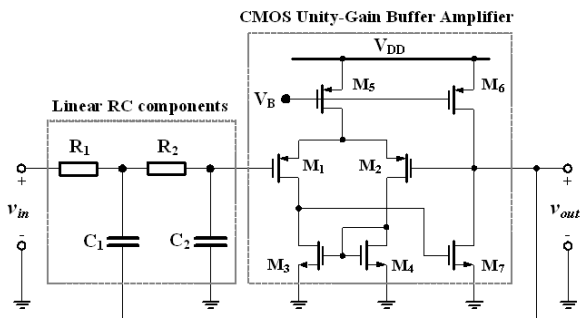
### 3.2 Preliminary Evaluations of Fault Influences

In order to investigate the fault influences on pulse response waveforms and to evaluate the effectiveness of the use of a narrow width pulse as an input test stimulus, defect-oriented simulations in schematic level were preliminarily conducted. The demonstrated CUT was a 2<sup>nd</sup>-order Sallen-Key low-pass filter, which offers high linearity and low-noise properties for the implementation of integrated analog base-band filters in RF receivers such as in IEEE 802.11 wireless LAN [16] or in CDMA receivers [17]. Fig.3 shows the circuit configuration of the Sallen-Key low-pass filter, comprising two major blocks, i.e. a linear RC network and a unity-gain buffer. The linear RC network is formed by two resistors ( $R_1, R_2$ ) and two capacitors ( $C_1, C_2$ ). The unity-gain buffer was implemented based on a two-stage differential amplifier, consisting of seven CMOS transistors ( $M_1$  to  $M_7$ ). The corresponding 2-pole Butterworth transfer function in s-domain denoted as  $H_f(s)$  can be expressed as

$$H_f(s) = \frac{(2\pi f_c)^2}{s^2 + \frac{2\pi f_c}{Q}s + (2\pi f_c)^2} \quad (5)$$

where the cutoff frequency ( $f_c$ ) and the quality factor ( $Q$ ) are given by

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \quad (6)$$



**Fig.3:** Circuit configuration of a second-order Sallen-Key low-pass filter employed as a demonstrating CUT.

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{C_2(R_1 + R_2)} \quad (7)$$

It is seen from (5) that the transfer function  $H_f(s)$  exhibits a 2<sup>nd</sup>-order LTI system, which satisfies the

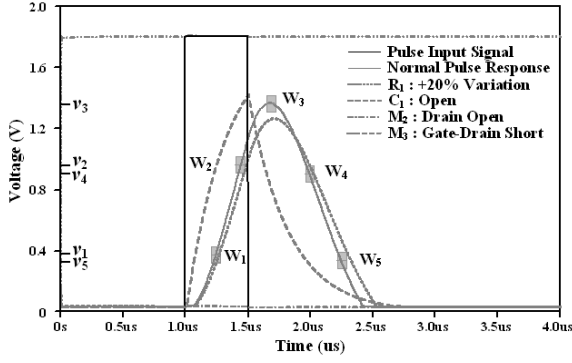
criteria of  $H(s)$  described in (1), and is therefore capable to provide the proper pulse response characteristics. As for example, an analog baseband filter with the cutoff frequency of 450 kHz to 500 kHz and a unity quality factor was designed. The values of the resistors  $R_1$  and  $R_2$  were equally selected at 84 k $\Omega$ , and the values of the capacitors  $C_1$  and  $C_2$  calculated using (6) and (7) were consequently equal to 8 pF and 2 pF, respectively, yielding the resulting cut-off frequency of 476 kHz. Through the use of a 0.18- $\mu$ m CMOS transistor model, the aspect ratios of transistors in the unity gain buffer were optimized for robust unity-gain and appropriate settling time. The width of the pulse input signal was set at 0.5  $\mu$ s. Since different types of CUTs exhibit different and specific transfer functions, this pulse width of 0.5  $\mu$ s was optimized from a trial and error process so that the output signal possesses a symmetric and narrow pulse response shape.

The injection of catastrophic and parametric faults was performed for fault coverage investigations. In the case of catastrophic faults, shorts and opens were realized by the insertion of a resistor into each component [18]. Shorts were modeled by inserting a small 1- $\Omega$  resistor in parallel between each pair of component terminals. Opens were modeled by inserting a large 10-M $\Omega$  resistor in series between two disconnecting terminals. In order to eliminate the voltage discontinuity at MOS gate terminals, the transistor gate opens were distinctively modeled by connecting a large 10-M $\Omega$  resistor to gate and disconnecting terminals with respect to the system ground. In the case of parametric faults, the component variation was realized where the practical component variations are in an extensive range from 10% to 50% [19-20]. In summary, the total number of 54 faults was investigated, including 13 faults in the linear RC network and 41 faults in the unity-gain buffer.

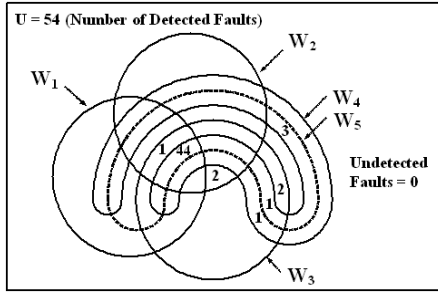
The discrimination of detected faults was done by means of window criterion. Detected faults were counted as when the voltage value exceeds the criterion thresholds, which are determined by voltage tolerances. The

propagation time of pulse response waveforms was particularly divided into six partitions for the approximate investigations of voltage samples at the peak and on charging and discharging periods. Therefore, five window criteria denoted as  $W_1$  to  $W_5$  were realized. The values of window criterion thresholds were carried out by considering  $\pm 5\%$  tolerance. The minimum and maximum thresholds of each window criterion were estimated by the worse case boundaries, i.e. the intervals between the maximum and the maximum values [3].

For purpose of demonstrations, Fig. 4 shows the transient waveforms of a normal pulse response and four examples of faulty responses. Such four examples of faults include +20% variation of  $R_1$ , open at  $C_1$ ,



**Fig.4:** Transient waveforms of a normal pulse response and four examples of faulty pulse response waveforms.

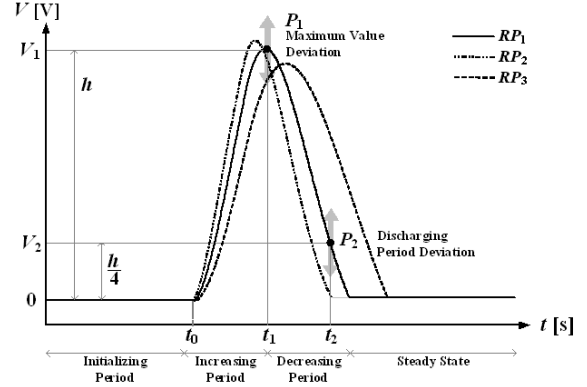


**Fig.5:** Venn diagram of the detected faults in five sets of window criteria  $W_1$  to  $W_5$ .

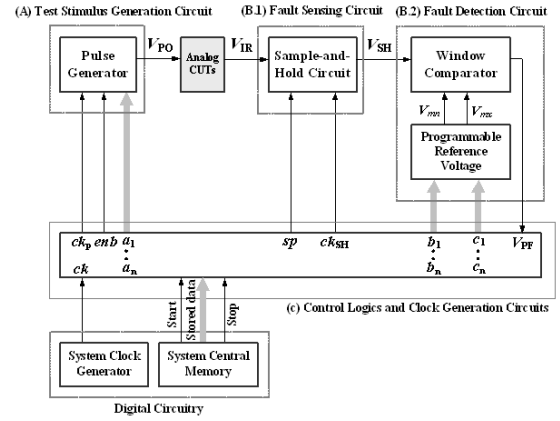
drain open at  $M_2$ , and gate-drain short at  $M_3$ . Five voltage values  $V_1$  to  $V_5$  were captured from the normal pulse response waveform, and employed as references for  $W_1$  to  $W_5$ , respectively. It is seen from Fig.4 that the variation in  $R_1$  causes small changes in charging and discharging periods, whereas shorts and opens in  $C_1, M_2, M_3$  cause tremendous changes in pulse response waveforms. As expected, Fig.4 indicates that the parametric faults cause small variations whereas the catastrophic faults cause hard changes in pulse response waveforms.

In order to determine the overall fault coverage, fault injection simulations of 54 cases were performed. One fault was injected into each component of the CUT per one simulation, while other components were kept at fault-free condition. Fig. 5 shows the Venn diagram of the number of detected faults in  $W_1$  to  $W_5$ . It can be seen

from Fig.5 that all 54 faults can be detected, indicating that the use of a narrow width pulse as an input test stimulus is effective. In addition, all 54 faults can potentially be detected in  $W_3$  and  $W_5$  while other three windows could not detect some faults. Therefore, this fault detection indicates that the use of  $W_3$  and  $W_5$  effectively yields complete fault detection, resulting in a simple fault detection circuit designs.



**Fig.6:** Graphical representation of the proposed impulse response-based fault detection technique.



**Fig.7:** Block diagram of the pulse-response based BIST system architecture.

#### 4. PROPOSED PULSE RESPONSE-BASED BIST TECHNIQUE

As a result of the preliminary investigation of fault impacts on pulse response characteristics described in (2), (3) and (4) and demonstrated in Figs. 4 and 5, this work proposes a pulse response-based BIST technique. The technique employs only two samples of pulse response waveforms for fault detection by means of voltage comparison in allowable tolerances. Fig.6 illustrates the graphical representation of the technique proposed, including the pulse response waveform of a fault-free CUT ( $RP_1$ ), and two examples of pulse response waveforms of a faulty CUT ( $RP_2$  and  $RP_3$ ). As illustrated in Fig.6, changes in  $RP_1$  can be investigated through the deviations of the maximum point at time  $t_1$  and the discharging period at time  $t_2$ . Correspondingly, two voltage samples  $V_1$  and  $V_2$  are obtained from  $RP_1$  at two sampling points  $P_1$  and  $P_2$ . The voltage  $V_1$  is measured at the maximum point  $P_1$  with the height of  $h$ . The voltage  $V_2$  is measured on the discharging period at the point  $P_2$ , which is set at  $h/4$ . It can be seen in Fig.6 that small changes in response shapes of  $RP_2$

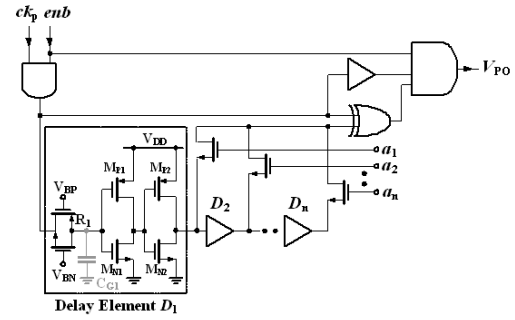
and  $RP_3$  cause large vertical deviations in voltage  $V_1$  and  $V_2$  at the points P1 and P2, respectively. Monitoring at time  $t_1$  and  $t_2$  reveals significant deviations in voltage values and the widow criteria are therefore utilized for fault discriminations.

This proposed technique can detect both parametric and catastrophic faults. In the case of parametric faults, parameter variations of capacitors, resistors, and transistors may affect both charging and discharging behaviors of pulse response waveforms as illustrated in Fig.6. Therefore, the parametric fault detection procedure depends upon the allowable tolerance bands of the voltage  $V_1$  and  $V_2$ . In the case of catastrophic faults, circuit operation failures cause tremendous changes in the peak value and the discharging period, resulting in significant changes in the voltage  $V_1$  and  $V_2$ . Therefore, catastrophic fault detection can be achieved easily.

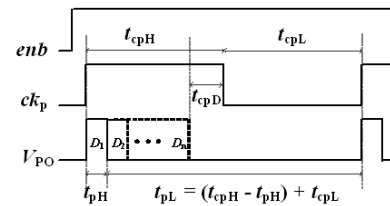
## 5. PROPOSED PULSE RESPONSE-BASED BIST SYSTEM AND CIRCUIT REALIZATIONS

The BIST system has been designed corresponding the proposed pulse response-based BIST technique described in Fig.6. Based on the general testing scheme in Fig.1, this BIST system is implemented entirely on-chip, including all the blocks A, B, and C. It is assumed that the digital portion in mixed-signal system can provide a sufficient number of system memories. Unlike other techniques in which software with specific algorithms or A/D converters are exploited, the circuit realization of this BIST system focuses on simple digital and analog techniques in order to reduce circuit complexity and area overhead. In addition, circuits with programmable features are employed in order to provide the versatility in applying to various types of analog CUTs.

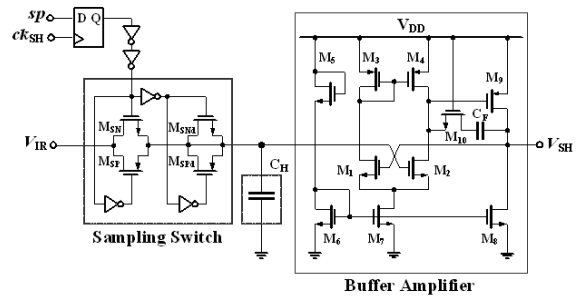
Fig.7 shows the block diagram of the pulse response-based BIST system. As shown in Fig.7, this BIST system comprises four major components, i.e. a pulse generator, a sample-and-hold (S/H) circuit, a window comparator, and control circuitry. First, the impulse generator provides a pulse stimulus  $V_{PO}$  for stimulating the CUT, and uses the clock  $ck_p$  as an input. This pulse generator is controlled by the signals  $enb$  and  $a_1 - a_n$ . Second, the S/H circuit samples the voltage values at two specific points of the output response  $V_{IR}$  and holds as  $V_{SH}$  for the subsequent fault detection circuit. The sampling operation is controlled by the clock  $ck_{SH}$  and the signal  $sp$ . Third, the window comparator compares the two points through tolerance bands determined by the threshold voltages  $V_{mn}$  and  $V_{mx}$ , and provides the pass/fail output  $V_{PF}$ . Last, control circuitry provides clock and control data for controlling BIST operations.



**Fig.8:** Circuit diagram of the programmable pulse signal generator.



**Fig.9:** Timing waveforms of pulse generation operations.



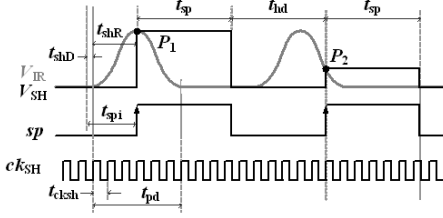
**Fig.10:** Circuit configuration of the S/H circuit.

### 5.1 Programmable Pulse Signal Generator

Generally, a practical pulse input test stimulus for BIST is a narrow-width rectangular pulse in order that the stimulated CUT can provide appropriate pulse response characteristics. Fig.8 shows the circuit diagram of the programmable pulse signal generator. As shown in Fig.8, the design is based on the propagation of a reference clock through a delay line and the phase comparison at the rising edge of low-to-high state transition between the input clock and the associated delay stages. Two input signals are the reference clock  $ck_p$  with a duty cycle of 0.5 and the enable signal  $enb$  that controls pulse generation operation within two periods of  $ck_p$ . A cascade connection of  $n$  identical delay elements  $D_1$  to  $D_n$  constitutes an  $n$ -stage delay line. Each of these delay stages delays the  $ck_p$  with constant delay time  $t_{pH}$ .

Since a delay element based on a threshold level of inverters or logic gates provides small delay time in

the range of picosecond, the implementation of this pulse generator therefore utilizes a variable resistor-based delay element. As particularly demonstrated at  $D_1$ , this delay element comprises two inverters and a variable complementary switch  $R_1$ , which is biased in linear



**Fig.11:** Timing waveforms of the sampling operations.

region and connected at the input of each delay element. The resistor  $R_1$  forms an inherent low-pass filter with the intrinsic gate capacitances  $C_{G1}$ , offering sufficient delay time for generating pulse widths in microsecond. The inclusion of  $R_1$  enables the fine adjustment of pulse widths through the setting of the bias voltages  $V_{BN}$  and  $V_{BP}$ . In addition, the coarse adjustment of pulse widths can be achieved by incrementing the number of delay stage through switches  $a_1$  to  $a_n$ . The delay time of the pulse output  $V_{PO}$  selected at the  $i^{th}$  stage is  $t_{pHi} = it_{pH}$  where  $i = 1, 2, 3 \dots n$ . The phase comparison is made by XOR gate, and the output  $V_{PO}$  obtained from the rising edge of the state transition is provided at the NAND gate.

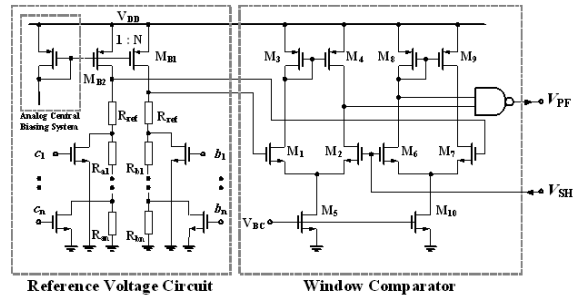
Fig.9 shows timing waveforms of pulse generation operations. As shown in Fig.9, high time  $t_{cpH}$  of the clock  $ck_p$  can be determined by the summation of the delay time  $t_{pHn}$  obtained from the  $n^{th}$  stage and the extra time  $t_{cpD}$  that provides sufficient time for pulse response propagation, i.e.  $t_{cpH} = t_{pHn} + t_{cpD} = nt_{pH} + t_{cpD}$ . Therefore, the frequency of the clock  $ck_p$  is equal to  $f_{ckp} = 1/(2t_{cpH}) = 1/(2(nt_{pH} + t_{cpD}))$ . This pulse generator is programmable through course and fine adjustments using simple delay elements with low area overhead, and a low frequency clock for generating high-frequency pulses.

## 5.2 Sample-and-Hold Circuit

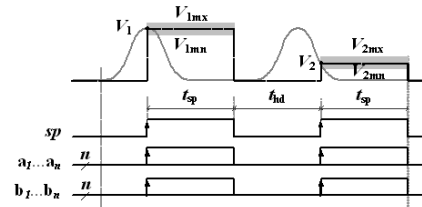
The S/H circuit was designed based a simple unity-gain sampler with error reduction. Fig.10 shows the circuit configuration of the S/H circuit, including three components, i.e. the sampling switch, the holding capacitor and the buffer amplifier. First, the sampling switch consists of the main switch ( $M_{SN}$  and  $M_{SP}$ ) and the dummy switch ( $M_{SNd}$  and  $M_{SPd}$ ). The complementary switch was realized in order to reduce on-resistance over the entire input range for high-speed sampling process with low DC offset. The dummy switch was employed for reducing clock

feedthrough errors. Second, the capacitor  $C_H$  is an available on-chip linear capacitor. The optimized size of  $C_H$  is in the range of 0.3pF to 0.7pF, providing a reasonable tradeoff among sampling speed, sampling accuracy and area overhead. Last, the buffer amplifier determines the sampling speed and the settling time stability of the sampled voltages. Therefore, the high bandwidth two-stage operational amplifier, consisting of transistors  $M_1$  to  $M_9$  with phase compensation using  $C_F$  and  $M_{10}$ , was realized.

Fig.11 shows the timing waveforms of the sampling operations. As shown in Fig.11, the input and output waveforms are the pulse response  $V_{IR}$  and the sampled-and-held signal  $V_{SH}$ , respectively. Sampling operations



**Fig.12:** Circuit configuration of a comparator.



**Fig.13:** Timing waveforms of the comparison operations.

are controlled by the clock  $ck_{SH}$  and the sampling signal  $sp$ . The clock period  $t_{cksh}$  of  $ck_{SH}$  can be determined by dividing time duration of one pulse response into six partitions. The signal  $sp$ , which is stored as a fault-free control bits in system memory, determines the sampling points  $P_1$  and  $P_2$  for each specific CUT. The initial delay time  $t_{spi}$  of  $sp$  is the summation of the propagation offset and the rising time to the peak of the first pulse response, i.e.  $t_{spi} = t_{shD} + t_{shR}$ . The sampling phase  $t_{sp}$  and the hold phase  $t_{hd}$  are equal to a half of time difference between the points  $P_1$  and  $P_2$ .

## 5.3 Programmable Window Comparator

The voltage comparator was designed based on a window criterion in which maximum and minimum threshold levels are set through tolerance bands.

Fig.12 shows the circuit configuration of the programmable window comparator, consisting of a main window comparator and a programmable voltage reference circuit. The window comparator comprises two differential amplifiers, consisting of transistors  $M_1$  to  $M_{10}$ , and a NAND gate. Unlike a logic-based comparator in which voltage thresholds are fixed and dependent on technology, this comparator provides an adjustable voltage threshold through the switching of reference voltages, and low vulnerability to process variations. Nonetheless, reference voltages are needed. As depicted in Fig.12, the reference voltages can be obtained from the analog central biasing system in mixed-signal systems. Two transistors  $M_{B1}$  and  $M_{B2}$  mirror the DC currents from the central biasing system, which is subsequently conveyed through a cascade connection of  $R_{ref}$  and the respective chains of resistors. Upon setting suitable resistor values, the required values of voltage references can be obtained and controlled through two sets of controlling switches.

Fig. 13 shows the timing waveforms of comparison operations. Through the exploit of the same clock  $ck_{SH}$  as

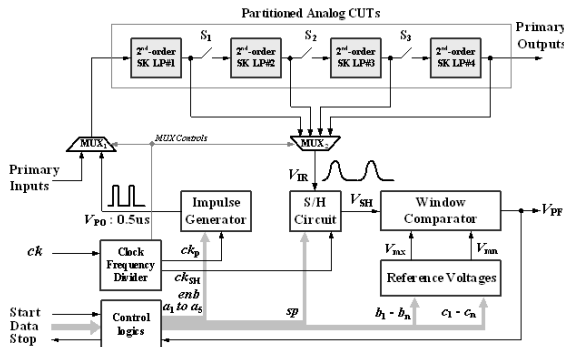


Fig.14: Block diagram of the BIST design example.

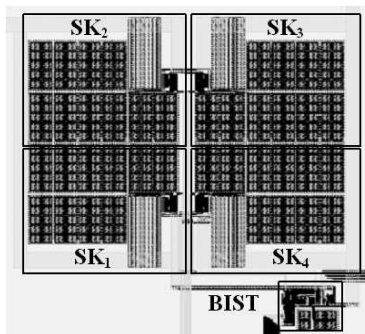


Fig.15: Layout design of the BIST system.

in the S/H circuit, two sets of control signals ( $b_1$  to  $b_n$ ) and ( $c_1$  to  $c_n$ ) are applied for switching the resistors, providing  $V_{mx}$  and  $V_{mn}$  for comparisons. This comparison process is performed during sampling mode of the S/H signals. During the hold mode,

all switches are turned off and therefore the high reference voltages are equal at the two inputs of NAND gate, yielding low signal at the output. The test result  $V_{PF}$  is two bit signals and reported as High when faults are detected.

## 6. SIMULATION RESULTS

The proposed BIST system was laid out using 0.18- $\mu\text{m}$  standard CMOS technology in Cadence environments and post-layout simulations were performed using Hspice. Fig.14 shows the block diagram of the BIST design example. As shown in Fig.14, four example of CUTs, including 2<sup>nd</sup>-order, 4<sup>th</sup>-order, 6<sup>th</sup>-order and 8<sup>th</sup>-order Sallen Key low-pass filters, were employed as a means of different filter orders. Fig.15 shows the corresponding layout designs where the areas of CUT and BIST are 355 $\mu\text{m} \times 338\mu\text{m}$  and 63 $\mu\text{m} \times 58\mu\text{m}$ , respectively.

Firstly, performance degradation was investigated in order to evaluate the impacts of the inclusion of BIST system. Fig. 16 shows the frequency responses of the original CUT, which is a 2<sup>nd</sup>-order filter, and the CUT with BIST system. The DC gain and the cutoff frequency were measured at 0dB and 504.98 kHz, respectively. It can be seen from Fig. 16 that the inclusion of BIST system does not degrade the unity-gain bandwidth of the original filter. As the BIST system was removed from the CUT during normal operations by associated switches, no

Table 1: Summary of the measured delay time at different pairs of  $V_{BP}$  and  $V_{BN}$ .

Measured Delay Time $t_{pH}$ (ns)		$V_{BN}$			
		0.3V	0.4V	0.5V	0.6V
$V_{BP}$	1.4V	0.017	0.016	0.015	0.013
	1.5V	0.25	0.19	0.18	0.18
	1.6V	3.82	3.54	3.16	2.76
	1.7V	10.05	10.05	10.05	10.05

Table 2: Measured nominal voltages with tolerance bands at  $\pm 5\%$  deviation, and timing parameters.

CUTs	Parameters of Two-Point Sampling Voltages and Timing								
	(a) Voltage (V)						(b) Time ( $\mu\text{s}$ )		
	$V_1$			$V_2$			$t_{qD}$	$t_{S1}$	$t_{S2}$
	$V_{1mn}$	$V_{1nor}$	$V_{1mx}$	$V_{2mn}$	$V_{2nor}$	$V_{2mx}$			
2 <sup>nd</sup> -Order	1.36	1.39	1.43	0.43	0.44	0.49	0.1	0.6	1.9
4 <sup>th</sup> -Order	1.01	1.08	1.14	0.37	0.39	0.43	0.4	1.3	1.8
6 <sup>th</sup> -Order	0.95	1.01	1.06	0.40	0.42	0.47	0.7	1.8	3.4
8 <sup>th</sup> -Order	0.95	1.00	1.42	0.42	0.44	0.48	1.0	2.2	3.8

significant loading effects on the CUT was evident on the cutoff frequency. At higher frequency region of more than 1MHz, parasitic capacitances of these switches cause some deviations at a very low gain region of less than -60 dB, which exceeds the filter specification. Therefore, the specification of the original CUT was satisfied with no performance degradation caused by the inclusion of the BIST system.



**Table 3:** Summary of performances of the S/H circuit and the window comparator.

Performances		Values	Units
(a) S/H Circuit	Offset Error	<0.0065	V
	Settling Time	0.012	ns
	Maximum $V_{mx}$	1.46	V
(b) Window Comparator	Minimum $V_{mn}$	0.12	V
	Narrowest Region	0.80-0.89	V
	Offset Error	<0.12	%

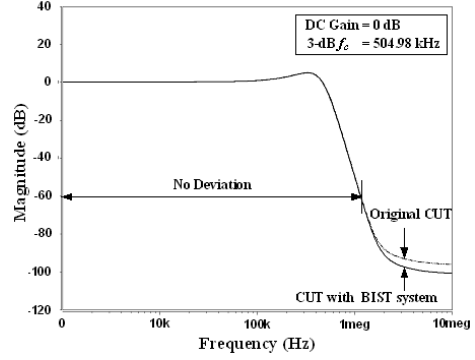
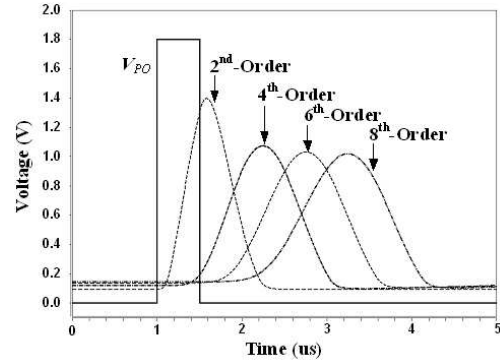
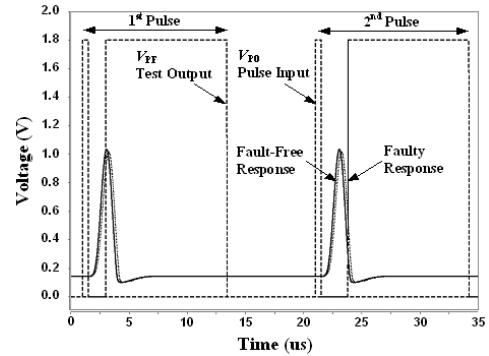
**Table 4:** The total number of injected faults and resulting fault coverage.

Lists of Injected Faults	No. of Faults	Detected Faults	Undetected Faults	Fault Coverage
(a) Resistor Shorts	32	32	0	100%
(b) Capacitor Opens	32	32	0	100%
(c) Transistor Shorts	20	20	0	100%
(d) Transistor Opens	20	20	0	100%
(e) $\pm 20\%$ Variation of C	32	30	2	93.75%
(f) $\pm 20\%$ Variation of R	32	28	4	87.5%

Secondly, the optimum pulse width was investigated through the mapping of  $V_{BP}$  and  $V_{BN}$  pairs. With reference to Fig.9, Table 1 summarizes the measured values of the delay time  $t_{pH}$  where  $V_{BP}$  was set as a dominant voltage in the range of 1.4V to 1.7V and  $V_{BN}$  were investigated in the range of 0.3V to 0.6V. It is seen from Table 1 that the setting of  $V_{BP}$  at 1.4V and 1.5V provides relatively small delay time of less than  $0.25\mu s$ . The increase of  $V_{BP}$  to 1.6V yields a longer  $t_{pH}$  in the range of  $2.76\mu s$  to  $3.82\mu s$  prior to the maximum  $t_{pH}$  of  $10.05\mu s$  at  $V_{BP}$  of 1.7V. Based on Table 1, the delay time  $t_{pH}$  of each delay stage was chosen at  $0.25\mu s$  by setting  $V_{BP}$  and  $V_{BN}$  to 1.5V and 0.3V, respectively. Two delay stages were activated, i.e.  $n=2$ , by setting  $a_2$  to high, resulting in the pulse width  $V_{PO} = 0.5\mu s$ . The frequency of the clock  $c_{kp}$  was set to 40kHz. Fig.17 shows the pulse response waveforms of the four CUTs when the  $0.5\mu s$  pulse stimulus was applied. It is seen from Fig.17 that the CUTs provide appropriate pulse response waveforms. The 2<sup>nd</sup>-order filter provides high peak values with narrow width while other orders have wider widths with approximately the same peak values.

Thirdly, Table 2 summarizes the measured nominal values of voltages  $V_1$  and  $V_2$  with tolerance bands of  $\pm 5\%$  deviation, i.e.  $V_{mn}$  and  $V_{mx}$ , and timing parameters. As summarized in Table 2 (a), the values of reference voltages can be set corresponding to filter orders. The reference voltages were set and selectable in the range of 0.3V to 1.5V. As also summarized in Table 2 (b), the frequency of the clock  $ck_{SH}$  was determined by parameters  $t_{shD}$ ,  $t_{P1}$  and  $t_{P2}$  where  $t_{P1}$  and  $t_{P2}$  are sampling time at points  $P_1$  and  $P_2$ , respectively. For instance, the clock period of  $0.1\mu s$  is sufficient for sampling the two points for the 2<sup>nd</sup>-order filter, and therefore the clock  $ck_{SH}$  of 2MHz was used.

Fourthly, the accuracy of the S/H circuit and the win-

**Fig.16:** Frequency responses of the original CUT and the CUT with the inclusion of BIST system.**Fig.17:** Pulse response waveforms of the four CUTs when the  $0.5\mu s$  pulse input signal was applied.**Fig.18:** Demonstrating waveforms of the testing for the potential open at the capacitor.

dow comparator was also investigated in Table 3. For the S/H circuit, the offset error is a major parameter that sets the testing accuracy. As summarized in Table 3(a) that the offset error is very low of less than  $0.0065V$  and the settling time is relative fast at  $0.012ns$ .

For the window comparator, the width of a window criterion, which sets the tolerance band, can be adjusted through the reference voltages. As also summarized in Table 3(b), the maximum allowable volt-

**Table 5:** Comparisons of this work and other three related BIST techniques,  $\times$  = not reported.

Performances	This Work	Related BIST Techniques		
		[12]	[13]	[15]
Technology	0.18- $\mu$ m CMOS	$\times$	$\times$	Discrete Components
Types of Results	Simulation	Simulation	Simulation	Experiment
Demonstrating CUTs	Sallen-Key Filter	Sallen-Key Filter	$\times$	Sallen-Key Filter
Number of Required Pulse Inputs	Two Pulses	Random-Width Pulse Trains	Pseudo-Random Pulse Inputs	Multiple Pulse Inputs
Pulse Generation Methods	Programmable Pulse Generator	Digital LFSR	$\times$	Microcontroller
Fault Detection Methods	Sampling and Window Criteria	Signature Compaction	Cross-Correlation Analysis	Algorithms in Microcontroller
Catastrophic Fault Coverage	100%	8 faults@5% Tolerances	$\times$	$\times$
Parametric Fault Coverage	Capacitor = 93.75% Resistor = 87.5%	$\times$	$\times$	$\times$

age  $V_{mx}$  and  $V_{mn}$  were found in the range of 0.12V and 1.46V. The narrowest range of effective window criterion was found in the region of 0.8V to 0.89V, respectively. The designed window comparator exhibits a low offset error of less than 0.12% of the nominal values.

Finally, realistic faults were injected randomly using a local layout realistic fault mapping ( $L^2$ RFM) technique [21]. Parametric faults were investigated through  $\pm 20\%$  variations of capacitors and resistors. Catastrophic faults were injected by means of shorts and opens at capacitors, resistors, and MOS transistors. Note that catastrophic faults in MOS transistors were considered from critical layout areas. Table 4 summarizes the total number of injected faults and fault coverage of the 8<sup>th</sup>-order Sallen-Key low-pass filter. As summarized in Table 4 (a) to (d), all shorts and opens were detected effectively, yielding fault coverage of 100%. All of these shorts and opens were detected because the two voltage samples were captured from the tremendously distorted pulse response waveforms, which are considerably out of the tolerance bands.

As summarized in Table 4 (e) to (f), fault coverage of capacitor and resistor variations are relatively high at 93.75% and 87.5%, respectively. However, some faults could not be detected because changes in these component values were small deviations on the peak values and the discharging periods. Therefore, the two voltage samples are included in the acceptable tolerance bands. The CUTs that have these types of undetected faults can be considered as non-defective when high yieldloss is preferred in the pre-screening process. Fig.18 demonstrates the waveforms of fault detection procedures when the potential open was injected at the capacitor  $C_2$  of the first 2<sup>nd</sup>-order section of the 8<sup>th</sup>-order filter. It is demonstrated in Fig.18 that the open of capacitor results in a shift of impulse response and therefore the vertical detection at two points provides the high state of output test  $V_{PF}$ , indicating a faulty CUT.

## 7. COMPARISON TO OTHER TECHNIQUES

Table 5 compares the proposed BIST technique to those of existing BIST techniques. In an attempt to enable fair comparison, three particular references that previously proposed BIST techniques based on pulse stimulation and measurement are considered. With reference to Table 5, comparisons are made based on preferable requirements for BIST systems, including implementation cost, testing time, and fault coverage. First, this work offers low implementation cost through the use of the programmable pulse generator. Neither digital LFSR, which is commonly used in digital testing, nor microcontroller is required. Furthermore, the proposed BIST technique enables the use of a simple S/H with window comparators for fault detection process while other techniques necessitate complex devices such as A/D converter, microcontroller, and DSP with specific algorithms for fault signature compaction or cross-correlation analysis.

Second, this work uses low testing time within a two-pulse duration, and the fault detection procedure performs instantaneously during sample and hold operations, generating the pass/fail output in digital forms. Other techniques employ a random width pulse sequence or a multiple pulse train as input stimuli. Therefore, the fault detection procedures require time for processing long pulse sequence responses in digital domain through the use of digital counters or microcontroller. Last, the fault coverage of this work is relatively high as demonstrated for the testing of Sallen-Key low-pass filter. Noted that fault coverage depends on test set-up environments such as CUT specifications and tolerance conditions. References [3] and [4] show examples of fault detection performances while complete fault coverage were not reported.

## 8. CONCLUSIONS

The pulse response-based BIST technique and implementation for the testing of analog integrated circuits in mixed-signal systems have been proposed.

The proposed BIST technique employs two pulses as input stimuli generated by the programmable pulse generator, and monitors two voltage samples on a pulse response waveform for fault detection using the S/H circuit with window comparators. Advantages over other exiting works include low testing time and low implementation cost with relatively high fault coverage. This BIST system is compatible to mixed-signal systems since the test system employs digital clocks and signals as input resources and the test output is provided in digital forms. Limitations of this BIST system are the limited applications for the testing of LTI circuits and the test accuracy may sensitive to analog window comparators. The future planed work include the design for the testing of analog-to-digital converters and the improvement of comparators for high-accuracy fault detection process. In conclusions, the proposed pulse response based-BIST technique has offered a potential alternative to low-cost and high-speed BIST system for the pre-screening test process for defective analog integrated circuits in mixed-signal systems.

## 9. ACKNOWLEDGEMENT

This work was partially supported by a grant of "High-Tech Research Center Development Program". The authors are grateful to Kochi University of Technology (KUT) for a Special Ph.D. Scholarship Program.

## References

- [1] K. Arabi, B. Kaminska, "Design and realization of a built-in current sensor for IDDQ testing and power dissipation measurement," *J. of Analog Integrated Circuits*, Vol.23, No.2, pp. 117-126, 2000.
- [2] J. Font, J. Ginard, R. Picos, E. Isern, J. Segura, M. Roca, E. Garcia, "A BICS for CMOS opamps by monitoring the supply current peak," *J. of Electronic Testing*, Vol.19, No.5, pp. 597-603, 2003.
- [3] J.B. Kim, S.H. Hong, "A CMOS built-in current sensor for IDDQ testing," *IEICE Trans. Electron.*, Vol.E89-C, No.6, pp. 868-870, 2006.
- [4] S. Bhunia, A. Raychowdhury, K. Roy, "Defect oriented testing of analog circuits using wavelet analysis of dynamic supply current," *J. of Electronic Testing*, Vol.21, No.2, pp. 147-159, 2003.
- [5] C. Dufaza, H. Ihs, "A BIST-DFT technique for DC test of analog modules," *J. of Electronic Testing*, Vol.9, No.1-2, pp. 117-133, 1996.
- [6] G. O. Ducoudray-Acevedo, J. Ramirez-Angulo, "Innovative built-in self test schemes for on-chip diagnosis, compliant with IEEE 1149.4 mixed-signal test bus standard," *J. of Electronic Testing*, Vol.9, No.1, pp. 20-27, 2003.
- [7] R. Rashidzadeh, M. Ahmadi, W.C. Miller, "On-chip measurement of waveforms in mixed-signal circuits using a segmented sub-sampling technique," *J. of Analog Integrated Circuit Signal Processing*, Vol.50, No.2, pp. 105 -113, 2007.
- [8] C.E. Stroud, "Designer's guide to built-in self-test," *Kluwer Academic Publishers*, 2002.
- [9] M.G. Mendez-Rivera, A. Valdes-Garcia, J. Silva-Martinez, E. Sanchez-Sinencio, "An on-chip spectrum analyzer for analog built-in testing," *J. of Electronic Testing*, Vol.21, No.3, pp. 206-219, 2005.
- [10] L. Cassol, O. Betat, L. Carro, M. Lubaszewski, "The  $\Sigma\Delta$ -BIST method applied to analog filters," *J. of Electronic Testing*, Vol.19, No.1, pp. 13-20, 2003.
- [11] S. R. Das, J. Zakizadeh, S. Biswas, M. H. As-saf, A. R. Nayak, E. M. Petriu, W. B. Jone, M. Sahinoglu, "Testing analog and mixed-signal circuits with built-in hardware-A new approach," *IEEE Trans. on Instrumentation and Measurement*, Vol.56, No.3, pp. 840 - 855, 2007.
- [12] P.N. Variyam, A. Chatterjee, N. Nagi, "Low-cost and efficient digital-compatible BIST for analog circuits using pulse response sampling," *Proc. of IEEE VLSI Test Symposium*, pp. 261-266, 1997.
- [13] C. Marzocca, F. Corsi, "Mixed-signal circuit classification in a pseudo-random testing scheme," *J. of Electronic Testing*, Vol.18, No.3, pp. 333-342, 2002.
- [14] A. Singh, C. Patel, and J. Plusquellic, "On-chip impulse response generation for analog and mixed-signal testing," *Proc. of Int. Test Conference*, pp. 262- 270, 2004.
- [15] Z. Czaja, "A fault diagnosis method of analog electronic circuits for mixed-signal systems controlled by microcontrollers," *Proc. of IEEE Instrumentation and Measurement Technology*, pp. 1211-1216, 2006.
- [16] B. Razavi, "A 2.4-GHz CMOS receiver for IEEE 802.11 wireless LANs," *IEEE J. of Solid-State Circuits*, Vol.34,
- [17] D. Yee, C. Doan, D. Sobel, B. Limketkai, S. Alalusi, R. Brodersen, "A 2-GHz low-power single-chip CMOS receiver for WCDMA applications," *Proc. of int. Solid-State Circuits Conference*, pp. 57 - 60, 2000.
- [18] V. Stopjakova, P. Malosek, D. Micusik, M. Matej, M. Margala, "Classification of defective analog integrated circuits using artificial neural networks," *J. of Electronic Testing*, Vol. 20, No.1, pp. 25-37, 2004.
- [19] S.J. Chang, C.L. Lee, J.E. Chen, "Structural fault based specification reduction for testing analog circuits," *J. of Electronic Testing*, Vol.18, No.6, pp. 571 - 581, 2002.
- [20] M. Negreiros , L. Carro, A. Susin, "A statistical sampler for a new on-line analog test method," *J.*

of *Electronic Testing*, Vol.19, No.5, pp. 585-595, 2003.

- [21] M.J. Ohletz, "Realistic faults mapping scheme for the fault simulation of integrated analogue CMOS circuits," *Proc. of Int. Test Conference*, pp. 776 - 785, 1996.



**Wimol San-Um** received B.E. Degree in Electrical Engineering and M.S. Degree in Telecommunications in 2003 and 2006, respectively, from Sirindhorn International Institute of Technology, Thammasat University, Thailand. In 2007, he was a research student at University of Applied Science Ravensburg-Weingarten, Germany. Since 2008, he has been working towards his Ph.D. at the Department of Electronic and Photonic System Engineering, Kochi University of Technology, Japan. His areas of research interests are analog circuit designs, involving chaotic oscillators and switched-current circuits, and on-chip testing design, involving DFT and BIST techniques.



**Masayoshi Tachibana** was born in Tochigi, Japan. He received the B.E., M.E., and D.Eng. degrees in electrical engineering from Waseda University in 1981, 1983, 1986 respectively. In 1986, he joined Toshiba Corporation, Tokyo, Japan. From 1989 to 1991, he was a visiting scholar at the University of California at Berkeley. In 2000, he left Toshiba Corporation, joined Kochi University of Technology, and now is a professor at the

Department of Electronics and Photonic System Engineering. His areas of research interest are computer algorithm for combinational problem, and VLSI systems design. Dr. Tachibana is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Information Processing Society of Japan, and IEEE.