An Intelligent CMOS Image Sensor with negative feedback resetting

Masayuki Ikebe[1] and **Junichi Motohisa**[2], Non-members

ABSTRACT

We investigated a negative feedback method for adding functionality to a CMOS image sensor. Our sensor effectively uses the method to set any intermediate voltage into a photodiode capacitance while a pixel circuit is in motion. The negative feedback reset functions as a noise cancellation technique and can obtain intermediate image data during charge accumulation. As an above application, dynamic range compression is achieved by individually selecting pixels and by setting an intermediate voltage or performing quasi-holding with respect to each pixel. Additionaly, we achieved duplicated interlaced processing and were able to output frame-difference images without frame buffers. The experimental results obtained with a chip fabricated using a 0.25-μm CMOS process demonstrate that Dynamic range compression and intra-frame motion detection are effective applications of negative feedback resetting.

Keywords: CMOS Image Sensor, Negative Feedback, Dynamic Range Compression, Motion Detection

1. INTRODUCTION

Digital cameras are widely used and almost all cell phones have a camera function. The heart of a digital camera is either a charge-coupled device (CCDs) or CMOS image sensor, both of which are being aggressively developed for a wide range of applications including cell phones, monitors, and on-vehicle equipment. Image sensors of the CMOS type are especially good at integrating peripheral CMOS circuits and thereby enabling various types of image-processing functions to be included on the same chip, an extremely convenient feature. Although noise (both thermal noise and the fixed-pattern noise due to device variation) is a greater problem in CMOS image sensors than in CCDs, improvements in the manufacturing process and the use of noise-elimination techniques such as correlated double sampling (CDS) have reduced the noise levels of CMOS image sensors almost to those of CCDs.

Manuscript received on April 12, 2009 ; revised on April 4, 2010.

[1,2] The authors are with Graduate School of Information Science and Technology, Hokkaido University,Sapporo, Japan 060-0814, Tel: +81-11-706-7689, Fax: +81-11-706-7689, E-mail: ikebe@ist.hokudai.ac.jp and motohisa@ist.hokudai.ac.jp

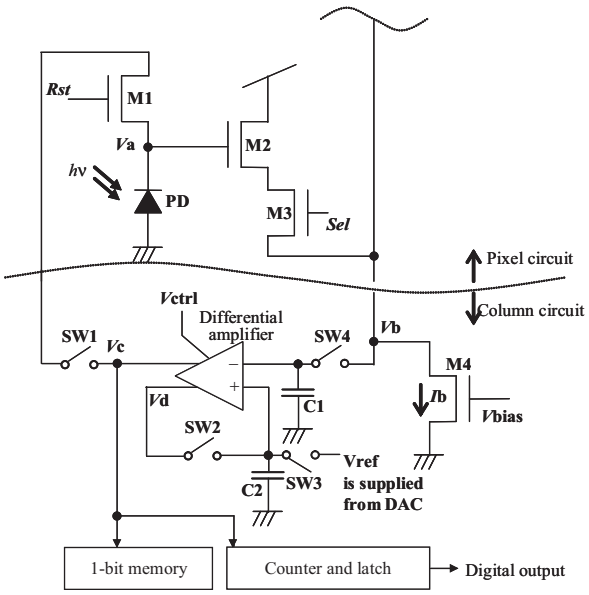
We recently proposed a negative-feedback reset as a noise cancellation technique and showed that it can obtain intermediate image data during the charge-accumulation process [1, 2]. The availability of intermediate image data makes it possible to read the change in luminosity during charge accumulation, and we expect this capability to be exploited in a variety of applications [3]. In this paper we show how a CMOS image sensor with functionality can be obtained by using a negative-feedback reset to modulate photodiode (PD) capacitance. The proposed technique enables a pixel circuit with a minimum configuration to be individually reset and realizes applications such as dynamic range compression and motion detection.

2. PIXEL CIRCUIT PERFORMING NEGATIVE-FEEDBACK RESET

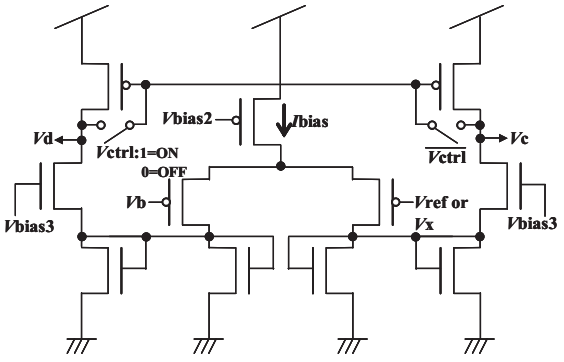
2.1 Configuration of proposed circuit

Figure 1(a) shows the configuration of the circuit we designed for performing negative-feedback reset at any voltage and quasi-holding of the pixel state. The format of the pixel portion of this circuit is that of a conventional three-transistor active pixel sensor (APS). A signal line is laid vertically from the upper electrode of nMOSFET M1, and the Va point of the gate electrode of nMOSFET M2 connects to the upper end of the photodiode (PD). The Rst label indicates the reset signal of the pixel circuit and Sel is the select signal. The Vb point is output of the pixel circuit. The Vb value is equivalent to $Vpix$ in subsection III.B. The common portion of this circuit for each column consists of a current source for the source follower, a differential amplifier, switches SW1-SW4 to change wiring connections, and a 1-bit state-holding memory. The voltage $Vref$ from DAC provides non-inverting input to the differential amplifier. It can be set to various values to perform the operations described in subsection II.B.

The circuit of the differential amplifier is shown in Fig. 1(b), where both the Vc and Vd outputs are the outputs of a single-end amplifier. The output to use is selected by $Vctrl$, which changes only the input electrode (+/-) and leaves the input connection unchanged.

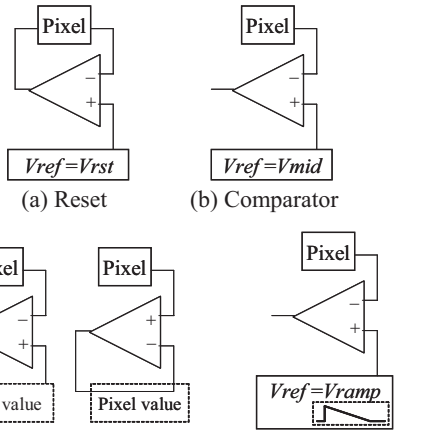


(a) Proposed circuit configuration



(b) Circuit configuration of differential amplifier

Fig.1: *Proposed configuration of image sensor*



(a) Reset (b) Comparator

(c, d) Signal save, refresh (e) Signal output "A/D"

Fig.2: *Wiring connection of each mode*

2.2 Operation of proposed circuit

The proposed circuit performs operations in the following five modes corresponding to specific wiring connections and control signals.

1. Reset mode
2. Comparator mode
3. Signal-save mode
4. Refresh mode
5. Signal-output mode

Figure 2 shows the wiring connections of operations. In mode 1 (Fig. 2(a)), at the beginning of the image pickup cycle, M1 is set to ON by the Rst signal so as to reset the PD. We specified the reset period as 1 μs. At the same time, M3 is set ON by the Sel signal to form a negative-feedback loop between the pixel circuit and the output amplifier. Here we denote the transconductance, threshold and threshold variation of M2 as β, Vth, and ΔVth; the current flowing through M4 as Ib; the gain of the differential amplifier as A; non-inverting input as $Vrst$; inverting input as Vb; and the gain of the source-follower due to M2 and M4 as $H = 0.8$ (constant value). The offset component $Dout$ on the negative- feedback loop can then be given by Eq. (1) and the transfer characteristic of the closed loop by Eq. (2). We see from Eq. (2) that A$\gg$1 in the state corresponding to the formation of a negative-feedback loop and that the potential of the output line is reset so that Eq. (2) is always satisfied. In other words, at any voltage the system performs a reset based on the value of $Vrst$.

$$Dout = -\left(Vth + \Delta Vth + \sqrt{\frac{Ib}{\beta}}\right) \tag{1}$$

$$Vb = Vrst\frac{AH}{1+AH} + Dout\frac{H}{1+AH} \tag{2}$$

In mode 2 (Fig. 2(b)) the differential amplifier operates as a comparator with respect to signal output Vb (with the result that differential-amplifier output is set to a logical 1 or 0). We specified the judgment period as 0.5 μs. In mode 3 (Fig. 2(c)) the differential amplifier acts as an elemental voltage follower whereby SW2 can be controlled to save the value of Vb in capacitor C2. We specified the save period as 0.5 μs. Since there are small parasitic elements in the save mode connection, convergence becomes quick. In mode 4(Fig. 2(d)) the completion of mode 3 results in a reset operation similar to mode 1 but based on the signal value saved in capacitor C2. We specified the reset period as 1 μs. Finally, in mode 5 (Fig. 2(e)) the system outputs a pulse-width modulation (PWM) signal. A circuit is configured as a comparator like the mode (2). The PWM signal according to the value of Vb can be obtained by comparing Vb with the RAMP signal $Vramp$. This mode is used for single-slope ADC. Since the single-slope ADC is 10-bit accuracy, 1024 clock cycles are required. Therefore, the ADC period is 20.48 μs at 50MHz clock.

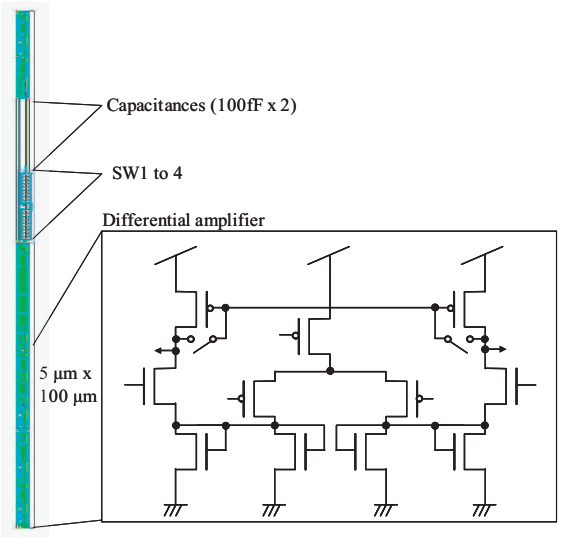


Fig.3: *Basic layout of trial circuit*

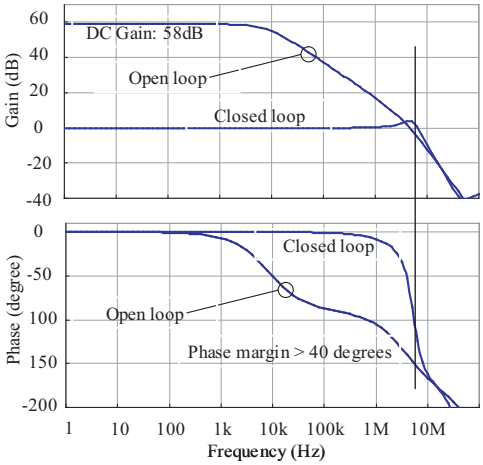


Fig.4: *Loop characteristics of designed circuit*

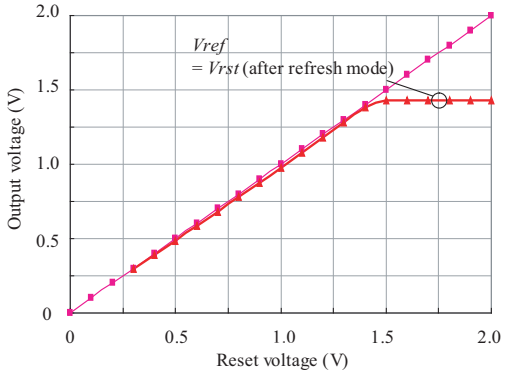


Fig.5: *Characteristics of refresh operation*

3. CIRCUIT DESIGN

3.1 Design considerations of basic circuit

The circuitry of differential amplifier, in Fig. 1(b) is important for stability of the reset operation. In using two-stage configurations for the amplifier, a large phase-compensation capacitance is need for stability. Therefore the slew rate becomes low and the settling time becomes slow. In this work a single-stage configuration was used and stability was obtained without phase-compensation capacitance. The gain of the amplifier was compensated with cascode connection of the output portion.

We specified reset within 1 μs in the signal range 1V, so a signal rising time under 0.25 μs was needed. In this case, a power bandwidth greater than 640 kHz was required in using the amplifier as a unity-gain buffer. Because the circuitry we used did not have phase-compensation capacitance, slew rate is defined by parasitic elements and the current of the output portion. However, a secondary pole is produced by a parasitic element and the delay of the settling time by dumping can be considered. Then because one of our top priorities was a DC gain of 60 dB, the output portion was designed for to provide a settling time $<$ 0.5 μs under the conditions of a slew rate $>$ 4 V/μs.

We adopted the differential amplifier as single-end use. Therefore possibility of a common-mode-noise problem was considered. Then, we suppressed noise generating of the digital part which was the key factor of a common mode noise as much as possible. The taken measures were as follows.

1. Two or more switching is not performed simultaneously within a column circuit. 2. The digital circuit stops during analog circuitry operation without digital data output. 3. Powerful guard ring is arranged in the boundary of a digital part and an analog part. 4. The digital output lines are protected with a shield. 5. Gray code is used to the counter circuit for single slope ADC. Since it is 1-bit change at a time, gray code can suppress the noise of the counter. 6. A low pass filter is put into a DAC output. The DAC may become noise sauce with the output change by bit change at the time of RAMP waveform generation. Therefore, we put valid LPF into the DAC output.

When we use the differential amplifier, although the kTC noise is not eliminated, the kTC noise in the band of the closed loop becomes a fraction of amplifier gain.

3.2 Layout design of basic circuit

We designed a trial version of a basic circuit using a 0.25-μm CMOS process. In the pixel circuit a negative-feedback bus from the readout circuit connects to a traditional three-transistor configuration. The pixel circuit including this negative-feedback bus was designed to be 5 μm square with a fill-factor ratio of 40%. Moreover, the circuits without photodiodes are shaded by metal and black polymer.

The column circuit was designed to have a width of 5 μm to facilitate connection with the pixel circuit

(assuming one circuit per column). Figure 3 shows the layout of the analog portion of the column circuit. The size of the differential amplifier was 5 μm × 100 μm. The values of capacitors C1 and C2 in Fig. 2(a) were both 100 fF.

3.3 Main circuit simulation

We did a simulation of a column circuit and a pixel circuit, and the loop characteristics of the column circuit and the pixel circuit are shown in Fig. 4. Parasitic capacitance and resistance, 1 pF and 400 Ω, were added to reset-line and readout-line. The circuit had an open-loop DC gain of 58 dB and a phase margin of 42 degrees. The closed-loop characteristics are shown in Fig. 4. We confirmed that the circuit operated as a unity gain buffer.

The amplifier does not change in the loop characteristic until the light current of the PD exceeds 50 nA. Although the gain decreases and the phase characteristic changes over 50 nA, the stability is satisfactory (phase margin =: 40 degrees). 50 nA is equivalent to about 3,000,000 lux in this process.

We examined the characteristics of refresh operation through simulation. Figure 5 shows readout values in signal-save mode (voltage follower) immediately after performing refresh mode. The light current of the pixel circuit was set to be 0 nA. The plots shown were obtained while varying $Vrst$ with $Vref = Vrst$. We confirmed that the circuit operated saving and rewriting the pixel value.

3.4 Controller Design

The architecture of the controller is that of a programmable sequencer (PS) that has eight instructions that consist of 12-bit words. The list of instructions is shown in Table I. The WAIT commands controls waiting time to next command operation. The LINE_CNT commands controls row selecting. The SW_OPA, SW_MISC, and SW_AR commands control switches. Using these commands, a certain switch is selected and on/off controlled at a cycle. The SET_LOOP and JMPL commands are used for repeat operations. The WREG command has double word, and set control value such as voltage code, voltage-offset code and delay-code to control register of DAC and ADC. When a command sequence for dynamic range compression is written to the 128-word instruction memory and is executed, the function is realized.

4. APPLICATIONS

4.1 Individual reset

Pixels can be reset individually by making use of the modes described in subsection II.B. Figure 6 shows the mechanism of individual resetting. First, using the comparator mode, the result of comparison is stored in the 1-bit state-holding memory. Next, using the signal-save mode, the current pixel value is saved to C2. Our system can selects the wire connection of column circuits according to the data stored in the 1-bit memory. If the stored data is "0", the connection for refresh mode is selected. If the stored data is "1", the connection for reset mode is selected. The reset value is $Vref = Vmid$ supplied from DAC. At that time, if the negative feedback loop is formed by Rst and Sel turning on, the current pixel value is reset to the pixel circuit with refresh connection of column circuit and the $Vref$ (=$Vmid$ supplied by DAC) value is reset to the pixel circuit with the reset connection of the column circuit. In other words, Rst can be ON for all columns on a certain row k simultaneously and the pixel at coordinates (M, k) can be reset while the value of the pixel at (N, k) can be saved. The significance of this is that each pixel can be reset individually without having to increase the number of transistors in the standard three-transistor APS configuration in the pixel section of the circuit.

Table 1: *Instruction set of programmable sequencer*

Command name	Function	Number of words
WAIT	Waiting time	1
LINE_CNT	Line selection	1
SW_OPA	Amplifier switching	1
SW_MISC	Pixel-circuit switching	1
SW_AR	Test-circuit switching	1
SET_LOOP	Loop operation	1
JMPL	Loop operation	1
WREG	DAC/ADC control	2

1 word consists of 3 bit header and 9 bit body.
2 words consist of 3 bit header and 21 bit body.

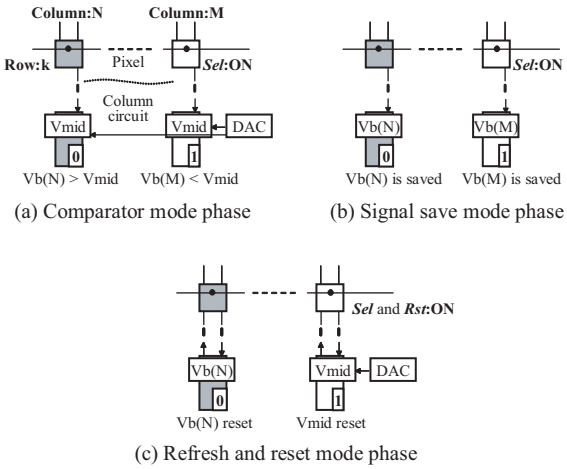
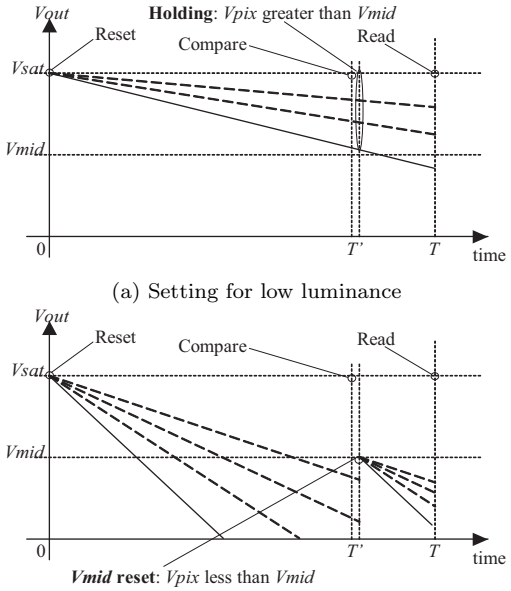


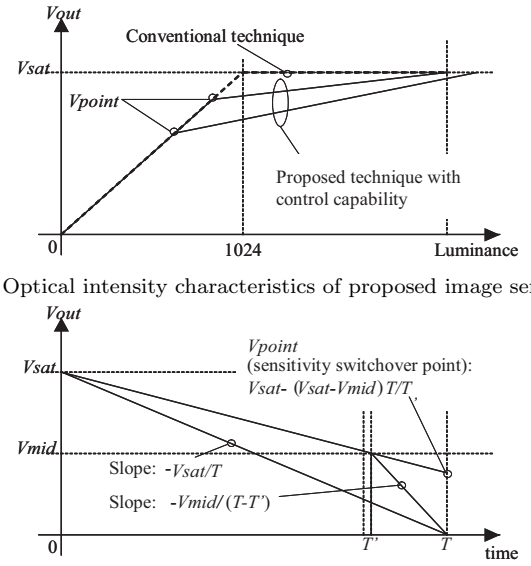
Fig.6: *Individual resetting mechanism*



(a) Setting for low luminance

(b) Setting for high luminance

Fig.7: *Timing diagrams and characteristics of proposed dynamic range compression*



(a) Optical intensity characteristics of proposed image sensor

(b) Output characteristics of proposed image sensor

Fig.8: *Output form of proposed image sensor*

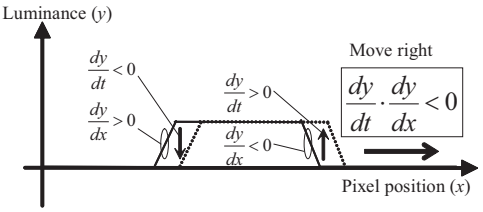


Fig.9: *Motion detection mechanism*

4.2 PD-capacitance control and expanding of dynamic range

In a CMOS image sensor, a variety of techniques can be used for wide dynamic range image capturing [4–6]. In this paper we show how achieve a wide dynamic range by using negative-feedback resets to modulate the PD capacitance of each pixel individually. Figures 7(a) and 7(b) shows timing diagrams for two types of settings. It is assumed here that each pixel circuit performs output at fixed intervals corresponding to frame period T. The pixel output range is denoted $Vsat$.

The system first performs an initial reset on the pixel circuit. This reset cancels out circuit dispersion error by negative feedback. Then at time T' the system performs an intermediate image readout and detects whether the pixel output $Vpix$ is greater than or less than $Vmid$. When luminance is higher, light current is larger and $Vpix$ falls faster. The $Vpix$ value may therefore be saturated under very high luminance. If $Vpix$ is greater than $Vmid$ (luminance is low), the system does nothing (Fig. 7(a)). If $Vpix$ is less than $Vmid$ (luminance is high), the system supplies a current resetting $Vpix$ to $Vmid$ (Fig. 7(b)). In both case the exposure and charge accumulation continue until time T. In the high luminance case the range of output $Vpix$ values at time T is compressed because of the reset at exposure time $T-T'$. Optical-intensity characteristics can be changed by the adjusting the time T' and the value of $Vmid$, but the output range $Vsat$ does not change.

Figure 8(a) shows output characteristics versus optical intensity. The system exhibits usual exposure characteristics up to a certain value of optical intensity, at which point the output characteristics change abruptly. At higher optical intensities the sensitivity is reduced and even strong light will result in an unsaturated output value. This means that a single pixel can have both a high-sensitivity state and a low-sensitivity state. Furthermore, as the values of T', $Vmid$ and $Vsat$ described in subsection II.B correspond to the switchover point and the low-sensitivity slope, it becomes quite easy to change characteristics to accommodate various types of picture-taking scenarios. Referring to Fig. 8(b), the ratio of the low-sensitivity slope to the high-sensitivity can be given as $(T-T')/Vmid : T/Vsat$ and $Vpoint$ can be given as $Vsat-(Vsat-Vmid)\cdot(T/T')$. For example, when $T' = T/128$ and $Vmid = Vsat/2$, a dynamic range 36 dB greater can be obtained within the output data range.

4.3 Motion detection

Our motion detection method is shown in Fig. 9. The motion flags can be obtained by the product of space derivation and temporal differentiation with any background and object luminance. The temporal differentiation indicates frame difference.

For obtaining the frame difference, we propose duplicated-interlaced processing by negative feedback resetting. Conventional frame difference requires

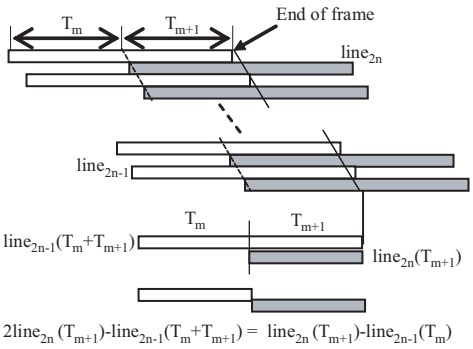


Fig.10: *Duplicated interlaced processing and its frame difference*

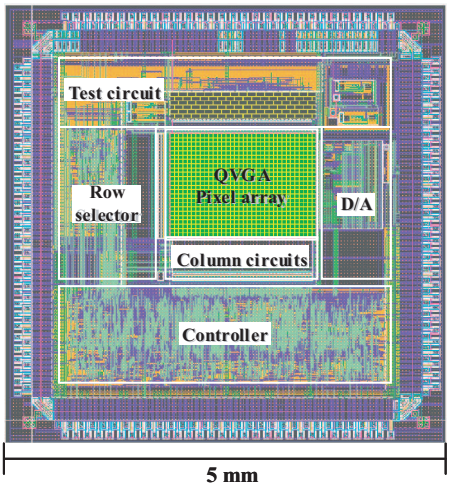


Fig.11: *layout of the trial chip*

frame memory. The duplicated-interlaced processing can generate two images with different exposure time in a frame. Using the similarity of neighboring pixels, the frame difference can be obtained without frame memory (in Fig. 10). However vertical resolution degrades. We implemented the duplicated interlaced processing to image sensor and the calculating space derivation and temporal difference to external unit. The unit requires no frame memory.

Figure 11 and table II show the layout of trial chip and our sensor performance. We confirmed that our sensor achieved HDR compression and motion detection (in Fig. 12 and 13).

5. CONCLUSION

We developed an image-sensor circuit that can perform a reset at any intermediate voltage by using negative feedback. This circuit enables pixels to be individually reset by an intermediate voltage without having to add a selection transistor. Using this reset scheme, we developed techniques for modulating photodiode capacitance in a CMOS image sensor to give it a wide dynamic range, and for detecting objects motion by the duplicated interlaced processing.

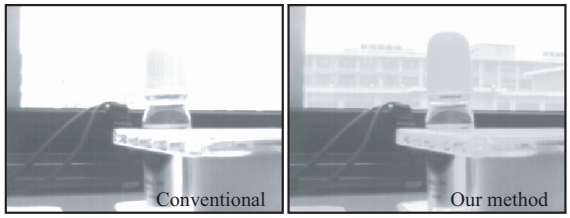


Fig.12: *Image capturing with HDR compression*

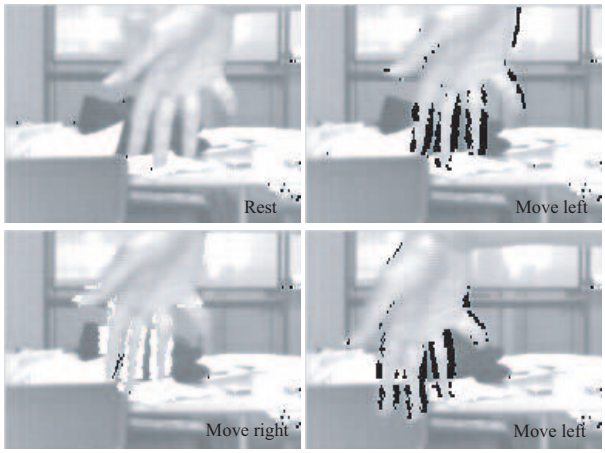


Fig.13: *Example of proposed motion detection*

References

[1] Kagaya R., Ikebe M., Asai T., and Amemiya Y., "On-chip fixed-pattern-noise canceling by negative-feedback reset for CMOS image sensors," *Journal of the Institute of Image Information and Television Engineers*, vol. 59, no. 3, pp. 415-421 (2005). (in Japanese)

[2] M. Ikebe, and K. Saito., "A Wide Dynamic Range Compression Image Sensor with Negative Feedback Resettingh , *IEEE Sensors Journal*, 7, 5, pp. 897-904 (May. 2007)

[3] D. Handoko, S. Kawahito, Y. Tadokoro, and A. Matsuzawa:"ACMOS image sensor with non-destructive intermediate readout mode, for adaptive iterative search motion vector estimation," *IEEE Workshop CCD and Advanced Image Sensors*, pp. 52-55 (June 2001)

[4] M. Sasaki, M. Mase, S. Kawahito, and Y. Tadokoro.,:"A Wide-Dynamic-Range CMOS Image Sensor Based on Multiple Short Exposure-Time Readout With Multiple-Resolution Column-Parallel ADC ," *IEEE Sensors Journal*, VOL. 7, NO. 1, pp. 151-158 (Jan. 2007)

[5] O. Yadid-Pecht.,:"Widening the dynamic range of pictures," *Proc. SPIE 1656*, pp. 374-382 (1992)

[6] B. Choubey, S. Aoyoma, S. Otim, D. Joseph, S. Collins:"An Electronic-Calibration Scheme for Logarithmic CMOS Pixels,"*IEEE Sensors Journal*, VOL. 6, NO. 4, pp. 950-956 (Aug. 2006)

Table 2: *Proposed image sensor performance*

Process	0.25 μm CMOS 1P4M
Resolution	320×240 (QVGA)
Pixel size	5μm × 5μm
Fill factor	40% (w/o μlens)
Transistors per pixel	3Tr./pixel
Sensitivity	0.6V/Lux*sec (with μlens)
Power consumption of column circuit	100μW/column
frame rate	60frame/s@50MHz

Masayuki Ikebe received B.S., M.S. and Ph.D. degrees in electrical engineering from Hokkaido University, Hokkaido, Japan, in 1995, 1997 and 2000, respectively. During 2000-2004, he worked for the Electronic device Laboratory, Dai Nippon Printing Corporation, Akabane, Japan, where he was engaged in the research and development of wireless communication system and image processing system. Presently, he is a Associate Professor of Graduate School of Information Science and Technology at Hokkaido University. His current research includes CMOS-image sensor and RF analog circuits. Dr. Ikebe is a member of IEEE and IEICE.

Junichi Motohisa received B.S., M.S. and Ph.D degrees in electrical engineering from University of Tokyo, Japan, in 1986, 1988, and 1993, respectively. During 1991-1993, he worked as a researcher in ERATO Project supported by Research and Development Corporation of Japan. In 1993, he became a Lecturer (later, Associate Professor) at Research Center of Interface Quantum Electronics (from 2001, Research Center for Integrated Quantum Electronics), Hokkaido University,where he was engaged in the growth and characterization of semiconductor quantum nanostructures including quantum dots and quantum wires. Presently, he is a Professor of Graduate School of Information Science and Technology at Hokkaido University.His current interest includes device and circuit application of nanostructures as well as their fabrication and characterization. Dr. Motohisa is a member of JSAP.