A Low Power SRAM Cell with High Read Stability

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ABSTRACT

In this paper, a 9T static random access memory (SRAM) cell design which consumes less dynamic power and has high read stability is proposed. In conventional six transistor (6T) SRAM cell, read stability is very low due to the voltage division between the access and driver transistors during read operation. Existing 9T SRAM cell design increases the read static noise margin (SNM) by twice as compared to conventional 6T SRAM cell by completely isolating the bit-lines during the read operation. But the write operation is performed in this cell, by charging/discharging of large bit line capacitances causing 22.5% increase in dynamic power consumption. In the proposed technique, the SRAM cell utilizes charging/discharging of a single bit-line (BL) during write operation, resulting in reduction of dynamic power consumption by 45% as compared to a conventional 6T SRAM cell while the read SNM is also maintained at twice the read SNM of the conventional 6T SRAM cell. All simulations of the proposed 9T SRAM cell has been carried out in 0.13 μm CMOS technology.

Keywords: SRAM, Read Stability, Static Noise Margin, Dynamic Power Consumption

1. INTRODUCTION

Semiconductors have seen a revolution over a decade and the trend will continue in terms of area, speed and power. With continuous scaling of the devices to minimize feature size, power and performance have become the predominant concerns. To meet the performance requirements, the amount of embedded SRAM in modern microprocessors and systems-on-chips (SoCs) has increased. Thus designing a SRAM cell that consumes low power is highly desirable. There has been considerable effort over the past several years to design a SRAM cell which operates in low power. This causes a significant degradation in SRAM cell data stability. With each technology generation, the scaling of CMOS devices results in random variations in the number of dopant atoms in the channel region of the device. This causes random variations in the device parameters (in particular, threshold voltage (Vt)) known as random dopant fluctuation (RDF) [1]. SRAM cells are by far the electronic circuits most negatively affected by random fluctuations of the doping concentration [2-3]. Moreover SRAM cell stability which depends on delicately balanced transistor characteristics degrades with the scaling of CMOS technology [4]. Stability expressed as static-noise-margin (SNM) [5], is defined as the maximum value of DC noise voltage that can be tolerated by the SRAM cell without altering the stored bits. For a device to be robust and insensitive to noise disturbance, it is essential that the "0" and "1" interval be as large as possible [6]. The conventional six transistor (6T) SRAM cell shows poor stability at very small feature size with low power supply. During the read operation, voltage division between the access and driver transistors causes the read stability to be very low. An eight transistor (8T) SRAM cell is proposed in [7] for low voltage operation. It uses additional word line, increasing the metal density, wire delay and enhances capacitive coupling between adjacent word lines. This results in increase of dynamic power consumption. In [8] a nine transistor (9T) SRAM cell is proposed to reduce the power by using a write bit-line balancing circuitry which increases the area overhead. A 9T SRAM cell proposed in [9] enhances the read SNM by twice as compared to conventional 6T SRAM cell but the dynamic power consumption is increased due to conventional write operation with more number of transistors.

Hence in this paper, a 9T SRAM cell is proposed for high read stability and low power consumption. The proposed cell utilises single bit-line (BL) for write operation, resulting in reduction of dynamic power consumption. During read operation, the data storage nodes are completely isolated from the bit-lines, thus enhancing the read static noise margin.

This paper is organized as follows. The proposed 9T SRAM cell is presented in Section 2. Read stability, dynamic power consumption, the effect of process variations and the area of SRAM cells are discussed in Section 3. Finally, some conclusions are offered in Section 4 and References are noted in Section 5.

2. PROPOSED 9T SRAM CELL

Figure (1) shows the conventional 6T SRAM cell with transistor sizing in 130 nm CMOS technology.

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Figure (2) shows the 9T SRAM cell presented in [9]. The data in a conventional 6T SRAM cell as shown in figure (1), is most vulnerable to external noise due to the direct access of the data storage nodes by the access transistors (N3 and N4) connected to bit line (BL) and bit line bar (BLB) respectively. During read operation, the voltage division between the access transistors and cross coupled inverters fluctuate the storage node voltage, resulting in destructive read operation. The 9T SRAM cell in figure (2) has an improved static noise margin (SNM) as compared to conventional 6T SRAM cell. The upper sub-circuit of the memory cell is essentially a 6T SRAM cell (composed of N1, N2, N3, N4, P1, and P2). The two write access transistors (N3 and N4) are controlled by a write signal (WR). The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (N5 and N6) and the read access transistor (N7). The operations of N5 and N6 are controlled by the data stored in the cell. N7 is controlled by a separate read signal (RD). This structure completely isolates the bit lines from the data storage nodes during read operation hence improving the static noise margin (SNM). But during write operation it utilizes both bit line (BL) and bit line bar (BLB) capacitances for charging and discharging, resulting in increased dynamic power consumption.

The sizing of the transistors plays a major role in the data stability of the SRAM cell. If the size of the transistor is larger, the resistance decreases and hence the current conduction capability of the transistor increases. The read stability in 6T SRAM cell is maintained by making the sizes of N1 and N2 transistors larger as compared to N3 and N4. The write stability is maintained by making the sizes of N3 and N4 transistors larger as compared to P1 and P2. The conditions are achieved by maintaining the length of all the transistors to be at minimum (L min = 130 nm) and the width of the transistors are increased from its minimum (W min = 130 nm) value, so that the strength of the required transistors are increased as shown in figure (1).

To reduce the dynamic power consumption, a 9T SRAM cell is proposed in this paper as shown in figure (3). In the proposed 9T SRAM cell, the access transistor N4 is placed in the feedback path and only access transistor N3 is connected to bit line (BL) to store data in the cell. Hence only one bit line capacitance (BL) will be charged and discharged during write operation which results in significant reduction in dynamic power consumption and at the same time the data stability of the 9T SRAM cell as in [9] is also maintained. The upper sub circuit of the proposed cell has 6 transistors composed of N1, N2, P1, P2, N3 and N4. The 9T SRAM cell shown in figure (2) has two write access transistors controlled by a write signal (WR) connected to bit line (BL) and bit line bar (BLB).

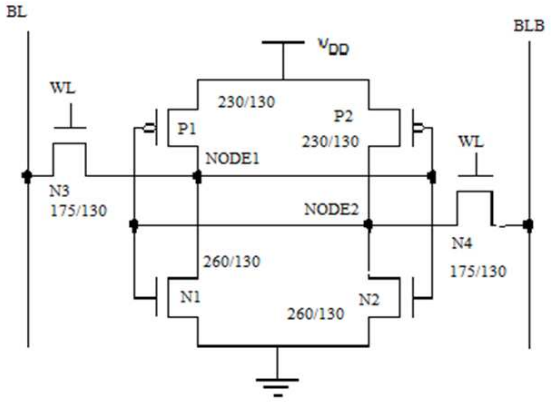

Fig.1: *Conventional 6T SRAM Cell*

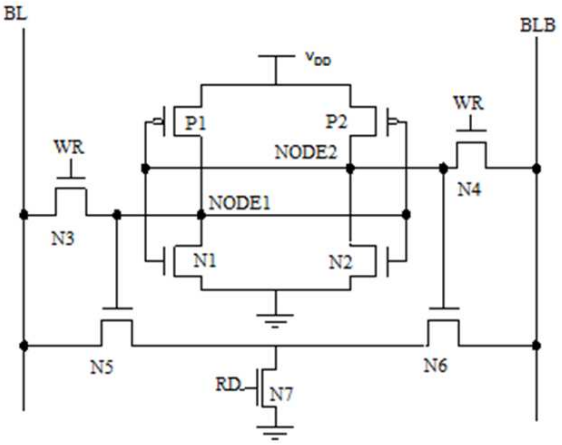

Fig.2: *9T SRAM Cell proposed in [9]*

The proposed cell consists of one write access transistor (N3) connected to BL, controlled by a write signal (WR), and one read and hold access transistor (N4) controlled by a control signal (CTRL). The lower sub circuit of the proposed cell is composed of bit line access transistor (N5), bit line bar access transistor (N6) and read access transistor (N7) controlled by a read signal (RD). As shown in figure (3), during a write operation, WR signal is maintained at a high voltage ("1" level). RD and CTRL signals are maintained at a low voltage ("0" level). Hence the access transistors N4 and N7 are cut OFF and the write access transistor N3 is turned ON. To write a "1" to Node 1, BL is charged and "1" is forced to Node X through N3. This turns ON the transistor N2, forcing "0" into Node 2. This turns ON the transistor P1, forcing "1" into Node 1. Similarly, to write a "0" to Node 1, BL is discharged. Hence, to perform a write operation charging /discharging of only bit line (BL) is utilized.

During a read operation, RD and CTRL signals are maintained at a high voltage ("1" level) while WR is maintained low voltage ("0" level) as shown

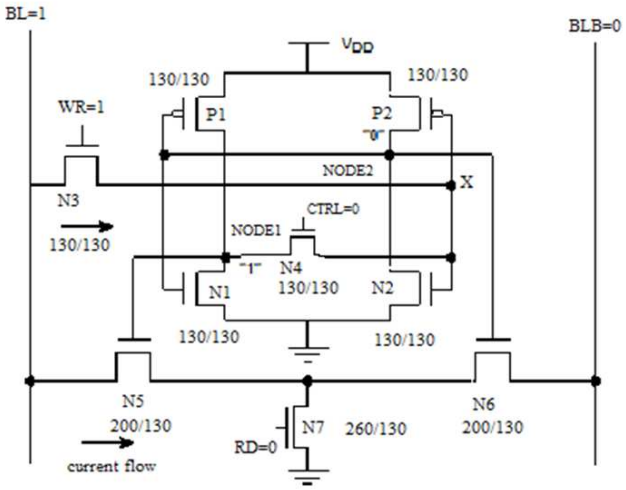

Fig.3: *Proposed 9T SRAM Cell during a write operation*

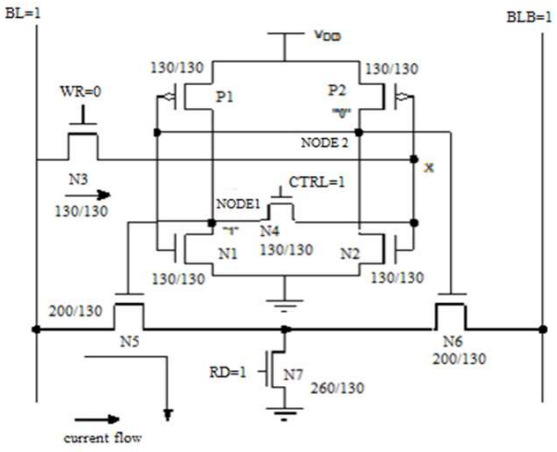

Fig.4: *Proposed 9T SRAM Cell during a read operation*

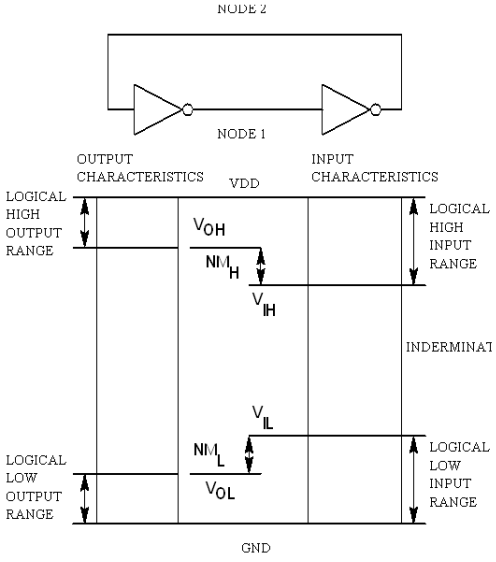

Fig.5: *Noise Margin*

in figure (4). Hence, N3 is cut-off, N4 and N7 are activated. To perform a read operation BL and BLB are initially precharged to a high voltage. Suppose that Node1 stores "1" BL is discharged through N5 and N7. Alternatively, if Node 2 stores "1", BLB is discharged through N6 and N7. Since N3 is cut-off, the storage nodes Node 1 and Node 2 are completely isolated from the bit lines during a read operation.

In Hold mode, Both RD and WR signals are kept in the low level while CTRL signal is kept in high level. Hence N3 and N7 are cut-off and N4 is activated which closes the feedback path in the upper sub circuit that enhances the hold stability of the proposed 9T SRAM cell.

In addition to maintaining the data stability, the sizing of the transistors also decides upon the total leakage power of the SRAM cell. In the proposed 9T SRAM cell, the upper sub-circuit is a conventional 6T SRAM cell. Since the proposed 9T cell has good data stability, the transistors in the sub-circuit, comprising of N1, N2, N3, N4, P1and P2 are chosen to have minimum size, with W = W min and L = L min. Thus, the width of the transistors producing leakage current in the standby mode is chosen to have minimum width as compared to 6T SRAM cell. So, the total leakage power consumed by proposed 9T SRAM cell is less as compared to 6T SRAM cell.

3. SIMULATION RESULTS

3.1 Static Noise Margin (SNM)

A measure of sensitivity of a cell to noise is called noise margin denoted by NM. The noise immunity of the circuit increases with NM. Two noise margins defined are NML (Noise Margin Low) and NMH (Noise Margin High), which quantize the size of the legal "0" and "1" respectively.

These margins should be larger than "0" for a digital circuit to be functional and by preference should be as large as possible. Figure (5) shows the graphical illustration of the noise margins. To characterize the read stability of the SRAM cells, the metric used in this paper is SNM. The SNM of an SRAM cell is defined as the minimum amount of DC noise voltage required to flip the state of the cell [10]. Traditionally, it is modelled by measuring the side of the longest diagonal square that can be inscribed between mirrored DC characteristics of the cross-coupled inverters in a memory cell.

Figure (6) shows the VTC and SNM of the conventional 6T SRAM cell without Vt variations. As illustrated in figure (6), when Node1 of the cell is at VDD, Node2 rises to a higher steady state voltage of 0.125 V due to the voltage division between the access transistor and the pull down transistor in the inverter. Data is more vulnerable to external noise

due to this intrinsic disturbance produced by the direct read access mechanism of the conventional 6T SRAM cell. In order to get the worst case SNM, the supply voltage is maintained at 0.8 volts. The read SNM measured is only 0.15V.

Static VTC and SNM of the proposed 9T SRAM cell during a read operation is shown in figure (7). The read SNM measured is 0.30V. In the proposed 9T SRAM cell the storage nodes Node1 and Node2 are completely isolated from the bit lines during a read operation, as proposed in [9]. This isolation prevents the rising of the node voltages storing "0" from ground level. Hence the read stability of the proposed 9T SRAM cell is thereby maintained at the same level as the 9T SRAM cell in [9] which is twice as compared to the conventional 6T SRAM cell.

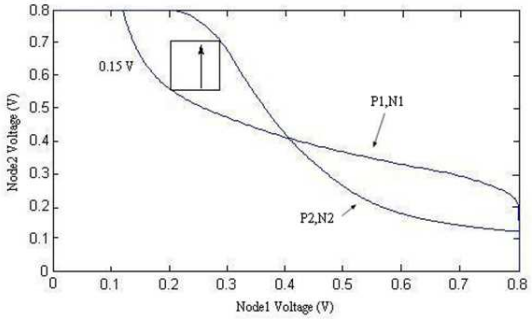

Fig.6: *Static VTC and SNM of the conventional 6T SRAM cell during a read operation*

3.2 Dynamic power dissipation

The dynamic power dissipation occurs due to charging and discharging of load capacitance and short circuit current when both the NMOS and PMOS devices remain ON for short time duration. The former term is usually the dominant term [11-12]. The average dynamic power (Pd) dissipated is given by equation (1)

$$P_d = C_L {V_{dd}}^2 f \tag{1}$$

The power dissipated is proportional to the charging and discharging of load capacitance (C_L), supply voltage (V_{dd}), and the switching frequency (f).
Dynamic power dissipation can be lowered by reducing the switching activity and clock frequency but it affects the performance [13]. Reduction of supply voltage leads to degradation of the cell data stability. Hence in this work charging/discharging of bit line capacitance is reduced to reduce the dynamic power consumption of the SRAM cell without degrading the performance.

In the proposed 9T SRAM cell, to write "1" into the cell, BL has to be charged and to write "0" into cell, BL has to be discharged as illustrated in figure (3). In figure (2), to write "1" into cell BL has to be

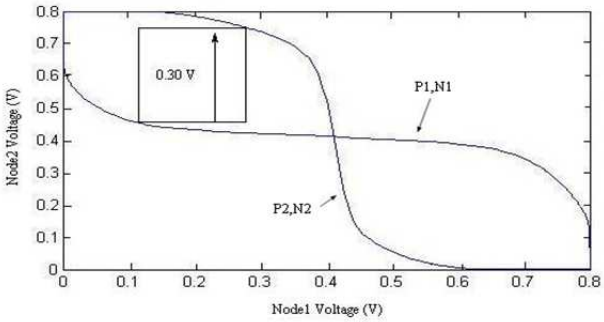

Fig.7: *Static VTC and SNM of the proposed 9T SRAM cell during a read operation*

charged and BLB has to be discharged. Similarly, to write "0" into cell, BL has to be discharged and BLB has to be charged. Hence the bit lines capacitances for charging/discharging during write operation are comparatively higher than in the proposed 9T SRAM cell. This results in the reduction of dynamic power consumption in the proposed 9T SRAM cell. Figure (8) illustrates the amount of power consumed by 6T and 9T SRAM cells. It shows that the power consumption of proposed 9T SRAM cell is reduced by 45% as compared to 6T SRAM cell.

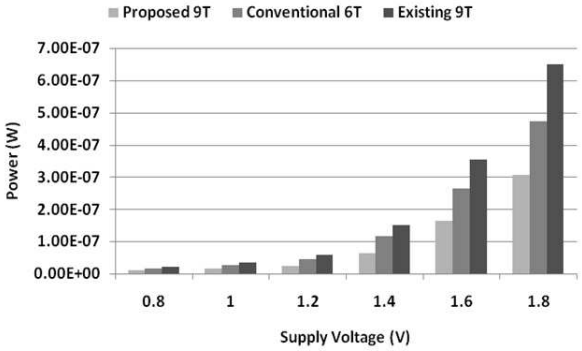

Fig.8: *Power consumption of SRAM cells*

The simulation results of the proposed 9T SRAM cell is also compared with the 8T SRAM cell presented in [7]. The 8T SRAM cell utilises the conventional 6T method of write operation. It has additional read word line (RWL) and read bit line (RBL) to perform the read operation. It has good read stability as compared to 6T cell. In 6T cell, the worst case static noise margin occurs during the read condition. In this case, the pass gate disturbs the storage node "0" by pulling it above ground, which significantly degrades the static noise margin. In 8T cell, with additional word and bit line, the storage nodes are isolated from bit lines. So, the cell disturbs during a read access are effectively eliminated. The read SNM of 8T cell measured is 0.34 V. It is twice as compared to 6T SRAM cell but it is approximately equal to read SNM of proposed 9T SRAM cell (0.3V). This

is because the storage node of proposed 9T cell is also completely isolated from the bit lines. The write operation of 8T cell is however similar to conventional 6T cell utilising the charging and discharging of both write bit line (WBL) and write bit line bar (WBL) capacitances increasing the dynamic power consumption by 17.6% as compared to 6T cell. But in the proposed 9T cell, dynamic power consumption decreases by 45% as compared to 6T cell.

3.3 Impact of Process Variations

Process variations are posing a major challenge to nanoscale integrated circuits design. Hence, the read stability of the conventional 6T and proposed 9T SRAM cells with process parameter variations (in particular, threshold voltage (V_t)) are evaluated. Vt is assumed to have -50% to +50% uniform variations in all transistors. Monte Carlo simulations are run to evaluate the read stability. The static voltage transfer characteristics (VTC) and the worst case SNM of the conventional 6T and the proposed 9T SRAM cells for a read operation under process parameter variations are shown in figure (9) and figure (10) respectively.

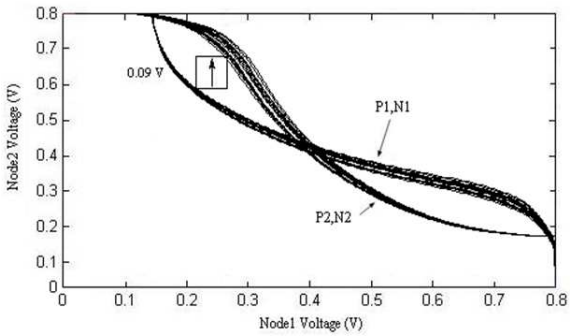

Fig.9: *Static VTC and SNM of conventional 6T SRAM cell during a read operation under process variations*

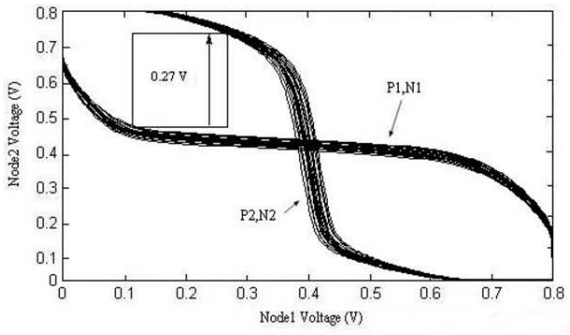

Fig.10: *Static VTC and SNM of the proposed 9T SRAM cell during a read operation under process variations*

Process parameter variations degrade the read SNMs of the conventional 6T and the proposed 9T SRAM cells. The worst-case read SNM of the conventional 6T SRAM cells under process parameter variations is degraded by up to 40% as compared to the read SNM at the nominal design corner as shown in figure (6) and figure (9). Alternatively, the worst-case read SNM of the proposed 9T SRAM cell is 10% lower as compared to the nominal process corner as shown in figure (7) and figure (10). The proposed 9T SRAM cell provides three times higher worst-case SNM as in [9] when compared to the conventional 6T SRAM cell under process parameter variations. Table 1 gives the comparison results of the conventional 6T, 9T in [9] and proposed 9T SRAM cell for dynamic power consumption and read SNM under nominal Vt and under process parameter variations. It shows that the dynamic power consumption of the proposed 9T SRAM cell is reduced by 45% as compared to conventional 6T SRAM cell while there is 22.5% increase in dynamic power consumption in the 9T SRAM cell [9], under normal operating voltage of 1.2 volts.

Table 1: *SNM and power comparison*

SRAM Cells	Read SNM under Nominal V_t	Read SNM under Process Parameter variations	Dynamic power consumption
Conventional 6T Cell	0.15 V	0.09 V	44.4 nW
9T Cell in [9]	0.30 V	0.27 V	57. 3 nW
Proposed 9T cell	0.30 V	0.27 V	24.4 nW

3.4 Area Comparison

The layouts of 6T and the proposed 9T SRAM cells are shown in figure (11) and figure (12) respectively. The 6T SRAM cell size is 3.5 μm $\times$ 3.1 μm which consumes an area of 11.16 μm^2 in 130 nm technology. The proposed 9T SRAM cell size is 4.8 μm $\times$ 4.4 μm which consumes an area of 21.12 μm^2 resulting in an increase of area by 47% as compared to the conventional 6T SRAM cell.

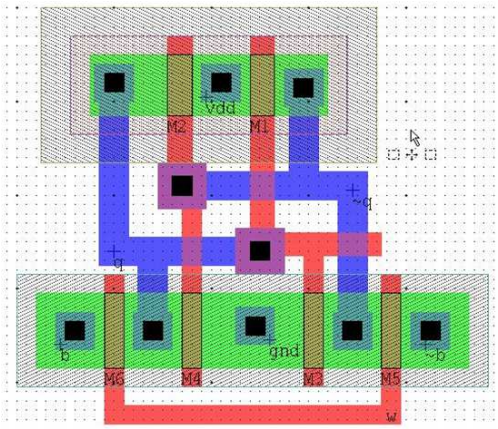

Fig.11: *Layout of 6T SRAM cell*

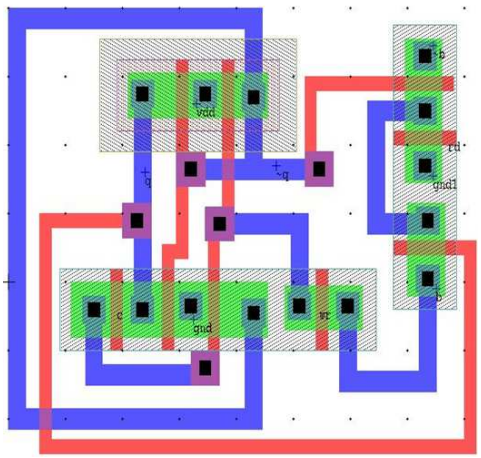

Fig.12: *Layout of proposed 9T SRAM cell*

4. CONCLUSION

A Novel 9T SRAM cell is presented in this paper for high read stability and low dynamic power consumption. The proposed 9T SRAM cell provides two separate data access mechanisms for read and write operations. During a read operation, the data storage nodes are completely isolated from the bit lines, thereby improving the read SNM by twice as compared to the read SNM of the conventional 6T SRAM cell. The data stability of the proposed 9T SRAM cell is also verified under process parameter variations. During the write operation, the SRAM cell utilizes the charging/discharging of only one bit line (BL), resulting in reduction of dynamic power consumption by 45% as compared to conventional 6T SRAM cell while there is an increase of 22.5% in the 9T SRAM cell in [9].

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