Exploring of Third-Order Cascaded Multi-bit Delta- Sigma Modulator with Interstage Feedback Paths

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ABSTRACT

The emergence of mixed-signal integrated circuit results in the tremendous increase in the numbers of high performance data converters with the trend toward high resolution and large bandwidth. Delta-Sigma modulator, employing oversampling technique, provides high output precision by shaping the in-band quantization noise to the out-of-band. This paper explores characteristics of Thirdorder cascaded multi-bit Delta-Sigma modulator with interstage feedback paths using behavioural simulation. Comparisons between mathematical models with behavioural models are demonstrated for theoretical analysis. Simulation models with various non-ideal sources of Delta-Sigma modulator are presented. A comparative analysis of non-ideal effects including sampling jitter noise, integrator noise, integrator nonidealities, and capacitor mismatch on a cascaded architecture with interstage feedback paths of a Thirdorder multi-bit Delta-Sigma modulator are also discussed.

Keywords: Delta-Sigma Modulator, Non-idealities, Simulation Model, Interstage, Feedback Paths

1. INTRODUCTION

Delta-Sigma modulator exploits an oversampling technique and digital signal filtering to achieve high resolution of digital output bits. The resolution of Delta- Sigma modulator generally can be increased by adding the order of the modulator or its sampling frequency.

A cascaded (**M**ulti-st**A**ge noise **SH**aping: MASH) modulator typically uses stable lower-order modulator, such as first and second-order modulator, to form a highorder modulator. By employing a cascaded modulator, it can mitigate instability problems.

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The use of internal multi-bit quantizer increases the signal-to-noise ratio (SNR) of modulator and lowers the required oversampling ratio for given resolutions. However, the major drawback of cascaded multi-bit modulator is that the capacitor mismatch in a multi-bit DAC results in the DAC nonlinearity problem. In typical VLSI fabrication technology process, the smallest capacitor mismatch that can be achieved is on the order of 0.1-0.5% [1]. The error from nonlinearity of DAC still remains unshaped at the output of each modulator stage and causes the deterioration of modulators performance.

Most analog non-idealities in cascaded multi-bit modulator consist of coefficient mismatches, integrator leakages, and DAC nonlinearity. Among those, in theory, the most deterioration performance of modulator is the DAC nonlinearity errors [2]. To minimize the DAC nonlinearity problems, four major approaches [1] have been proposed: Element trimming approaches, Dynamic element matching techniques, Digital correction techniques, and Innovative architectures.

Innovative architectures have been widely proposed in many research works to solve the DAC nonlinearity problems. The techniques can be grouped into: dualquantizer architecture [3,4], multiple dualquantizer architecture with interstage scaling [5], and multi-bit structure with extra feedback paths [6,7]. Because dualquantizer architecture techniques can only increase the modulators order by one, the highest noise-shaping function is limited to third-order. The more complex circuit design and large die area make multiple dualquantizer architecture techniques less attractive. Therefore, this paper focuses on multi-bit structure with extra feedback paths.

Because a cascaded multi-bit modulator employs a multi-bit DAC in the loop, capacitor mismatch in a multibit DAC causes the DAC nonlinearity problem. An architecture that improves the performance deterioration caused by the DAC nonlinearity in a cascaded multi-bit Delta-Sigma modulator is presented in [6] and shall be referred to as the modified architecture in this paper. The modified architecture with the extra feedback paths in each internal stage can totally cancel the DAC nonlinearity errors of the final stage. In addition, the modified architecture also

increases one order of noiseshaping function for DAC error of other internal stages compared to a conventional cascaded (MASH) architecture. As a result, comparing results between the modified architecture and a conventional MASH architecture, improvement of SNR of the modified topology has been observed.

For general structure of Delta-Sigma modulator, analog non-idealities that affect on the modulator performance can be classified into four categories [8]: sampling jitter noise, integrator noise (kT/C thermal noise, amplifier thermal noise), integrator non-idealities (amplifier finite DC gain, amplifier slew-rate, and amplifier bandwidth), and capacitor mismatch.

Referring to [8-11], a second-order modulator is used to demonstrate effects of non-idealities as an example. A low-pass second-order modulator and a band-pass sixthorder single-loop modulator are analyzed in [12]. However, cascaded architectures are more sensitive to capacitor mismatch than simple second order modulators [11]. In this paper, a comprehensive study on the effects of non-idealities on both a conventional and the modified architectures is also presented. All four categories of circuit non-idealities including sampling jitter noise, integrator noise, integrator non-idealities, and capacitor mismatch are examined on both architectures.

The outline of this paper is organized as follows. The introduction is briefly discussed in Section 1. In Section 2, the concept of cascaded architectures with interstage feedback paths, which prevents the performance degradation by the DAC nonlinearity errors, is described. Details of behavioural simulation model of Delta-Sigma modulators in MATLAB Simulink tool are presented in Section 3. In Section 4, discussions of simulation results in both effects of DAC nonlinearity errors and other various circuit non-idealities are covered. Finally, conclusions and summary table are given in Section 5.

2. THE CONCEPT OF CASCADED ARCHITECTURES WITH INTERSTAGE FEEDBACK PATHS

Previously, concepts of a conventional Third-order cascaded (1-1-1) multi-bit Delta-Sigma modulator and a cascaded architecture with interstage feedback paths have been proposed in [13] and [6], respectively. In this section, mathematical analysis of both a conventional modulator and a cascaded architecture with interstage feedback paths are discussed comparatively in details.

2.1 A Conventional Cascaded Architecture

A conventional Delta-Sigma modulator is composed of three stages: First-order modulator in the first, second and third stages (MOD-1, MOD-2 and MOD-3, respectively) as shown in Fig. 1.

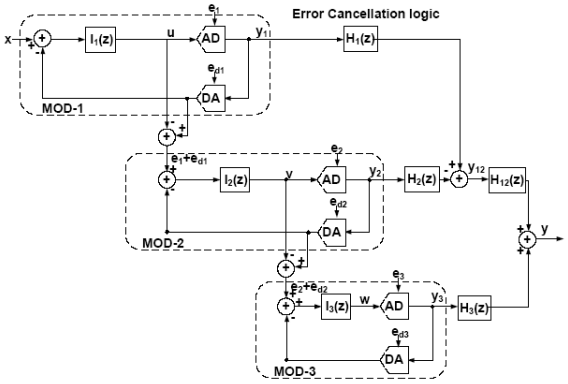

Fig.1: *Conventional Third-order Cascaded multi-bit Modulator*

For linear model analysis, the quantization errors and the DAC errors can be treated as additive white noise [1]. Assumed all the integrator functions are equal

$$I_1(z) = I_2(z) = I_3(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{1}$$

where the error cancellation logic are selected as $H_1(z) = z^{-1}$,$H_2(z) = 1 - z^{-1}$, $H_{12}(z) = z^{-1}$ and $H_3(z) = (1 - z^{-1})^2$, respectively. As a result, the overall modulator output can be derived as

$$\begin{aligned} y &= z^{-3}x + (1 - z^{-1})^3 e_3 - z^{-2} e_{d1} + z^{-1}(1 - z^{-1}) e_{d2} \\ &- z^{-1}(1 - z^{-1})^2 e_{d3} \end{aligned} \tag{2}$$

where the quantization errors and the DAC errors are denoted as e_1, e_2 and e_3, and e_{d1}, e_{d2} and e_{d3}, respectively.

Equation (2) shows that the internal quantization errors, e_1 and e_2, are totally cancelled out, while internal quantization error of the final stage, e_3 is shaped by a third-order noise function and remains at the output of the modulator. Moreover, the DAC error caused by DAC nonlinearity of the first stage, ed1 remains unshaped, while the other stage DAC errors, e_{d2} and e_{d3} are only shaped by first-order and second-order noise function, respectively. As a result, such errors, which remain at the output of the modulator, may cause the deterioration of modulators performance.

2.2 The Modified Cascaded Architecture

The modified architecture of a Third-order cascaded (1-1-1) multi-bit Delta-Sigma modulator is shown in Fig. 2. The idea of the modified architecture is to create extra internal feedback paths around the structure to shape the DAC errors further than the error cancellation logic [6]. The modified architecture has the DAC error feedback path at each stage,

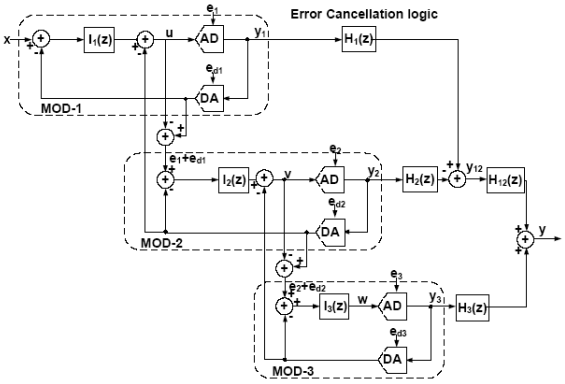

Fig.2: *The Modified Third-order Cascaded multi-bit Modulator*

excluding the first stage, to its previous stage and is summed at the integrators output of previous stage.

For linear model analysis, assumed the integrator function, $I_1(z)$, $I_2(z)$ and $I_3(z)$ are equal

$$I_1(z) = I_2(z) = I_3(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{3}$$

The output transfer function of each stage, MOD-1, MOD-2 and MOD-3, can be expressed as

$$y_1 = u + e_1 = 1I_1(x - y_1 - e_{d1}) - (y_2 + e_{d2}) + e_1 \tag{4}$$

$$y_2 = v + e_2 = I_2(e_1 + e_{d1} - y_2 - e_{d2}) - (y_3 + e_{d3}) + e_2 \tag{5}$$

$$y_3 = w + e_3 = I_3(e_2 + e_{d2} - y_3 - e_{d3}) + e_3 \tag{6}$$

where the digital error cancellation logic are selected as $H_1(z) = z^{-1}$, $H_2(z) = (1 - z^{-1})^2$, $H_{12}(z) = z^{-1}$ and $H_3(z) = (1 - z^{-1})^3$. The overall modulator output can be obtained as

$$y = z^{-3}x + (1 - z^{-1})^3 e_3 - z^{-2}e_{d1} + z^{-1}(1 - z^{-1})^2 e_{d2} \tag{7}$$

Equation (7) shows that the internal quantization errors, e_1 and e_2, are totally cancelled out, while internal quantization error of the final stage, e_3 is shaped by a third-order noise function. Moreover, the DAC error of the final stage, e_{d3} is totally cancelled out. The DAC error, e_{d2} is also shaped with higher one-order noise shaping function than a conventional architecture while e_{d1} remains unshaped. As a consequence, the modified architecture provides the significant improvement over a conventional architecture for DAC nonlinearity error reduction.

3. BEHAVIOURAL SIMULATION MODEL

The increasing demands of complexity of analogdigital converter drive the utilizing of behavioural simulation models become necessary during system-level design stage in top-down approach. The primary advantages of behavioural simulation models are fast and less time consuming. The MATLAB Simulink tool is used for behavioural models of Delta-Sigma modulator because it provides accurate and reliable results [8,9]. In this section, behavioural simulation models are presented for both a conventional and the modified architectures. The blocks of 17-level quantizer ADC-DAC given in [9] are adopted to verify the influence of the DAC nonlinearity errors. Fig. 3 shows a conventional Thirdorder cascaded (1-1-1) multi-bit (4b-4b-4b) modulator simulation model. The digital error cancellation logic of a conventional modulator is shown in Fig. 4.

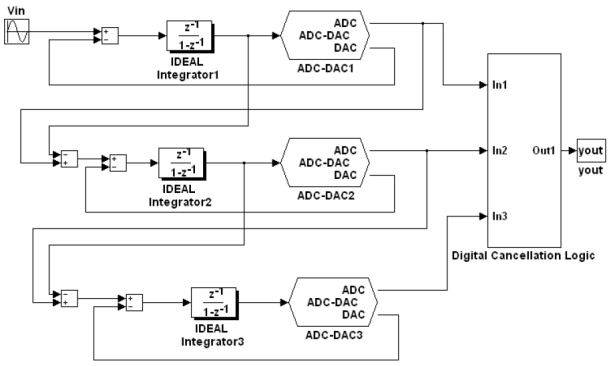

Fig.3: *A Conventional Third-order Modulator Simulation Model*

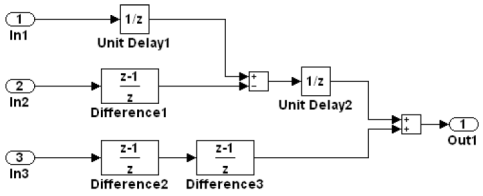

Fig.4: *A Digital Error Cancellation Logic of a Conventional Modulator*

The modified architecture with interstage feedback paths of Third-order cascaded (1-1-1) multi-bit (4b-4b- 4b) modulator simulation model is shown in Fig. 5. The digital error cancellation logic of the modified modulator is selected slightly different than a conventional one based on mathematical analysis in Section 2 as shown in Fig. 6.

Fig. 7 shows a conventional Third-order cascaded multi-bit modulator with non-ideal simulation model. The modified architecture of Third-order cascaded multi-bit modulator with non-ideal simulation model is shown in Fig. 8. The integrator non-idealities are taken into account only the first integrator with other ideal integrators in both simulation models because the first integrator mainly determines performance of Delta-Sigma modulator [8].

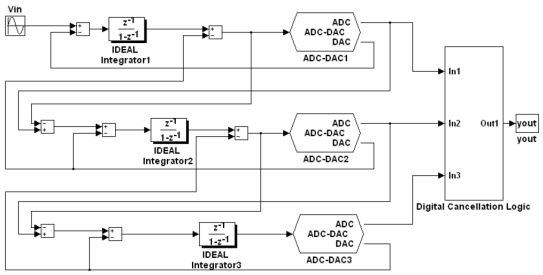

Fig.5: *The Modified Third-order Modulator Simulation Model*

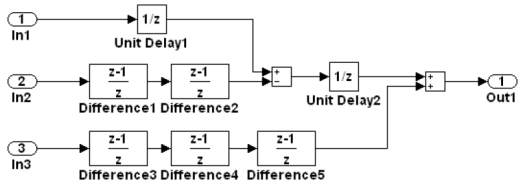

Fig.6: *A Digital Error Cancellation Logic of the Modified Modulator*

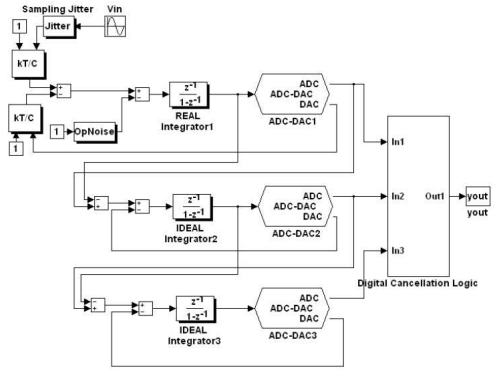

Fig.7: *A Conventional Third-order Modulator with Nonideal Simulation Model*

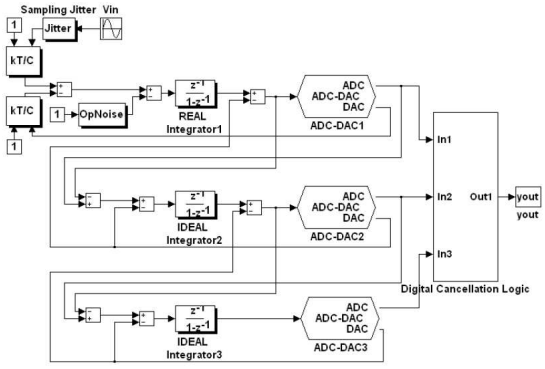

Fig.8: *The Modified Third-order Modulator with Nonideal Simulation Model*

4. SIMULATION RESULTS

In this section, simulation results of both effects of DAC nonlinearity errors and other various circuit nonidealities on a cascaded architecture with interstage feedback paths of a Third-order multi-bit Delta-Sigma modulator are discussed. The simulation model parameters used throughout this paper are summarized in the Table 1.

Table 1: *Simulation Model Parameters*

Parameter	Value
Input signal amplitude	Ampl = 0.9 V
Input frequency	F_{in} = 1 kHz
Signal bandwidth	BW = 19.53 kHz
Oversampling ratio	R =32
Sampling frequency	F_s= 1.25 MHz
Number of samples	N =16384
Reference feedback voltage	V_{refp} = 1 and V_{refn} = -1
Sampling capacitance of the first integrator	C_s= 2.5 pF
Total DAC capacitance value	CST = 2.5 pF
Capacitor mismatch	0.45%

4.1 Effects of DAC Nonlinearity Errors

To observe the only effect of DAC nonlinearity errors, the simulation models were simulated without other modulator non-idealities such as sampling jitter, integrator noise, integrator non-idealities, and capacitor mismatch unless stated otherwise. Table 2 summarizes the effects of each DAC error on both a conventional and the modified modulators with different input signal amplitude. It can be observed from simulation results that the DAC error of the first stage of modulator (DAC1) affects the highest SNR loss of the modulator.

The SNR values are calculated with the bandwidth of 19.53 kHz. The maximum capacitor mismatch is set to 0.45% to observe the effects of DAC nonlinearity errors on performance of modulators. In case of non-idealities [8], the simulation models were simulated with the first integrator output noise of 10 $\mu V/\sqrt{Hz}$, op-amp DC finite gain of 2×10^3, op-amp saturation of 1.25 V, slew-rate of 30 V/μs and op-amp finite bandwidth of 100 MHz. Fig. 9 shows the power spectral density of a conventional modulator with different conditions. The results show that DAC errors cause the most significant SNR loss and higher effect on modulators performance than other nonidealities for a conventional modulator.

Fig. 10 shows the power spectral density of the modified modulator. By comparing Fig. 9 with Fig. 10, the power spectral density in case of ideal DAC between a conventional and the modified modulators are similar. The results agree with the mathematical analysis which derived in Section 2. Without the DAC errors (ed1, ed2 and ed3), the overall modulator output of a conventional and the modified modulators equation (2) and (7) respectively must be the same. Considering the DAC errors, the effects of DAC nonlinearity errors cause a large amount of SNR losses

Table 2: *A Comparison of Resolution between a Conventional and the Modified Modulator*

Resolution (bits)		
Input signal amplitude (Ampl = 0.9 V)		
Effect of DAC error parameter	Third-order cascaded (1-1-1) modulator	
	Conventional	Modified
Ideal DAC	17.94	17.94
DAC3	17.69	17.94
DAC2	17.62	17.94
DAC1	12.25	13.44
DAC2 and DAC3	17.66	17.94
DAC1, DAC2 and DAC3	12.26	13.51
Input signal amplitude (Ampl = 0.7 V)		
Effect of DAC error parameter	Third-order cascaded (1-1-1) modulator	
	Conventional	Modified
Ideal DAC	17.61	17.61
DAC3	17.38	17.61
DAC2	17.18	17.61
DAC1	11.89	13.48
DAC2 and DAC3	17.14	17.61
DAC1, DAC2 and DAC3	11.89	13.61
Input signal amplitude (Ampl = 0.5 V)		
Effect of DAC error parameter	Third-order cascaded (1-1-1) modulator	
	Conventional	Modified
Ideal DAC	16.86	16.86
DAC3	16.92	16.86
DAC2	16.47	16.86
DAC1	11.19	12.82
DAC2 and DAC3	16.46	16.86
DAC1, DAC2 and DAC3	11.2	12.84

to both ideal a conventional and the modified modulators. However, the results reveal that the modified modulator has better immunity to DAC nonlinearity errors than a conventional modulator.

A comparison of dynamic ranges with different total DAC capacitance for both a conventional and the modified modulators with DAC errors is shown in Fig. 11. It can be observed with varying input signal from -120 to 0 dB in log-scale (0.000001 V to 1 V) that the modified modulator has better performance within the period of -10.46 dB to -0.35 dB (0.3 V to 0.96 V). In another word, the modified modulator does not outperform the conventional modulator in all input signal level. However, it performs better during the larger range from 0.3 to 0.96 V when the total input signal ranges from 0.000001 to 1 V.

In case of typical ideal value of capacitor mismatch in VLSI process, the maximum capacitor mismatch between two unit components is set to 0.1% [6]. Fig. 12 compares the amounts of SNR losses caused by DAC nonlinearity errors for both a conventional and the modified modulators. Both modulator models were simulated with ideal and non-ideal DAC nonlinearity error conditions. In case capacitor mismatch of 0.45%, it can be seen that a conventional modulator has significant SNR losses due to DAC nonlinearity errors when the input signal amplitude is less than -10.46 dB. On the other hand, the modified modulator has less SNR losses caused by DAC nonlinearity errors. When capacitor mismatch is set to 0.1%, the SNR loss due to DAC nonlinearity errors are nearly identical in both modulators since lower capacitor

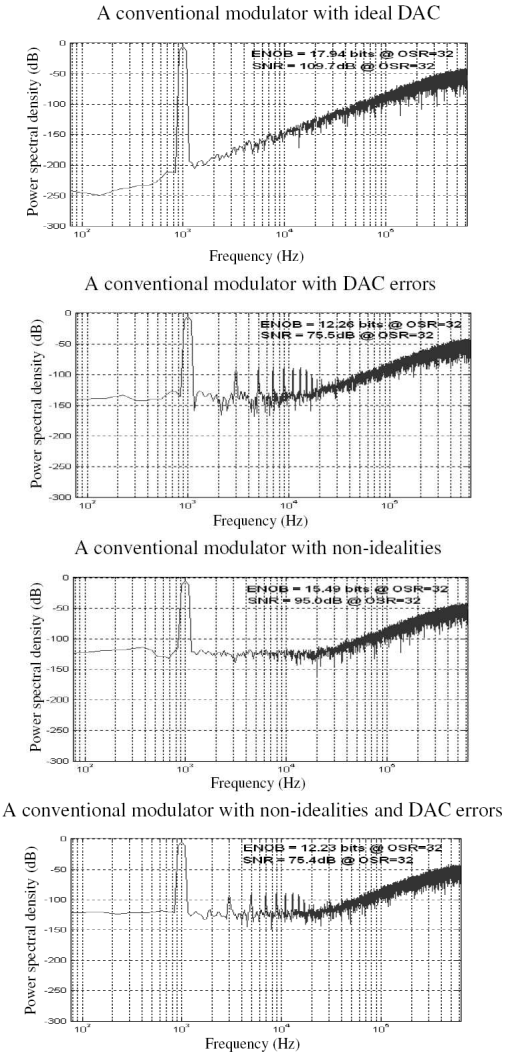

Fig.9: *Power Spectral Density of a Conventional Modulator with Different Conditions*

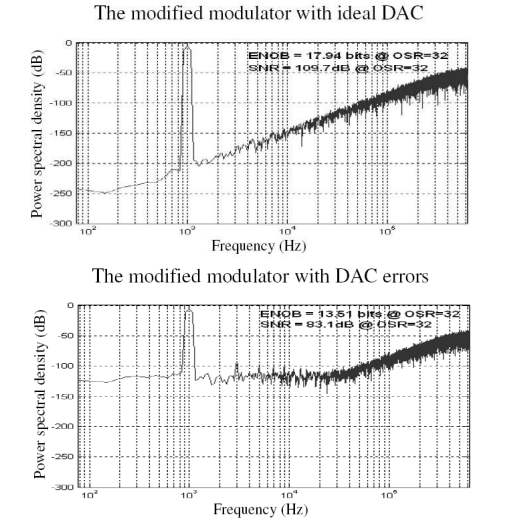

Fig.10: *Power Spectral Density of the Modified Modulator with Different Conditions*

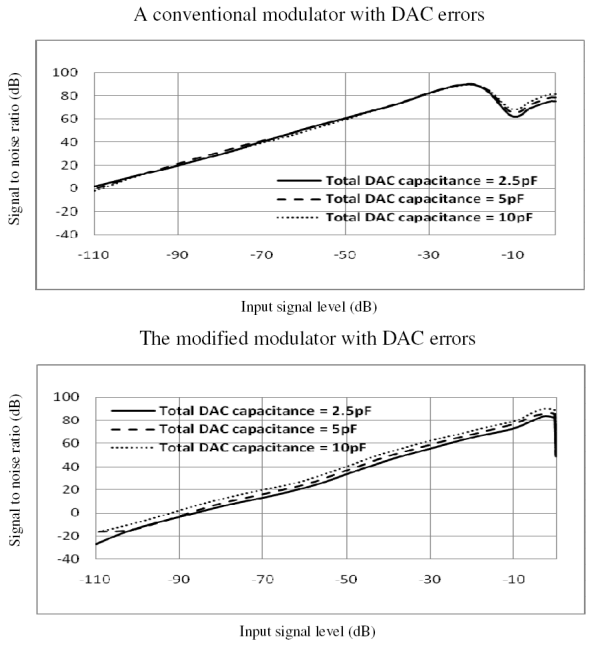

Fig.11: *Comparison of Dynamic Range with Different Total DAC Capacitance*

mismatch results in lower DAC nonlinearity errors. Fig. 13 shows a comparison of dynamic ranges with different capacitor mismatch of both a conventional and the modified modulators with DAC errors. It can be seen that higher capacitor mismatch results in larger deterioration of modulators performance.

4.2 Effects of Other Non-idealities

Simulation results of the power spectral density comparing ideal case with each of specific non-ideal case are illustrated as the following sequences: sampling jitter noise, integrator noise (kT/C thermal noise, amplifier thermal noise), integrator non-idealities (amplifier finite DC gain, amplifier slew-rate, and amplifier bandwidth), and capacitor mismatch. In addition, each of specific nonidealities is investigated whether affects on the in-band noise floor or harmonic distortions.

A.Effects of Sampling Jitter Noise

Fig. 14 shows the power spectral density in case of including sampling jitter effect (the sampling jitter noise is set to (a) 0 s (ideal), (b) 1 ps, (c) 1 ns, and (d) 1 μs). Fig. 15 illustrates the effect of SNR with sampling clock jitter varied from 1 ps to 1 s. The results reveal that sampling jitter noise affects on the modified modulator similar to a conventional modulator.

B.Effects of Integrator Noise (kT/C Thermal Noise, Amplifier Thermal Noise)

The power spectral density of both a conventional and the modified modulators with kT/C thermal noise effects is shown in Fig. 16. Because kT/C thermal noise is inversely proportional to the sizing of

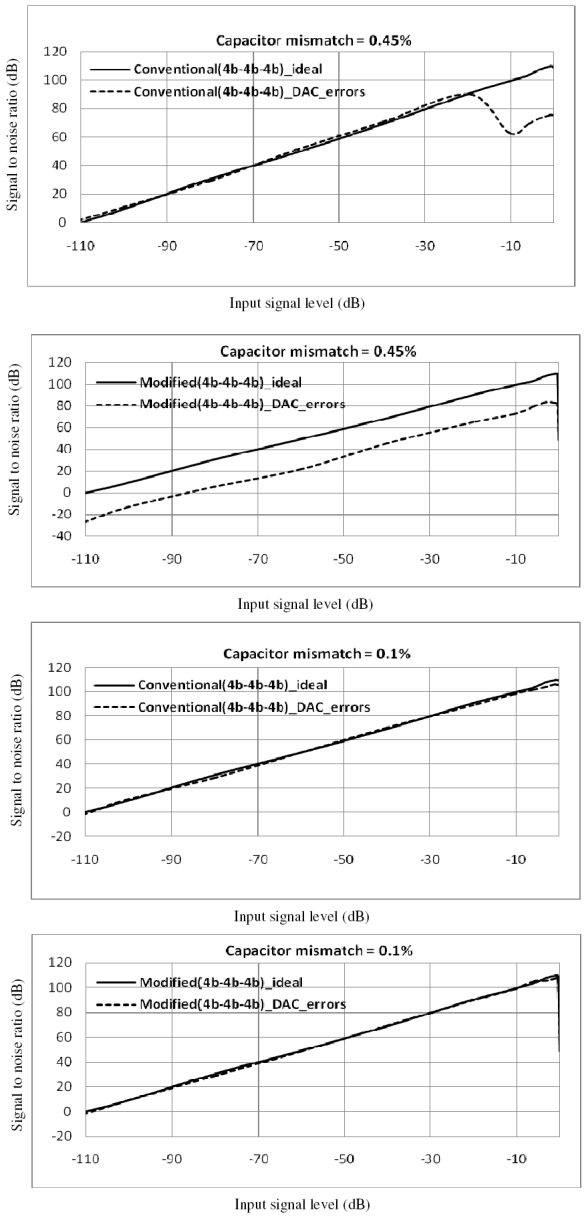

Fig.12: *Comparison of Dynamic Range between Ideal and DAC errors with both a Conventional and the Modified Modulators*

input sampling capacitor, the value of the input sampling capacitor is set to vary from (a) 10 nF, (b) 0.1 nF, (c) 1 pF, and (d) 10 fF. The effect of the value of the input sampling capacitor (from 1 fF to 1F) on SNR is shown in Fig. 17. The results show that the effect of kT/C thermal noise on a conventional modulator is same as the modified modulator.

Fig. 18 illustrates the power spectral density in case of including effect of amplifier thermal noise with (a) 0 $\mu V/\sqrt{Hz}$ (ideal), (b) 0.1 $\mu V/\sqrt{Hz}$, (c) 1 $\mu V/\sqrt{Hz}$, and (d) 10 $\mu V/\sqrt{Hz}$. Fig. 19 shows the effect the amplifier thermal noise on SNR from 0.001 $\mu V/\sqrt{Hz}$ to 1000 $\mu V/\sqrt{Hz}$. The results indicate that there is no difference between the effect

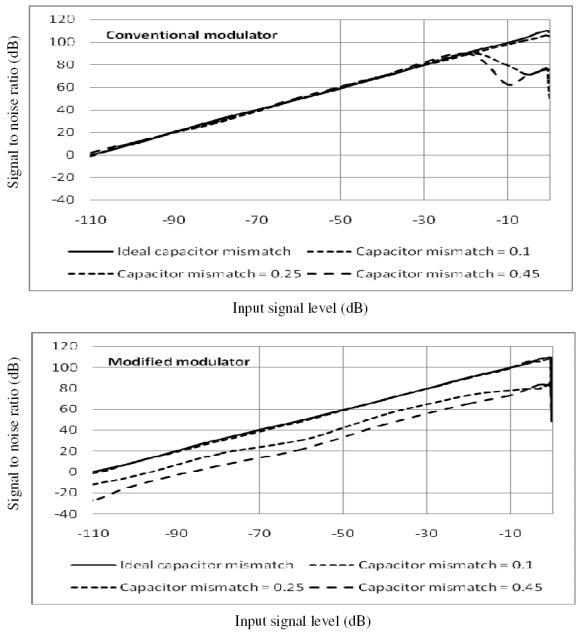

Fig.13: *Comparison of Dynamic Range of with Different Capacitor Mismatch with both a Conventional and the Modified Modulators with DAC*

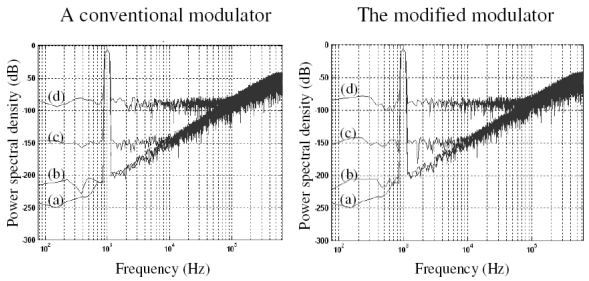

Fig.14: *Effect of Sampling Jitter Noise on Power Spectral Density*

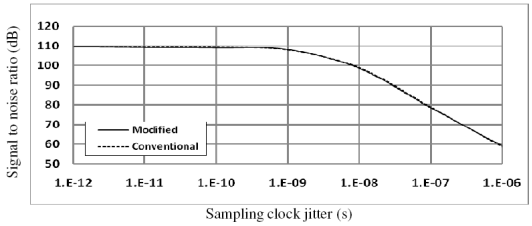

Fig.15: *SNR vary with Sampling Clock Jitter*

of amplifier thermal noise on a conventional and the modified modulators.

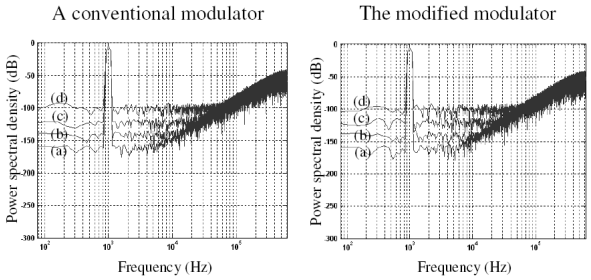

Fig.16: *Effect of kT/C Thermal Noise on Power Spectral Density*

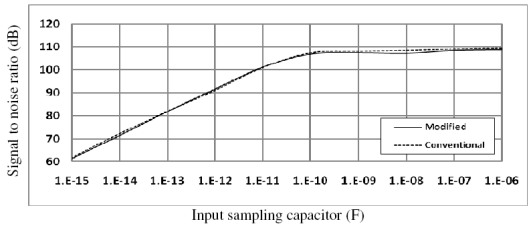

Fig.17: *SNR vary with Input Sampling Capacitor*

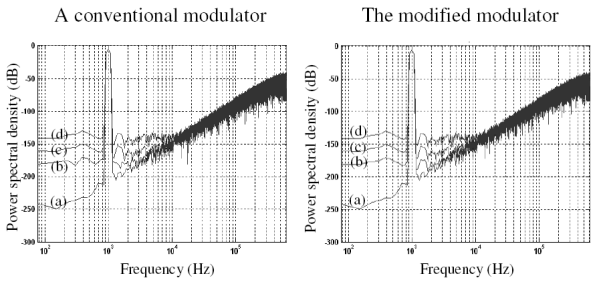

Fig.18: *Effect of Amplifier Thermal Noise on Power Spectral Density*

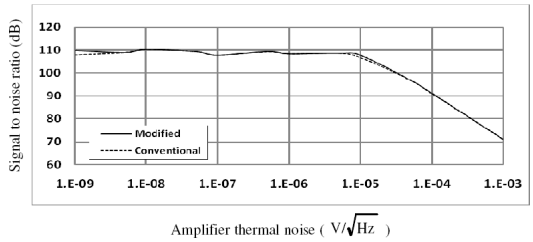

Fig.19: *SNR vary with Amplifier Thermal Noise*

C. Effects of Integrator Non-idealities (Amplifier Finite DC Gain, Amplifier Slew-rate, and Amplifier Bandwidth))

Fig. 20 shows the effect of amplifier DC gain on the power spectral density with (a) 40 dB, (b) 70 dB,

(c) 100 dB, and (d) 130 dB amplifier DC gain. The effect of amplifier DC gain varied from 10 dB to 150 dB on SNR is shown in Fig. 21. The results show that the modified modulator has better noise immunity to amplifier finite DC gain non-ideality than a conventional modulator.

The power spectral density with amplifier slew-rate which set to (a) 0.1 V/μs, (b) 1 V/μs, (c) 2 V/μs, and (d) 3 V/μs is shown in Fig. 22. Fig. 23 illustrates the effect of SNR with amplifier slew-rate varied from 0.1 V/μs to 3 V/μs. It can be seen that the modified modulator does not cause harmonic distortions as appearing in a conventional modulator when amplifier slew-rate is limited. However, more in-band noise floor of modified modulator causes the SNR to be lower than a conventional modulator.

Fig. 24 shows the power spectral density with the effect of amplifier bandwidth. The amplifier bandwidth is set to (a) 0.01 MHz, (b) 0.1 MHz, (c) 1 MHz, and (d) 10 MHz. Fig. 25 illustrates the effect of SNR with amplifier bandwidth varied from 0.001 MHz to 100 MHz. The results reveal that the effect of limited amplifier bandwidth does not cause harmonic distortions on the modified modulator. In contrast, both in-band noise floor and harmonic distortions are introduced to a conventional modulator when amplifier bandwidth is limited.

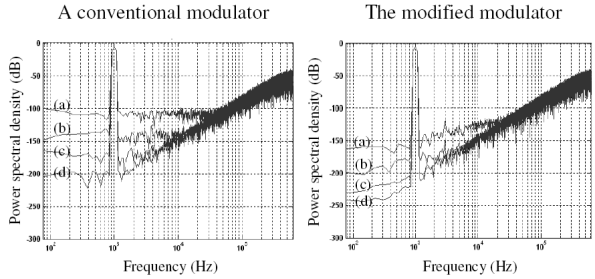

Fig.20: *Effect of Amplifier Finite DC Gain on Power Spectral Density*

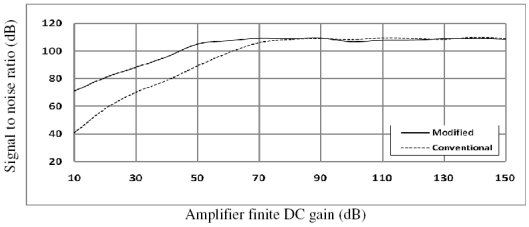

Fig.21: *SNR vary with Amplifier Finite DC Gain*

D. Effects of Capacitor Mismatch

Fig. 26 illustrates the power spectral density with capacitor mismatch effects. The capacitor mismatch is set to (a) 0% (ideal), (b) 0.1 %, (c) 0.3 %, and (d) 0.5 %. It can be observed in the results that harmonic distortions appear in the modified modulator is less

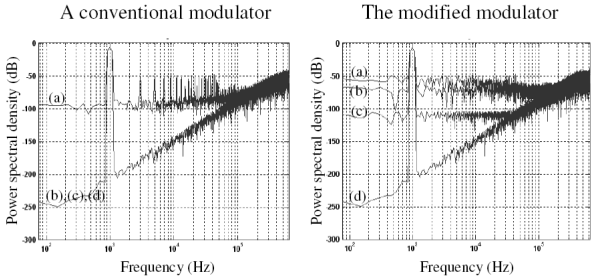

Fig.22: *Effect of Amplifier Slew-rate on Power Spectral Density*

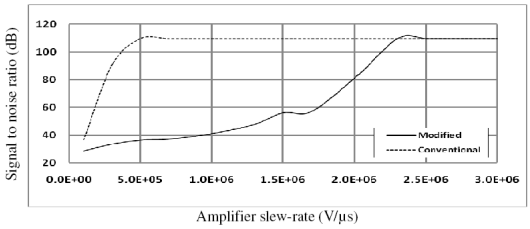

Fig.23: *SNR vary with Amplifier Slew-rate*

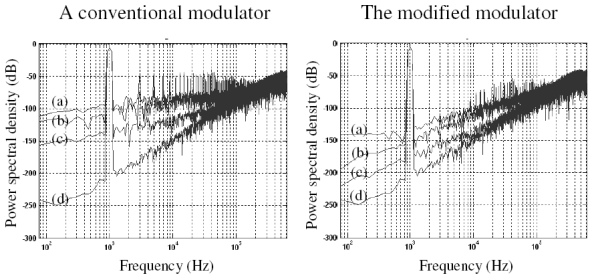

Fig.24: *Effect of Amplifier Bandwidth on Power Spectral Density*

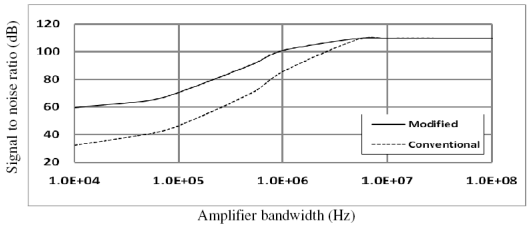

Fig.25: *SNR vary with Amplifier Bandwidth*

than a conventional modulator when high capacitor mismatch is introduced. According to mathematical analysis in Section 2, with the modified architecture, the DAC error of the second stage, e_{d2} is shaped with higher one-order noise shaping function than a conventional architecture. Additionally, the DAC error of the final stage, e_{d3} is totally cancelled out. As a result, the modified modulator has better noise shaping function associated with DAC errors caused by capacitor mismatch than a conventional modulator. Fig. 27 shows effects of SNR with capacitor mismatch

varied from 0% to 0.5% (typical standard VLSI process). The result shows that the modified modulator has better SNR than a conventional modulator. In other words, the modified modulator has better immunity to DAC nonlinearity errors than a conventional modulator when including effects of DAC errors caused by capacitor mismatch.

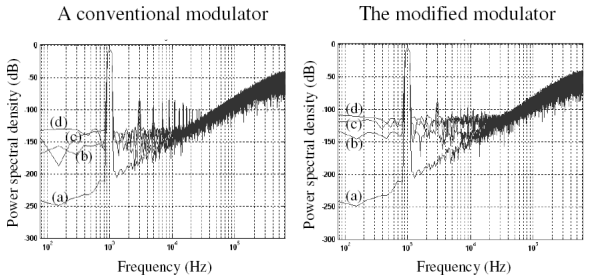

Fig.26: *Effect of Capacitor Mismatch on Power Spectral Density*

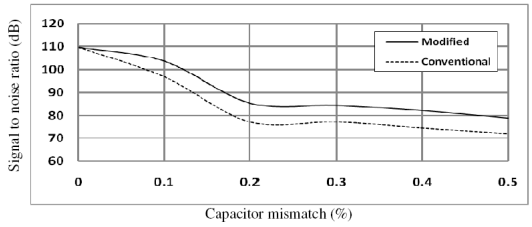

Fig.27: *SNR vary with Capacitor Mismatch*

5. CONCLUSION

A study of non-ideal effects on special architecture allow us to design carefully regarding this concerns and precisely estimate specifications of particular modulator basic building blocks at the early stage of design without deteriorated performance of modulator caused by nonidealities. In this paper, we have investigated characteristic of Third-order cascaded (1-1-1) multi-bit (4b-4b-4b) Delta-Sigma modulator with interstage feedback paths in behavioural simulation model. The concept of DAC nonlinearity error reduction technique for a third-order cascaded multi-bit Delta-Sigma modulator is presented. Behavioural simulations have been also performed for DAC errors as well as other analog non-idealities in both ideal and non-ideal cases.

Initially, analysis effects of DAC nonlinearity errors caused large degradation of modulator performance are studied. DAC nonlinearity problems in each stage of a conventional and the modified modulators have been analyzed. Behavioural simulation results show that, among modulator non-idealities, the most deterioration of modulators performance is caused by DAC nonlinearity errors. Moreover, the results reveal that the DAC error caused by the first stage of the cascaded modulator affects the highest SNR loss of the modulator. The effect of both total DAC capacitance and capacitor mismatch parameters to dynamic range of modulators has also been analyzed.

Finally, we demonstrate a comprehensive analysis of other analog non-ideal effects whether on the in-band noise floor or harmonic distortions of third-order cascaded modulator with interstage feedback paths. Table 3 summarizes the effects (the in-band noise floor and harmonic distortions) of each of specific non-idealities on both modulator architectures. It can be concluded from simulation results that non-ideal effects of amplifier DC finite gain, slew-rate, and bandwidth cause different inband noise floor and harmonic distortion results on both a conventional and the modified modulators.

Table 3: *Summary of Non-ideal Effects*

Non-idealities	Conventional		Modified	
	In-band noise floor	Harmonic distortions	In-band noise floor	Harmonic distortions
Samping jitter noise	Yes	-	Yes	-
kT/C thermal noise	Yes	-	Yes	-
Amplifier thermal noise	Yes	-	Yes	-
Amplifier finite DC gain	Yes	-	Yes	Yes
Amplifier slew-rate	Yes	Yes	Yes	-
Amplifier bandwidth	Yes	Yes	Yes	-
Gain capacitor mismatch	Yes	Yes	Yes	Yes

6. ACKNOWLEDGEMENT

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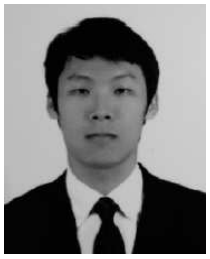

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