RF Energy Harvesting using Cross-coupled Rectifier and DTMOS on SOTB with Phase Effect of Paired RF Inputs

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ABSTRACT

In this paper, the design and evaluations of a cross-coupled rectifier (CCR) with floating sub-circuit using Dynamic Threshold MOSFET (DTMOS) for RF energy harvesting is presented. The circuit is fabricated using 65 nm Silicon on Thin Buried Box (SOTB) CMOS technology. The measurement result shows that the circuit exceeds 1000 mV DC output at –14 dBm input power and obtains 48 % power conversion efficiency (PCE) at a level of –10 dBm input power. The proposed circuit generated 0.9 μW DC output power at a level of –21 dBm input power which is equivalent to 10.6 % PCE when harvesting the 950 MHz LTE signal in the ambient environment. The study also indicates the effect of the phase difference between the two RF input signals on the DC output voltage in a CMOS CCR. The DC output voltage depends on the phase of the two RF input signals and reaches a maximum when the phase difference between the two RF signals is π. Experimental results demonstrate that the output voltage changes from 950 mV to –100 mV when the phase difference varies from π to 0 at an RF input power of –10 dBm. When the rectifier receives an RF signal from the environment at an input power of –21 dBm, the DC output voltage changes from 300 mV to –50 mV when the phase difference changes from π to 0.

Manuscript received on September 17, 2019 ; revised on March 16, 2020 ; accepted on May 30, 2020. This paper was recommended by Editor Apinunt Thanachayanont.

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Digital Object Identifier 10.37936/ecti-eec.2020182.216617

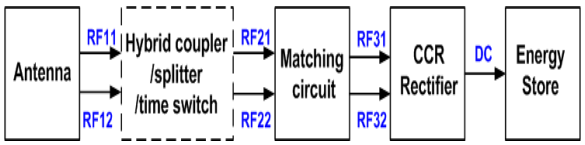

Fig.1: *Block diagram of a RFEH system*

Keywords: 65 nm SOTB, DTMOS, Cross-Coupled Rectifier, Phase Difference, RF Energy Harvesting

1. INTRODUCTION

Recently, the expansion of the Internet of Things (IoT) applications has a strong influence on human life. In IoT technique, energy harvesting takes an important role because the energy harvesting system is an essential solution to eliminate batteries for IoT applications [1]. RF energy harvesting (RFEH), which converts an RF signal in the ambient environment into a DC signal has received an increase in attention as a energy harvesting technique. The RF signal is very common in the environment where people are living today such that it becomes an ideal energy source for energy harvesting. However, the amount of RF level in the ambient environment is extremely low, usual μW level [2], [3]. At the low input power range, the input signal is lower than the threshold voltage (V_{th}) of the active component used for rectifying, resulting in a significant decrease in the PCE. Certain V_{th} cancellation techniques were proposed to boost the PCE of the system such as self V_{th} cancellation technique [4], differential-drive topology [5], and CCR with floating sub-circuit bias [6].

DTMOS has been shown to obtain much higher drain current than other normal MOSFET [7]. DTMOS was proposed in RFEH technique earlier in Dickson topology [8], self V_{th} cancellation [9], cross-coupled rectifier [10]. In [6], the PCE of CCR with floating sub-circuits exceeds that of conventional CCR. In this paper, we propose the application of DTMOS to CCR with floating sub-circuits. The circuit was fabricated using 65nm SOTB CMOS technology [11] because the threshold voltage of SOTB MOSFET can be changed to be larger than the bulk so that DTMOS becomes more effective.

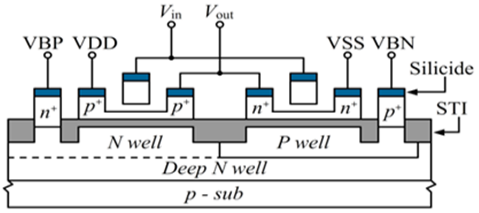

Fig.2: *Structure of SOTB CMOS inverter: VBN is the body of NMOS and VBP is the body of PMOS [11].*

Table 1: *RF characteristics of 65 nm SOTB*

	PMOS	NMOS
Gate length	60 nm	60 nm
Gate oxide thickness	2.0 nm	2.0 nm
Threshold Voltage	−0.32 V	0.35 V
F_T	26 GHz	40 GHz
F_{max}	20 GHz	28 GHz

Fig. 1 presents a block diagram of an RFEH system using CCR. In general, the RFEH system consists of an antenna, a matching circuit, a rectifier circuit, and an energy store. Depending on the application, in some cases, the RFEH system also has some additional parts such as splitter, time switch [1]. Because the structure of CCR is differential-drive topology, so RF signals supplied to the rectifier, which is RF_{31} and RF_{32} in Fig. 1, are required to be symmetrical signals. The requirement is ensured by the former parts of the RFEH system which consist of the antenna and rectifier in general, and the power divider for optional applications. Normally, a dipole antenna or a loop antenna, that can generate the two differential RF output signals, is suitable to utilize in the system. In addition, to increase the RF input power by harvesting multiple RF signals, the broadband antenna and wide bandwidth antenna are proposed [12], [13]. These antennas have one RF output, hence, there needs to be a hybrid coupler, which is used to create the differential signals from the input RF signal.

The design of differential power divider is proposed in [14], [15]. In the studies, the measurement results indicated that the phase difference between the two RF outputs of the divider is not ideal as π. Hence, the phase difference of the paired RF signals RF_{31}, and RF_{32} of the rectifier is different from π. In this study, we indicate the effect of the phase difference of the two paired RF inputs of the rectifier on its operation.

The paper is organized as follows: in Section 2, the design of DTMOS CCR with floating sub-circuits is presented. Section 3 indicates the effect of the phase difference of the paired RF inputs on the output of the CCR. Sections 4 and 5 present measurement results with a signal generator and with real RF signals in the environment. Section 6 presents the conclusion.

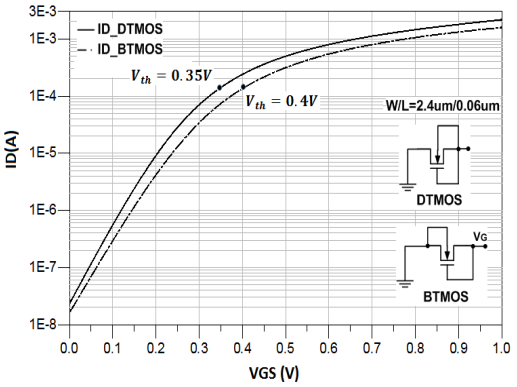

Fig.3: *ID-VD characteristics of DTMOS and BTMOS*

2. CROSS-COUPLED RECTIFIER USING DTMOS WITH FLOATING SUB-CIRCUIT ON 65 NM SOTB

2.1 Dynamic threshold MOSFET on 65 nm SOTB technology

The cross-sectional diagram of SOTB CMOS is shown in Fig. 2 [11]. In [16], the RF characteristics of 65 nm SOTB CMOS are measured and presented as shown in Table 1. f_{max} of PMOS and NMOS SOTB are 20 GHz and 28 GHz, respectively. Therefore, it can be concluded that the 65 nm SOTB technology is effective for application in frequency 1 GHz.

Fig. 3 shows the ID-VGS characteristic simulated results of DTMOS and Body tied to source MOSFET (BTMOS). From the figure, the threshold voltage of DTMOS is 0.35 V, lower than that of BTMOS which is 0.4 V. Besides, the drain current of DTMOS is higher than the drain current of BTMOS at the same value of V_{GS} voltage. From these results, it can be concluded that the application of DTMOS to rectifier in low input power ranges can provide higher efficiency than using BTMOS.

2.2 Proposed circuit structure

The proposed circuit consists of three-stage CCR with floating sub-circuits [6] as shown in Fig. 4. In each stage, two cross-coupled sub-circuits supply bias voltages for gate ports of MOSFETs in the main circuit. The loads of the sub-circuits are open so that DC levels at $FL_{11}, FL_{12}, FL_{21}, FL_{22}$ are boosted. These voltages are supplied to gates and bodies of MOSFETs in the primary circuit, thus making the circuit work more effectively in a low input power range than the simple CCR. Coupling capacitors in each stage are C_{mp} = 1 pF, C_{sp} = 0.5 pF. Load capacitor C_L = 10 μF. Chip micrograph and the photo of the RF energy harvesting system are shown in Figs. 5 and 6.

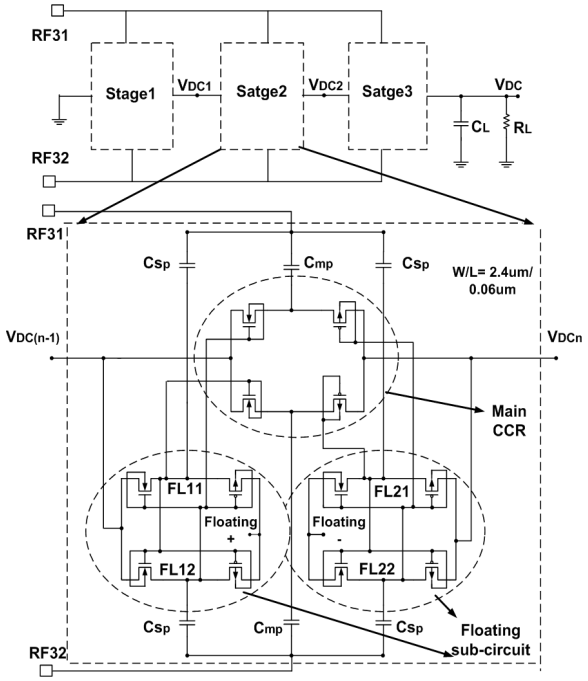

Fig.4: *Cross-coupled DTMOS rectifier with floating sub-circuit.*

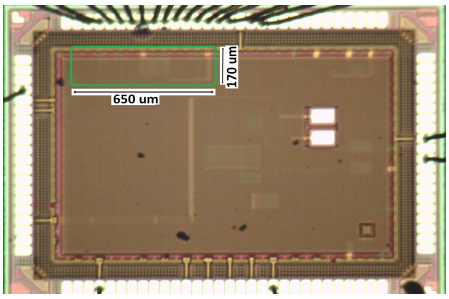

Fig.5: *Chip micrograph.*

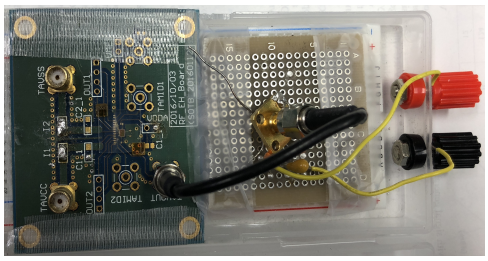

Fig.6: *The RF energy harvesting system.*

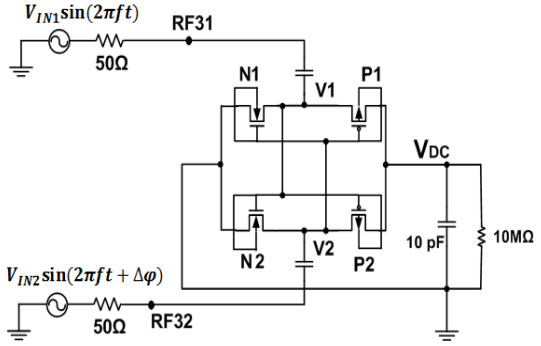

Fig.7: *Cross-coupled rectifier.*

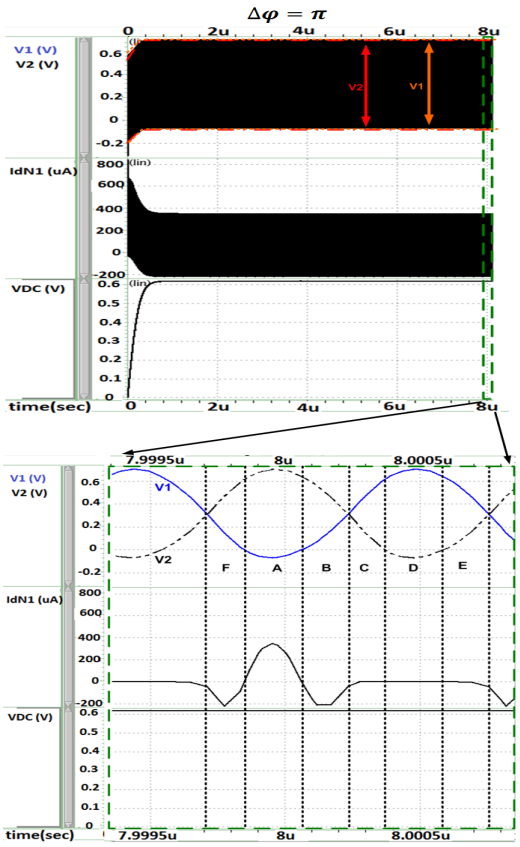

Fig.8: *Steady-state simulated time-domain waveforms of voltages and drain currents in NMOS N1 when* $\Delta\varphi = \pi$

3. EFFECT OF PHASE DIFFERENCE ON CROSS-COUPLED RECTIFIER AND SIMULATION RESULTS

To simplify analysis of the effect of the phase difference between the two RF inputs of the rectifier on its output voltage, in this section the configuration of a stage cross-couple rectifier is utilized as shown in Fig. 7. The two paired RF input signals are supplied by two sine wave voltage sources with a phase difference between them of $\Delta\varphi$. In [17], the steady-state simulated time-domain waveforms of NMOS N1 in the case $\Delta\varphi = \pi$ was specified in detail, as shown in Fig. 8. The simulation condition are at 954 MHz, $V_{in1} = V_{in2} = 0.4$ V and the load is 10 MΩ. Positive current is a forward current that charges the load. Negative current is a flow-back current that discharges the load. Owing to the symmetry of CMOS devices, the drain and source should be switched for analysis depending on these potentials. As a result, V_{GS} will be $(V_2 - V_1)$ or V_2 depending on which is higher.

The operation of the CCR in case of being supplied by two differential RF signals can be divided into

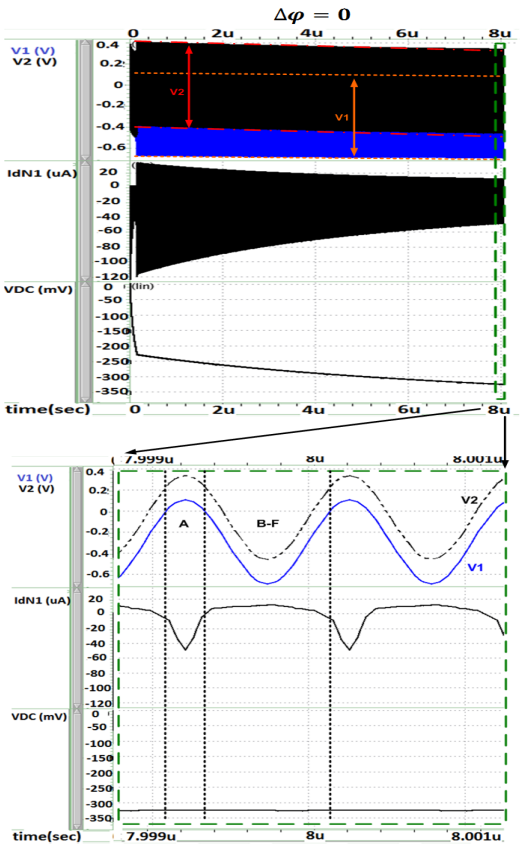

Fig.9: *Steady-state simulated time-domain waveforms of voltages and drain currents in NMOS N1 when* $\Delta\varphi = 0$

6 regions as shown in Fig. 8. In region A, where $V_{GS} > V_{th}$ and $V_1 < 0$, the current is forward current and reaches the highest value because $V_{GS} = (V_2 - V_1)$ reaches the highest absolute value. In regions B to F, because $V_1 > 0$ so $V_{GS} = V_2$ and $V_{DS} = V_1$. The currents in these regions are flow-back currents and have negative values. In region B and F, the absolute values of V_2 decrease in comparison with that of region A, then the absolute values of V_{GS} in these regions are smaller than those in region A. Therefore, the absolute values of the drain currents in these regions are smaller than that in region A. In regions C and E, $V_2 < V_{th}$ so these region are sub-threshold regions resulting drain current dramatically decreasing. In region D, $V_2 < 0$ so in this region NMOS is in off-mode. The current in the load is an integral of all currents in a cycle. In this case, the drain current in region A dominates the drain current in the cycle so the current in the load is a forward current and the output voltage is positive.

Fig. 9 presents the steady-state simulated time domain waveforms of voltages and currents of N1 when $\Delta\varphi = 0$. In region A, where $V_{GS} = V_2$ reaches highest value, $V_1 > 0$ so the current in this region is flow-back current. In regions B to F, where $V_1 < 0$

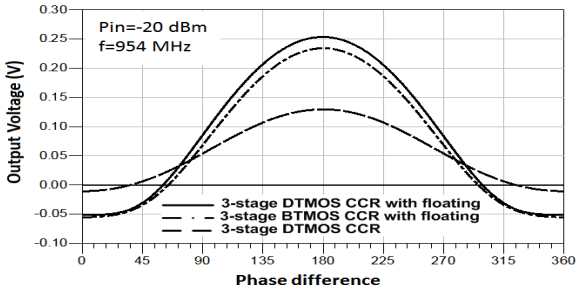

Fig.10: *Dependence of DC output voltage with* $\Delta\varphi$ *in 3-stage CCR, 3-stage CCR with floating sub-circuit using DTMOS and BTMOS.*

and $V_{GS} = V_2 - V_1$, the currents are forward currents and have smaller value than that in region A because V_{GS} reduces. The major drain current in this case is flow-back current and the output voltage is negative.

From the analysis, the output voltage of CCR depends not only on the absolute value of the two RF input signals but also on the phase difference between them. These dependencies are shown through simulation results of three 3-stage-CCR types: simple CCR, CCR with floating circuit using DTMOS, CCR with floating circuit using BTMOS (Fig. 10). The simulation conditions have an input power of –20 dBm, a load of 10 MΩ, and a frequency of 954 MHz. It can be seen from Fig. 10 that with all rectifier types the DC output voltage strongly depends on the phase difference between the paired RF inputs. The output voltage reaches the peak value when $\Delta\varphi = \pi$ and significantly decreases when $\Delta\varphi$ changes. Fig. 10 also shows the efficiency of the proposed circuit in comparison with the same stage of CCR and the same configuration using BTMOS. When $\Delta\varphi = \pi$, the output voltage of the proposed circuit reaches 240 mV while that of 3-stage CCR is 130 mV, and that of 3-stage CCR with floating circuits using BTMOS is 220 mV.

4. EXPERIMENTAL RESULTS WITH SIGNAL GENERATOR

In the measurement, evaluation conditions were set up as shown in Fig. 11. Signal generator (SG) SMJ100A is used to generate the RF signal to the input of a hybrid coupler KRYTAR 4010124. The RF signal then is divided into two RF signals by the coupler and supplied to the rectifier. Phase difference between points RF_{21} and RF_{22} in Fig. 11 is notated by $\Delta\varphi(RF_{21}, RF_{22})$. The phase difference between points RF_{31} and RF_{32} is denoted by $\Delta\varphi$, and it is the phase difference of the two RF inputs supplied to the rectifier. These phase differences are calculated by Eqs. 1 and 2:

$$\Delta\varphi\,(RF_{21}, RF_{22}) = \begin{cases} 0 & for \quad \Sigma \quad port \\ \pi & for \quad \Delta \quad port \end{cases} \qquad (1)$$

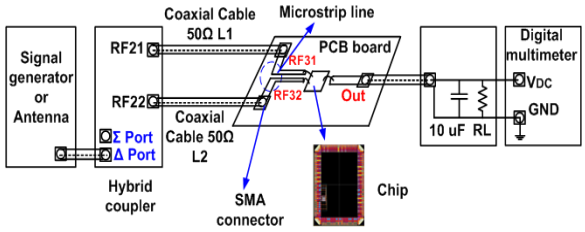

Fig.11: *Evaluation conditions.*

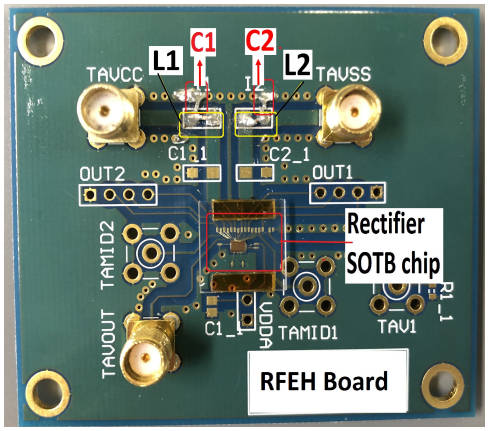

Fig.12: *The rectifier with matching circuit*

$$\Delta\varphi = \frac{2\pi}{\lambda_P}(L_1 - L_2) + \varphi(V_{RF21}, V_{RF22}) \qquad (2)$$

where L_1 and L_2 are lengths of coaxial cables used for connecting between the hybrid coupler and the rectifier board. λ_P is a wavelength of the RF signal in the coaxial cable.

4.1 Performance of DTMOS CCR with floating sub-circuits

To test the performance of the rectifier, matching circuits are attached in the rectifier PCB board as shown in Fig. 12. In the board, L type matching circuits are designed to match the two RF inputs of rectifier circuit with 50 Ω SMA connectors. Here, inductors L_1 and L_2 are 2 nH each. Capacitors C_1 and C_2 are 6.5 pF each. In this measurement, lengths of the coaxial cables are the same and Δ port is used so that the phase difference $\Delta\varphi$ is π. Figs. 13 and 14 show measured output voltage and PCE of the rectifier at 1 GHz frequency and different loads. In our measurement, the output voltage is measured up to a limitation of 1.3 V to avoid damage MOSFETs.

The PCE of the rectifier is calculated by

$$PCE = \frac{P_{DCout}}{P_{RFin}} = \frac{V_{Out}^2}{R_L P_{RFin}} \qquad (3)$$

As shown in Fig. 13, the rectifier obtained a sensitivity of 1 V at –14 dBm input power. From Fig. 14, the highest PCE of the rectifier is 48 % at a level of –10 dBm input power and a 10 kΩ load. These results prove the efficiency of the CTMOS CCR with floating sub-circuits.

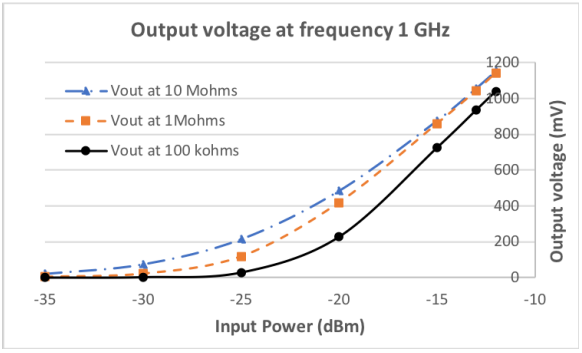

Fig.13: *Measured output voltage of the rectifier at 1 GHz.*

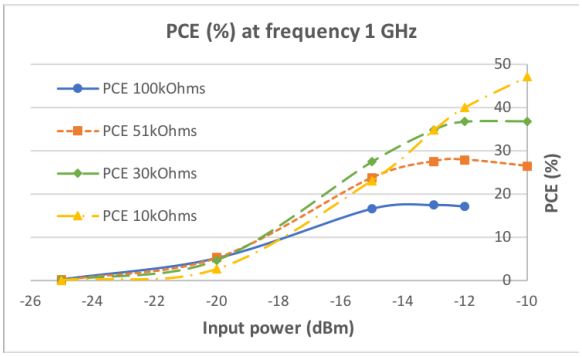

Fig.14: *Measured PCE of the rectifier at 1 GHz.*

4.2 Evaluation of phase effect with signal generator

Matching circuits were not used in the measurements to evaluate the phase effect at different frequencies. The phase difference of two RF signals of the rectifier is calculated in (2). From the equation, by changing the connecting ports of the hybrid coupler which are the Σ port and Δ port, or changing the length of the coaxial cables, the phase difference effect is evaluated.

In the first measurement, the cable lengths are kept the same so that when Σ port and Δ port of the coupler are used, the phase differences $\Delta\varphi$ are 0 and π, respectively. Figs. 15 and 16 show simulated and measured results at three frequencies. The output voltage was measured at a 10 MΩ load and over a wide range of input power.

When $\Delta\varphi = \pi$, all DC output voltages are positive in different frequencies and input power values. When $\Delta\varphi = 0$, all DC output voltages are negative. At 954 MHz and an input power of –10 dBm, the output voltage changes from 950 mV to –100 mV when $\Delta\varphi$ changes from π to 0. It can concluded in the figures that the measurement results demonstrate satisfactory agreement with simulation results at 954 MHz.

In the next measurement, the cable length is changed to drive $\Delta\varphi$ following Eq. 2. Fig. 17 presents measured and simulated phase differnece

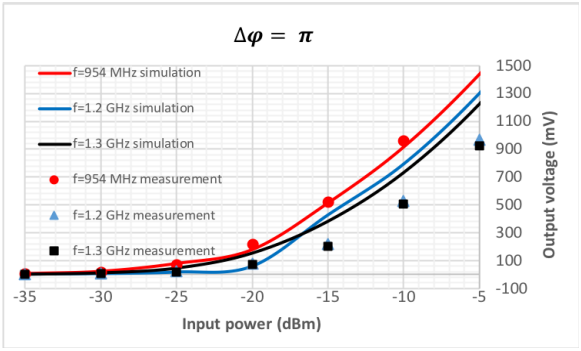

Fig.15: *Measured and simulated results with SG in case* $\Delta\varphi = \pi$.

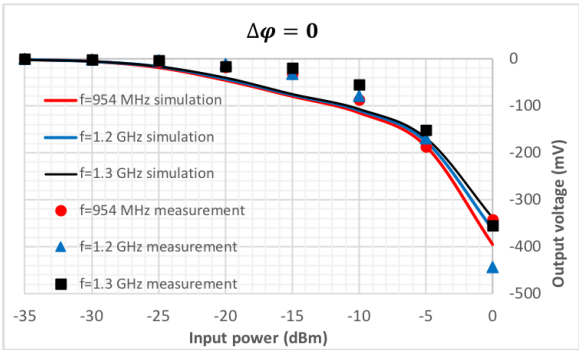

Fig.16: *Measured and simulated results with SG in case* $\Delta\varphi = 0$.

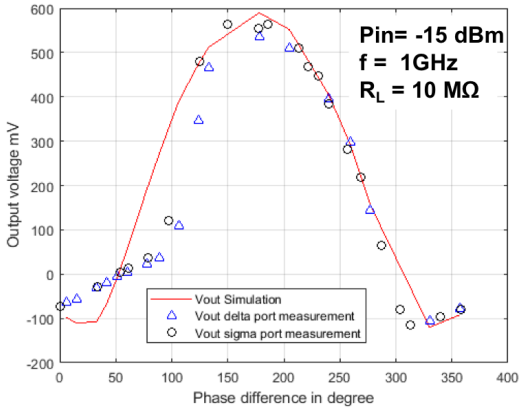

Fig.17: *Measured and simulated the effect of phase difference in 3-stage DTMOS CCR with floating sub-circuits.*

effect depending on different values of $\Delta\varphi$ in 3-stage DTMOS CCR with floating sub-circuit. The output voltages are measured at a level of –15 dBm, 1 GHz, and 10 MΩ loads. In the figure, triangle points and circle points present the measured data when SG are connected to the Δ port and the Σ port of the hybrid coupler, respectively. As shown in the figure, the measurement results in the two cases are similar and quite fit with a simulation curve.

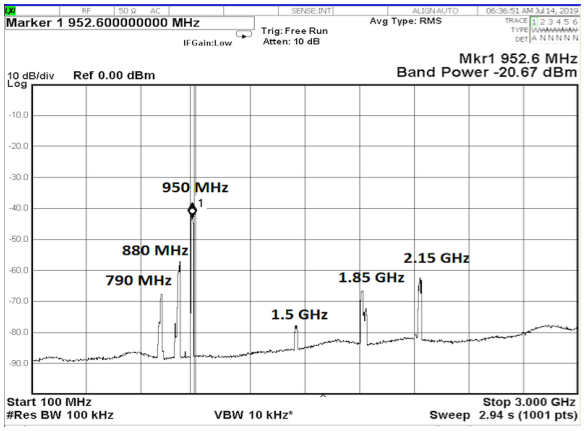

Fig.18: *Spectrum of signals at measurement positions.*

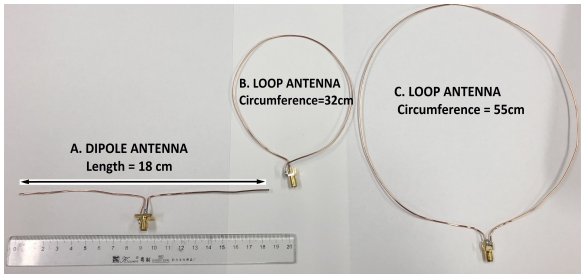

Fig.19: *Antennas used for measurements.*

5. RF ENERGY HARVESTING FROM ENVIRONMENT

Measurement is established in a laboratory room of The University of Electro-communication, Tokyo. The ambient RF signals at the measurement position measured by using a signal analyzer Agilent CXA N900A and a dipole antenna CANDOX 44Sa21. Fig. 18 shows the spectrum in a frequency range from 100 MHz to 3 GHz. At a bandwidth of 20 MHz, the band power of the signal at the 950 MHz band is –20.7 dBm, resulting in the signal being the strongest signal at the measurement place. The 950 MHz band signal corresponds to the 4 LTE downlink signal. The measurement set up is shown in Fig. 11.

In the first measurement, three antennas shown in Fig. 19 are used to receive RF signals in the environment. Antenna A is a dipole antenna, while antennas B and C are loop antennas. The antennas are designed to harvest signals at 545 MHz, 830 MHz, and 950 MHz bands, respectively. The length of the dipole antenna A is 18 cm which is equivalent to a half-wavelength at 830 MHz. The loop antennas B and C have lengths 32 cm and 55 cm which correspond to the wavelengths at 950 MHz and 545 MHz, respectively. These antennas have different resonant frequencies and polarizations, therefore, by using these antennas in the measurement, the phase difference effect is checked with various conditions.

Table 2 shows the measurement results. From the

Table 2: *Output voltage measurement results with signal from the environment.*

Antenna	V_{DC} when $\Delta\varphi = \pi$	V_{DC} when $\Delta\varphi = 0$
A	130 mV	−12 mV
B	124 mV	−18 mV
C	12 mV	−4 mV

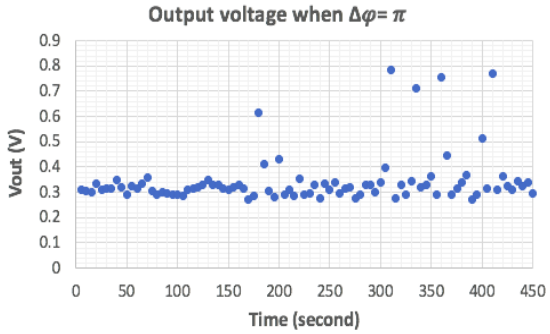

Fig.20: *Measured output voltage in the environment at 100 kΩ when $\Delta\varphi = \pi$.*

table, with respect to all antenna types, the output voltages are positive and reach the highest absolute value when $\Delta\varphi = \pi$. When $\Delta\varphi = 0$, the output voltages are negative and have small absolute values. These measurement results demonstrate that with different type and polarization of antennas, the effect of phase difference on the output of the rectifier shows an agreement with the theory proposed in Section 3.

In the next measurement, the matching circuit at 950 MHz is attached to the rectifier board to evaluate the performance of the proposed RFEH system. A 14.3 cm wired dipole antenna with length equivalent to 0.45 of the wavelength at 950 MHz is utilized. Because levels of RF signal in the environment continuously change, to evaluate the performance of the RFEH system, the output voltage is measured every second and automatically stored in a computer.

Fig. 20 presents measured output voltage at 100 kΩ load when $\Delta\varphi = \pi$. The output voltage is measured over 450 seconds. As shown in the figure, the output voltages, in this case, are positive and the average value is 0.3 V, which is equivalent to 0.9 μW DC output power received. The results indicate that at –20.7 dBm input power for the LTE signal, the proposed RFEH system can obtain 10.6 % PCE. The measurement results show the efficient performance of the proposed RFEH system when harvesting RF signals in the ambient environment.

Fig. 21 shows measured output voltage at 100 kΩ load when $\Delta\varphi = 0$. Here, all the output voltages measured over 450 seconds are negative with an average level of –50 mV. This result shows the effect of phase difference when the system harvests the real RF signal in the environment.

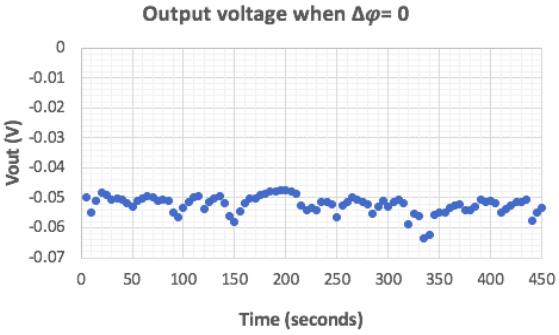

Fig.21: *Measured output voltage in the environment at 100 kΩ when $\Delta\varphi = 0$.*

6. CONCLUSION

This paper proposed the application of DTMOS to CCR with floating sub-circuits based on 65 nm SOTB CMOS technology. The designed system generated over 1 V DC voltage at –14 dBm input power, whereas the PCE reached 48 % at –10 dBm input power. With an ambient LTE signal at level of –20.7 dBm, the proposed RFEH generated 0.9 μW DC power which is equivalent to a PCE of 10.6 %. The effect of phase difference between the two RF input signals on the output voltage of the rectifier was shown. The simulations and measurements indicated that the output voltage becomes maximum at the phase difference of π and decreased when the phase difference differs from π. Therefore, one of the requirements in designing the RFEH system using CCR is to ensure two paired RF signals supplying to the rectifier are differential signals.

ACKNOWLEDGMENT

This work was supported by JST-CREST Grant Number JPMJCR16Q1. It was also supported by VLSI Design and Education center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc. and Cadence Design Systems, Mentor Inc.

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