A Low-voltage Current-mode Electronically Controllable Four-quadrant Zero/Span Circuit

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ABSTRACT

A low-voltage four-quadrant current-mode current-controllable zero/span circuit is discussed. The circuit structure is based on CMOS current follower with adjustable current gain and 4 diodes, without any resistor. The proposed circuit has advantages in such low-voltage architecture biased with as low as ±0.5 V power supply. It can generate four-quadrant outputs, without any changing circuit topology. Additionally, its zero and span levels can be independently tuned by electronic method though relative bias currents, where a low-offset output current can be achieved. The total power consumption is approximately 10 μW, much lower than a traditional one. Simulation results are shown; it offers good performance of the proposed circuit as depicted. Furthermore, to extend the workability of the proposed zero/span circuit, its application in current-mode Wheatstone bridge to alleviate the offset problem is described.

Keywords: Zero/span Circuit, Low-Voltage, Current-Mode, Four-Quadrant, Electronically Controllable

1. INTRODUCTION

A zero/span circuit is a useful and important circuit for an electrical engineering scope; for instance, it can be found in instrumentation systems to amplify or adjust/reduce the offset of a signal obtained from a sensor before interfacing with a computer or microcontroller. The linear equation is equivalent to $y = mx \pm c$. This is seen to be equivalent to the zero/span equation used in an instrumentation circuit, where m is the slope of the linear equation or span/amplifying and c is the zero or offset level in the instrumentation circuit. From literature review, we found that the zero/span circuits have been rarely reported. Traditionally, the zero/span circuit in the structure of an op-amp operating in voltage-mode was proposed [1]. It has disadvantages in such due to it using many active and passive elements and lack of electronic tunability. The last issue is necessary for modern controls via a microcontroller/ microprocessor, including an automatic control system. Subsequently, the zero/span circuit using current differencing transconductance amplifiers (CDTAs) working in transconductance-mode [2] was proposed; the important drawback of this structure is that it cannot be electronically tuned. Additionally, its circuit architecture is based on the use of many active and passive elements, as well. Especially, both op-amp and CDTA-based zero/span circuits cannot operate in low supply voltage configuration.

As is well known, the current-mode circuits offer many advantages superior to the traditional voltage-mode circuits, for example, larger dynamic range, lower power consumption, easier suitability for summing and higher speed [3–7]. Consequently, the current-mode technique is suited for applications in the low-voltage and low-power circuits to obtain high performance long-life battery-powered portable electronic equipment.

The current follower (CF) is a versatile active building block. It has been developed in many applications [8–13] due to the simplicity and flexibility of its circuit implementation. Recently, the zero/span circuit using multiple-output CF was presented [14]. Its features are that it operates in current-mode and uses minimal active components as only one multiple-output adjustable current gain CF cooperating with 4 diodes. In addition, it achieves electronic controllability and independent control between zero and span term. Unfortunately, its power consumption is in a milli Watt range, which is very high for a modern circuit. Moreover, its internal circuit configuration is based on bipolar junction transistors (BJTs) operating with power supply voltages as high as ±3 V.

This article aims to introduce a developed zero/span circuit, developed from the nonlinear circuit application as current limiters [15–17], using CMOS technology to reduce power supply voltages, and achieve a low power consumption. It offers 4 quadrant outputs to be used for any signal condition. The independently electronic control of zero and span levels can also be accomplished. Additionally, an application example of the proposed zero/span circuit in the current-mode Wheatstone bridge circuit is in-

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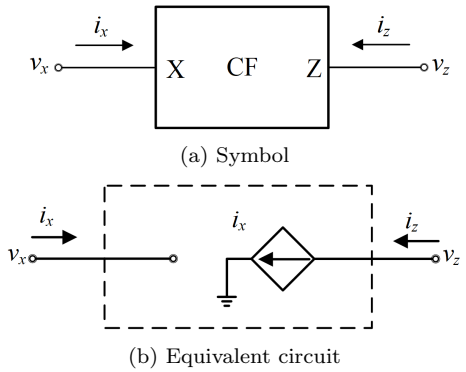

Fig.1: *Current Follower.*

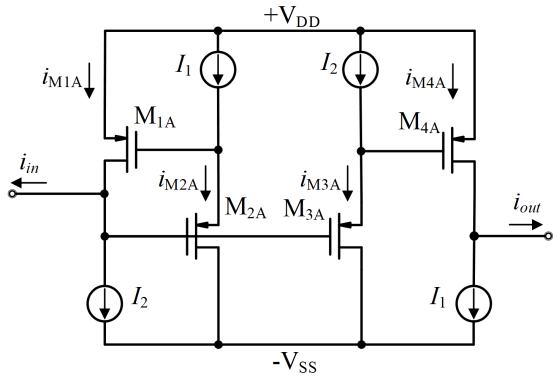

Fig.2: *Internal structure of CF with adjustable current gain.*

cluded to confirm the good performance to reduce the offset problem in an instrumentation system.

The paper is organized as follows; Section 2 is circuit description; the concepts of current follower and current amplifier including the multiple-output current follower with adjustable again are introduced. The proposed low-voltage current-mode electronically controllable zero/span circuit is presented in Section 3. The effect of non-ideal operation of the proposed zero/span circuit due to the CF and diodes is explained in Section 4. Section 5 is depicted to show simulation results for verifying the different performances of the proposed zero/span circuit. An example application of the proposed zero/span circuit in the current-mode Wheatstone bridge is disclosed in Section 6 to show the practical workability in the instrumentation system. The last section, Section 7, is conclusion to summarize the proposed work.

2. CIRCUIT DESCRIPTION

As explained earlier in Section 1, the active building block to be used in this work is the multiple-output CF with adjustable current gain. This section explains the basic concept of CF and subsequently the internal structure of multiple-output CF with adjustable current gain.

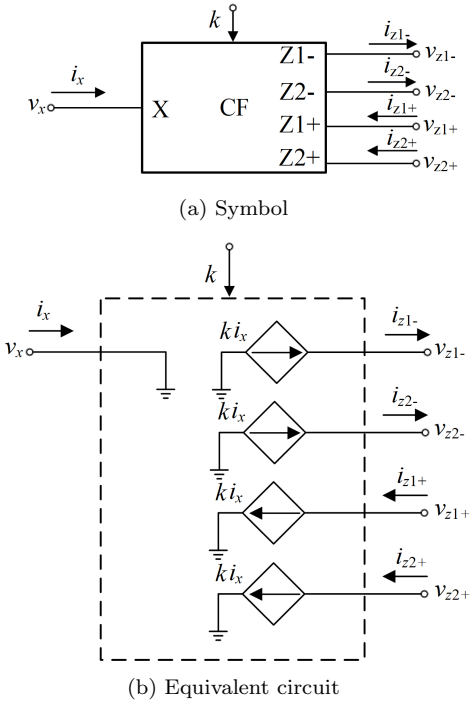

Fig.3: *Multiple-output CF with adjustable current gain.*

2.1 Basic Concept of Current Follower

The symbol and equivalent circuit of the CF are respectively shown in Figs. 1(a) and 1(b), the characteristic equation of a CF is

$$\begin{bmatrix} v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \end{bmatrix} [i_x] \tag{1}$$

2.2 Principle of Current Follower with Adjustable Current Gain

Fig. 2 shows a current follower with adjustable current gain whose output current gain can be electronically adjusted [18]; all transistors operate in the strong inversion region. The currents i_{in} and i_{out} are the input current and output current, respectively. I_1 and I_2 are external bias currents. Applying translinear principle [19] to this circuit, it can be derived to be

$$i_{M1A} \cdot i_{M2A} = i_{M3A} \cdot i_{M4A} \tag{2}$$

Due to $i_{M1A} = i_{in} + I_2$, $i_{M2A} = I_1$, $i_{M3A} = I_2$ and $i_{M4A} = i_{out} + I_1$, Eq. (2) is changed to

$$(i_{in} + I_2) \cdot I_1 = I_2 \cdot (i_{out} + I_1) \tag{3}$$

Distributing Eq. (3), it would be

$$(i_{in} \cdot I_1) + (I_1 \cdot I_2) = (I_2 \cdot i_{out}) + (I_1 \cdot I_2) \tag{4}$$

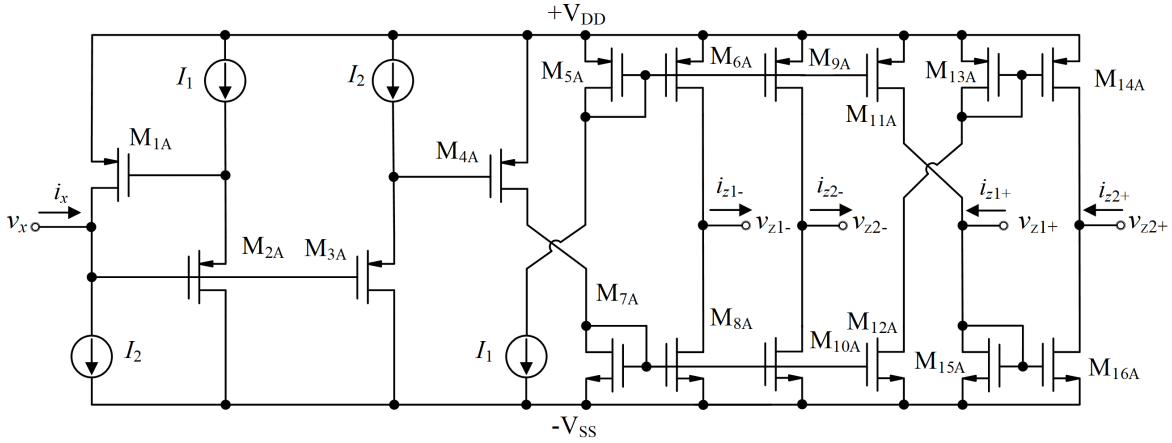

Fig.4: *Internal implementation of low-voltage multiple-output CF with adjustable current gain.*

Then, Eq. (4) can be changed to

$$i_{in} \cdot I_1 = I_2 \cdot i_{out} \tag{5}$$

From Eq. (5), it can be concluded that

$$i_{out} = k \cdot i_{in} \tag{6}$$

where k is the ratio of external bias current I_1/I_2. From Eq. (6), it is shown that the output current of the adjustable current gain current follower can be electronically controlled by adjusting the ratio of current source I_1 and I_2.

2.3 Multiple-output Electronically Adjustable Current Gain Current Follower

The symbol and equivalent circuit of multi-output CF with adjustable current gain are respectively shown in Figs. 3(a) and 3(b). It can be found that it can comprise several output ports (Z1–, Z2–, Z1+ and Z2+). The internal implementation of the low-voltage multiple-output CF with adjustable current gain is depicted in Fig. 4, consisting of the current amplifier; $M_{1A} - M_{4A}$ to amplify output current by ratio of I_1 and I_2. The CMOS $M_{5A} - M_{10A}$ transistors are a group of current mirrors, offering currents at Z1– and Z2–. Simultaneously, the function of CMOS $M_{11A} - M_{16A}$ is to copy current Z– and subsequently invert currents to port Z1+ and Z2+. By consideration of internal construction in Fig. 4, we can find that it provides a high impedance at port Z– and Z+ due to the effect of current mirrors. The characteristic equation of multi-output CF with adjustable current gain is

$$\begin{bmatrix} v_x \\ i_{z1-} \\ i_{z2-} \\ i_{z1+} \\ i_{z2+} \end{bmatrix} = \begin{bmatrix} 0 \\ -k \\ -k \\ +k \\ +k \end{bmatrix} [i_x] \tag{7}$$

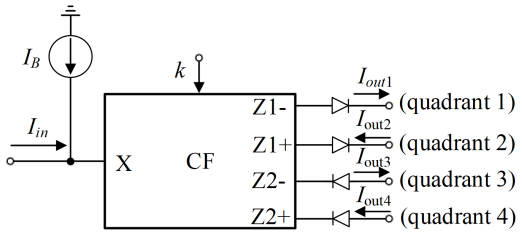

Fig.5: *Proposed low-voltage four-quadrant electronically controllable zero/span circuit.*

3. THE PROPOSED LOW-VOLTAGE FOUR-QUADRANT CURRENT-MODE ELECTRONICALLY CONTROLLABLE ZERO /SPAN CIRCUIT

The proposed low-voltage four-quadrant electronically controllable zero/span circuit is shown in Fig. 5. The circuit description consists of only 1 low-voltage multiple-output CF with adjustable current gain and 4 diodes. It offers output currents with four-quadrant characteristic of zero/span function, where I_{out1}, I_{out2}, I_{out3} and I_{out4} are output current terminals of zero/span function in quadrants 1, 2, 3 and 4, respectively. It obtains output current equations as

$$\text{Quadrature 1:} \quad I_{out1} = +kI_{in} \pm I_B \tag{8}$$

$$\text{Quadrature 2:} \quad I_{out2} = +kI_{in} \pm I_B \tag{9}$$

$$\text{Quadrature 3:} \quad I_{out3} = -kI_{in} \pm I_B \tag{10}$$

$$\text{Quadrature 4:} \quad I_{out4} = -kI_{in} \pm I_B \tag{11}$$

From Eqs. (8)–(11), it can be seen that the zero/offset level of the output currents of the proposed circuit can be electronically controlled by external current source I_B, whereas the span/slope level can also be electronically adjusted by gain k or ratio of current sources I_1 and I_2.

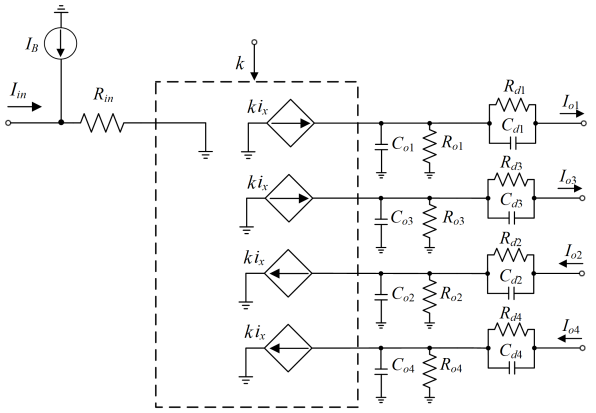

Fig.6: *Proposed low-voltage four-quadrant electronically controllable zero/span circuit with non-ideal consideration.*

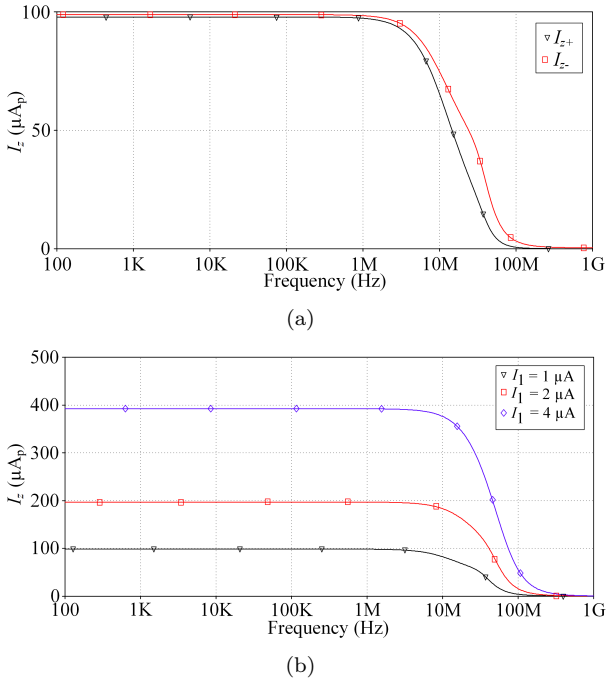

Fig.7: *Frequency response of the multiple-output CF.*

4. NON-IDEAL ANALYSIS

The effects of non-ideal consideration of multi-output CF and diodes are analyzed in this section. Fig. 6 shows the electrical notation of the proposed zero/span circuit with non-ideal effect, giving R_{in} is internal resistance of the multi-output CF, R_{o1-4} and C_{o1-4} are external resistance and capacitance of the multi-output CF in quadrant 1, 2, 3 and 4, respectively. The parameters R_{d1-4} and C_{d1-4} are respectively internal resistances and internal capacitances of diodes number 1, 2, 3, and 4. The non-ideal characteristics of output currents; I_{o1}, I_{o2}, I_{o3} and I_{o4} can be depicted to be

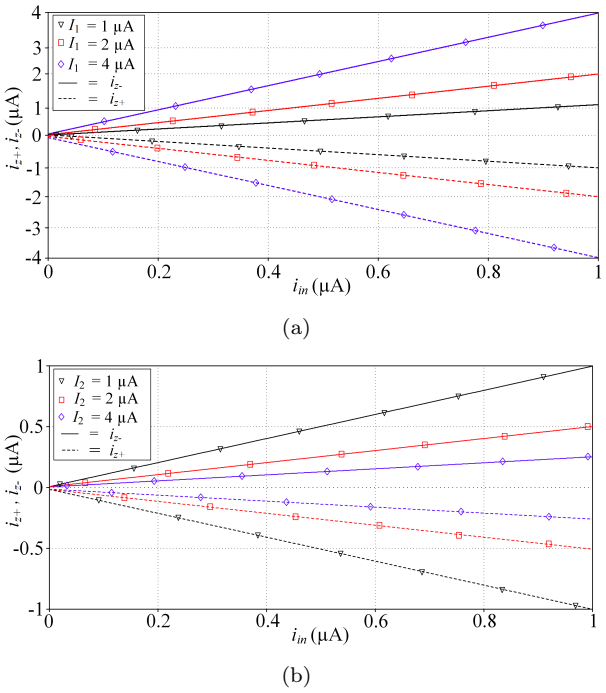

Fig.8: *Results of varying DC gain of multiple-output CF.*

Quadrant 1:

$$i_{o1} = +k\left[\frac{R_{o1}\left(sC_{d1}R_{d1}+1\right)}{sC_{d1}R_{d1}R_{o1}+sC_{o1}R_{d1}+R_{o1}+R_{d1}}\right]I_{in} \pm I_B \quad (12)$$

Quadrant 2:

$$i_{o2} = +k\left[\frac{R_{o2}\left(sC_{d2}R_{d2}+1\right)}{sC_{d2}R_{d2}R_{o2}+sC_{o2}R_{d2}+R_{o2}+R_{d2}}\right]I_{in} \pm I_B \quad (13)$$

Quadrant 3:

$$i_{o3} = -k\left[\frac{R_{o3}\left(sC_{d3}R_{d3}+1\right)}{sC_{d3}R_{d3}R_{o3}+sC_{o3}R_{d3}+R_{o3}+R_{d3}}\right]I_{in} \pm I_B \quad (14)$$

Quadrant 4:

$$i_{o4} = -k\left[\frac{R_{o4}\left(sC_{d4}R_{d4}+1\right)}{sC_{d4}R_{d4}R_{o4}+sC_{o4}R_{d4}+R_{o4}+R_{d4}}\right]I_{in} \pm I_B \quad (15)$$

From Eqs. (12)–(15), it can be seen that each output current port depends on the non-ideal parameters stemming from both the active building block CF and the diodes. These non-ideal errors affect magnitudes of the output currents. Consequently, in practical circuit implementation, accurate design of the devices must be considered to obtain the mentioned errors as low as possible, for example, using high-performance current mirrors and using high-efficiency diodes (HEDs).

5. SIMULATION RESULTS

To validate several performances of the proposed zero/span circuit. It is primarily verified by PSpice

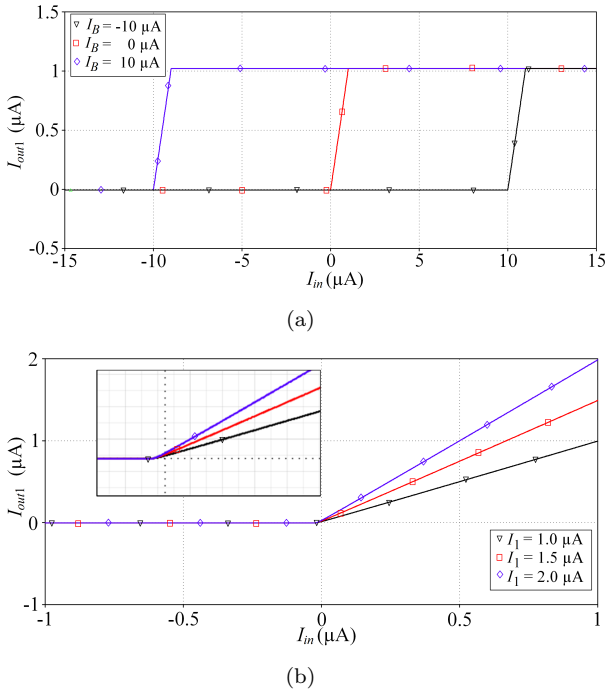

Fig.9: *Adjustable zero (I_B) and span (I_1) of proposed circuit in quadrant 1.*

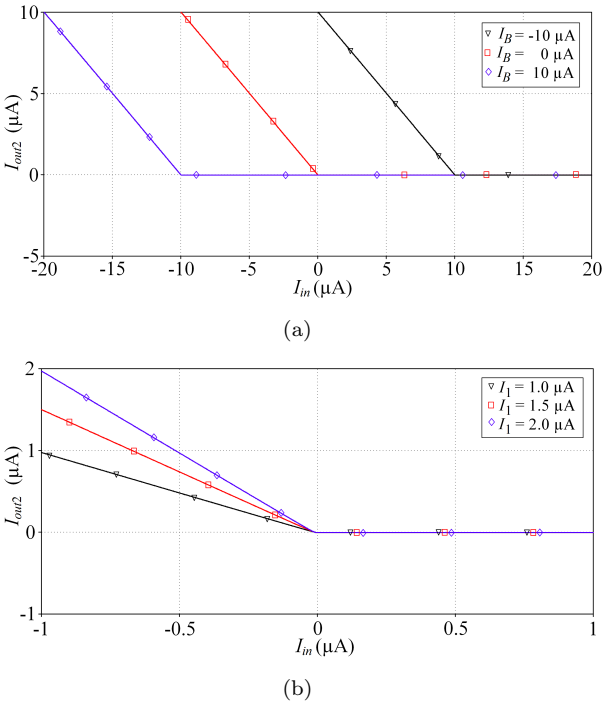

Fig.10: *Adjustable zero (I_B) and span (I_1) of proposed circuit in quadrant 2.*

Table 1: *Performance comparison of zero/span circuits.*

Parameters	Article	
	[14]	Proposed circuit
Power supply	±3 V	±0.5 V
Power consumption	1.35 mW	10.9 µW
Implemented technology	BJT	CMOS
Number of BJT/CMOS	56	16
Cut off frequency	17 MHz	11.85 MHz
Minimum input current	1 mA	200 µA

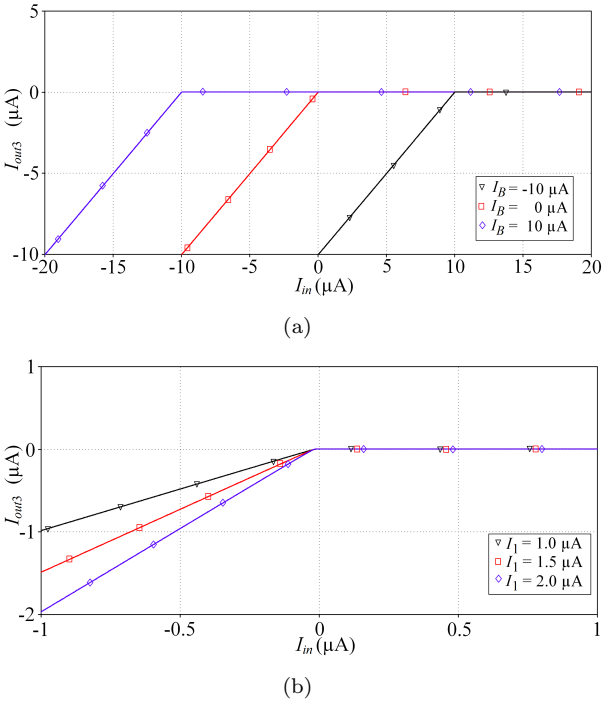

Fig.11: *Adjustable zero (I_B) and span (I_1) of proposed circuit in quadrant 3.*

simulation program using CMOS internal structure of the multiple-output CF in Fig. 4 based on TSMC 0.35 μm model described in the Appendix, including 1N4148 diode model, where the aspect ratio W:L of $M_{1A} - M_{16A}$ transistors is 56:0.7 μm. The bias currents were set to be $I_1 = I_2 = 1\mu$A, supply voltages $+V_{DD}$ and $-V_{SS}$ are ±0.5 V.

Firstly, the performances of the multiple-output electronically adjustable current gain CF are surveyed as shown in Figs. 7–8. Fig. 7(a) is the frequency response of current transfer of the multiple-output CF with adjustable current gain, with input current of 100μA_p; it can be found that its cut-off frequency is approximately 11.85 MHz. Fig. 7(b) is frequency response by adjusting I_1 to be 1 μA, 2 μA and 4 μA. In addition, Fig. 8 is the result of current gain adjustability of the CF at port Z– and Z+ by adjusting I_1 to be 1 μA ($m = k = 1$), 2 μA ($m = k = 2$), and 4 μA ($m = k = 4$) (Fig. 8(a)). Additionally, Fig. 8(b) depicts the frequency response of adjustable current gain by adjusting I_2 to be 1 μA ($m = k = 1$), 2 μA ($m = k = 0.5$) and 4 μA ($m = k = 0.25$).

Subsequently, several performances of the proposed zero/span circuit in Fig. 5 are demonstrated

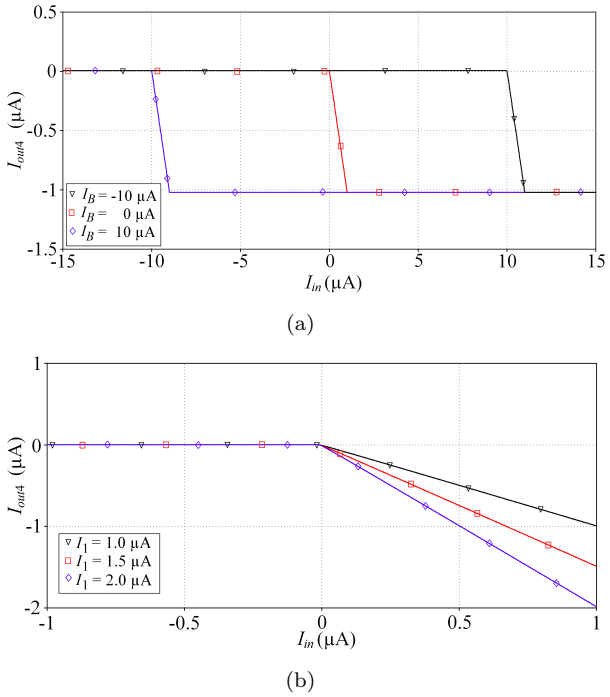

Fig.12: *Adjustable zero (I_B) and span (I_1) of proposed circuit in quadrant 4.*

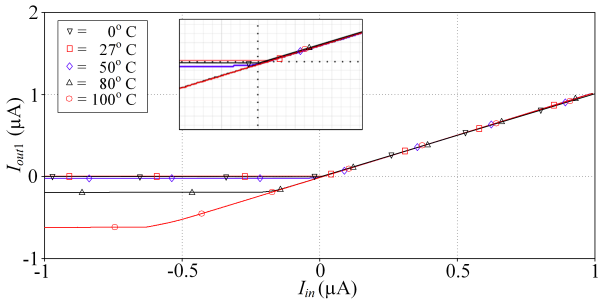

Fig.13: *Effect of temperature variation at the quadrant 1 output current.*

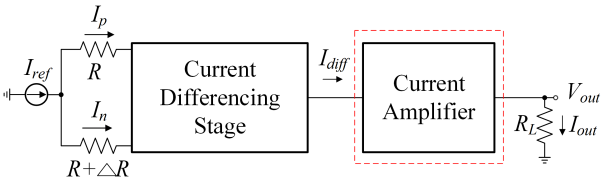

Fig.14: *A traditional current-mode Wheatstone bridge circuit [20].*

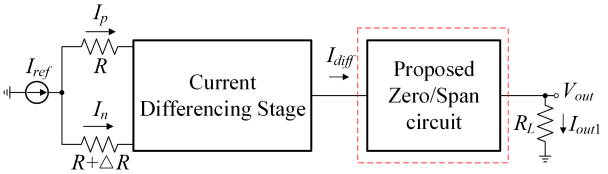

Fig.15: *Application of zero/span circuit in current-mode Wheatstone bridge circuit.*

via 1N4148 diode model. All of the results can be found in Figs. 9–13. Firstly, Figs. 9(a), 10(a), 11(a) and 12(a) are the results of adjusting different zero or offset levels, respectively obtained from quadrants 1 to 4 by tuning current I_B to be –10 μA, 0 μA and 10 μA. It is confirmed that the zero level can be electronically controlled by the bias current, I_B. Additionally, the span or gain can also be electronically adjusted by I_1 and/or I_2 as respectively shown in Figs. 9(b), 10(b), 11(b) and 12(b) for quadrants 1 to 4, where $I_1 = 1$ μA ($k = 1$), $I_1 = 1.5$ μA ($k = 1.5$) and $I_1 = 2$ μA ($k = 2$); I_2 is fixed for all quadrants. The last result, Fig. 13 is the output current deviation obtained from quadrant 1 due to temperature variation for 0°C, 20°C, 50°C, 80°C and 100°C by setting $I_1 = I_2 = 1$ μA. It is shown that during the operating temperature range (not more than 50°C), the output current is free from temperature variations.

The comparison for different performances between the proposed circuit and recently previous zero/span circuits [14] is shown in Table 1. It can be seen that the proposed zero/span circuit uses less power supply voltages, offers much less power consumption, and employs a lower number of transistors.

6. EXAMPLE OF APPLICATION

In this section, an example application of the proposed zero/span circuit is shown to extend the practical usability in instrumentation systems. The current-mode Wheatstone bridge circuit in Fig. 14 is used to detect small resistance changes [20–21]. It can be found being used for sensing several physical variations such as temperature, weight etc. [1, 22]. It consists of a current differencing stage and an amplifier. From this circuit, the output current of the current differencing stage (I_{diff}) is amplified before being sent to the output of the current-mode Wheatstone bridge circuit. It should be noted here that, in practice, the output current of current the differencing stage comprises not only the desired signal, but also the DC offset. Thus, the traditional current amplifier cannot eliminate the DC offset level but amplifies this DC offset; the zero/span circuit is entirely needed in this case. It can be substituted at the current amplifier stage, as depicted in Fig. 15.

Considering the circuit in Fig. 14, the current differencing (I_{diff}) consists of the desired signal and the DC offset, I_{offset} equal to

$$I_{diff} = I_p - I_n = \frac{I_{ref}\Delta R}{2R + \Delta R} + I_{offset} \qquad (16)$$

where $\Delta R << R$ for a practical application. Eq. (16) can be reduced to

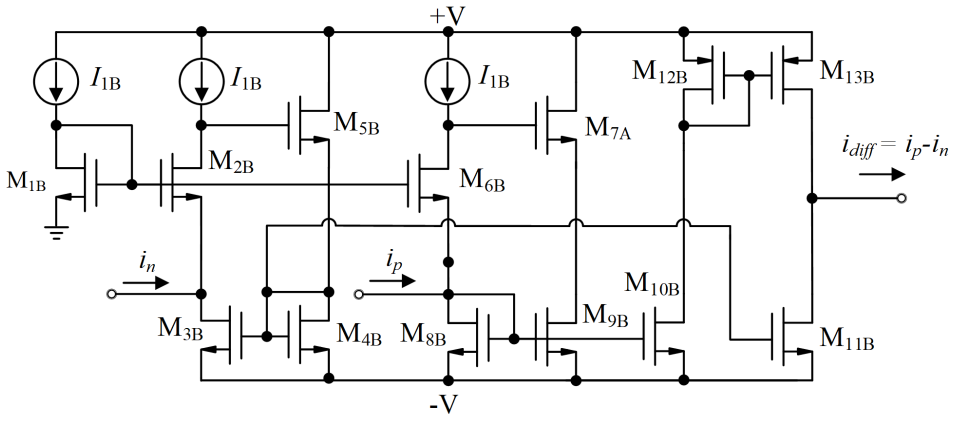

Fig.16: *Internal structure of current differencing stage in Figs. 14 and 15 [23].*

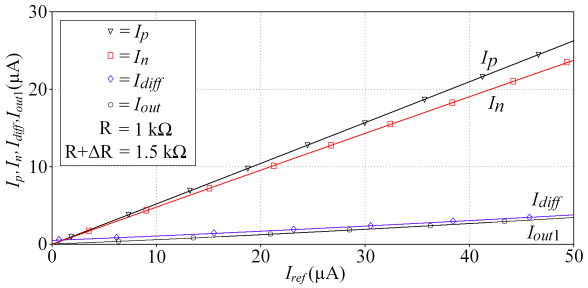

Fig.17: *Output of current differencing and I_{out1}.*

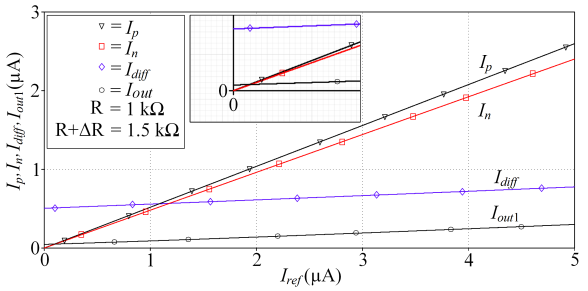

Fig.18: *Enlarged Fig. 17 to underline offset of output currents.*

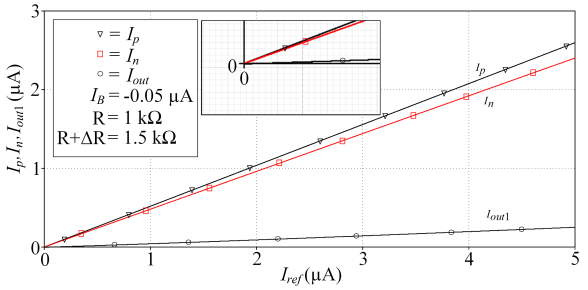

Fig.19: *Reducing offset current offset by adjusting I_B.*

$$I_{diff} = \frac{I_{ref}\Delta R}{2R} + I_{offset} \tag{17}$$

Giving G as the gain of the current amplifier in Fig. 14, the output I_{out} will be

$$I_{diff} = \pm G\left(\frac{I_{ref}\Delta R}{2R} + I_{offset}\right) \tag{18}$$

From Eq. (18), it can be clearly seen that not only is the desired signal amplified, but the DC offset is also amplified. As more DC offset level is given at the output, more errors in the mentioned instrumentation systems are inevitable.

Meanwhile, considering the current-mode Wheatstone bridge circuit using the proposed zero/span circuit replacing the conventional current amplifier as shown in Fig. 15, the output current in quadrant 1 can be easily depicted by using Eqs. (8)–(11) to be

$$I_{out1} = \pm k\left(\frac{I_{ref}\Delta R}{2R} + I_{offset}\right) \pm I_B \tag{19}$$

From Eq. (19), it is easy to conclude that the DC offset is also amplified by gain k of the zero/span circuit. However, using the proposed zero/span circuit can alleviate the DC offset problem, since it can be compensated by adjusting I_B.

To confirm the described performance, the current differencing stage in Fig. 16 [23] cooperating with the proposed zero/span circuit, as shown in Fig. 15, was also simulated using TSMC 0.35μm and aspect ratio $W : L$ of $M_{1B} - M_{13B}$ of 20:1 μm, current sources I_{1B} were set to be 20 μA, supply voltages $+V$ and $-V$ are $\pm$1.25 V. The current I_1 and I_2 in the zero/span circuit are set to 10 μA, $I_B = 0$ μA, Fig. 17 is the result of the current differencing output and output current of the zero/span circuit, where $R = 1$ $k\Omega$, $R+\Delta R = 1.5k\Omega$ and $I_{ref} = 50\mu$A. To enlarge the DC current offset levels obtained from the current differencing stage (I_{diff}) and the proposed circuit (I_{out1}), Fig. 18 is shown. It can be found that both signals contain a large offset.

This problem can be improved by adjusting the

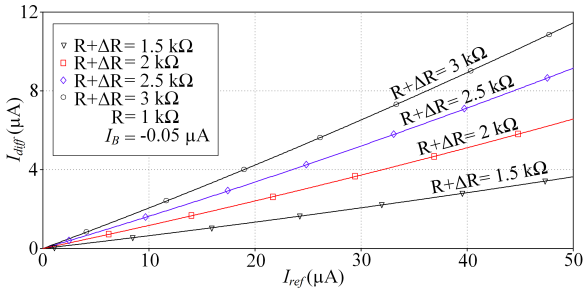

Fig.20: *Output current I_{out1} for different R.*

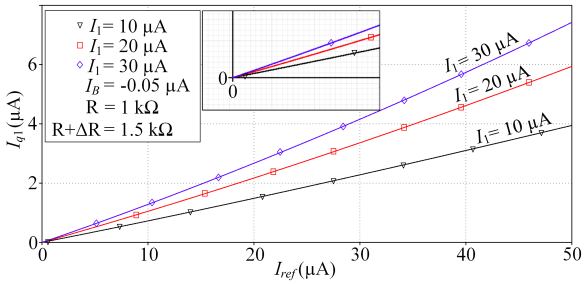

Fig.21: *Output current of proposed zero/span circuit in Fig. 15 for different I_1.*

current source I_B to be –0.05 μA, with the result in Fig. 19 achieved. It is clearly seen that the output current of the current-mode Wheatstone bridge circuit using the proposed zero/span circuit has no DC offset, as desired.

The changing resistance of $R + \Delta R$ is depicted in Fig. 20 by setting $R + \Delta R$ = 1.5 $k\Omega$, 2 kΩ, 2.5 kΩ, and 3 kΩ. Furthermore, Fig. 21 shows performance of adjusting span or gain obtained from the output of the zero/span circuit for different current source I_1 of I_1 = 10 μA, 20 μA and 30 μA. It is seen that the current-mode Wheatstone bridge architecture using the proposed zero/span circuit enjoys electronic tuneability with no DC offset, achieved from available compensation.

7. CONCLUSION

In this paper, the new low-voltage four-quadrant current-mode zero/span circuit is proposed. The advantages of the proposed circuit are that zero (offset) and span (gain) can be independently controlled by electronic method via related currents and it can operate with a low supply voltage as low as ±0.5 V, compared to a recently developed zero/span circuit, operating at ±3 V. Moreover, the proposed circuit employs only 1 multiple-output electronically adjustable current gain current follower, as an active building block, cooperating with 4 diodes. It can simultaneously provide 4 quadrant zero and span functions at 4 output currents. The total power consumption is as low as approximately 10.9 μW. The simulation results confirmed the theoretical analysis. The example application in the current-mode Wheatstone bridge circuit also confirmed the performance of a practical application of the proposed zero/span circuit. Consequently, the proposed circuit is suited for use in portable instrumentation circuits/systems.

APPENDIX

CMOS MODEL
N_TSMC35 NMOS LEVEL=3 TOX=7.9E-9 NSUB=1E17
+GAMMA=0.5827871 PHI=0.7 VTO=0.5445549 DELTA=0
+UO=436.256147 ETA=0 THETA=0.1749684
+KP=2.055786E-4 VMAX=8.309444E4 KAPPA=0.2574081
+RSH=0.0559398 NFS=1E12 TPG=1 XJ=3E-7
+LD=3.162278E-11 WD=7.046724E-8 CGDO=2.82E-10
+CGSO=2.82E-10 CGBO=1E-10 CJ=1E-3 PB=0.9758533
+MJ=0.3448504 CJSW=3.777852E-10 MJSW=0.3508721
TSMC35 PMOS LEVEL=3 TOX=7.9E-9 NSUB=1E17
+GAMMA=0.4083894 PHI=0.7 VTO=-0.7140674 DELTA=0
+UO=212.2319801 ETA=9.999762e-4 THETA=0.2020774
+KP=6.733755E-5 VMAX=1.181551E5 KAPPA=1.5
+RSH=30.0712458 NFS=1E12 TPG=-1 XJ=2E-7
+LD=5.000001E-13 WD=1.249872E-7 CGDO=3.09E-10
+CGSO=3.09E-10 CGBO=1E-10 CJ=1.419508E-3
+PB=0.8152753 MJ=0.5 CJSW=4.813504E-10 MJSW=0.5

DIODE D1N4148 MODEL
+D (Is=2.682n N=1.836 Rs=.5664 Ikf=44.17m Xti=3
+Eg=1.11 Cjo=4p M=.3333 Vj=.5 Fc=.5 Isr=1.565n
+Nr=2 Bv=100 Ibv=100u Tt=11.54n)

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