Switched-Capacitor-Based Preamplifier Circuit for Hearing Aid Devices

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ABSTRACT

This paper presents a switched-capacitor design for a preamplifier hearing aid circuit. The proposed circuit achieves good linearity in a wide range of amplification frequencies compared to the conventional type. The total power consumption of the proposed preamplifier is 1.093 μW. Undesirable outband high-frequency noise can be removed by the proposed preamplifier circuit before connecting to the analog-to-digital converter (ADC) in the front-end of the hearing aid. The third harmonic distortion ratio HD_3 is 44.39 dB while the figure of merit (FOM) is considerably better than the conventional type. The front-end of the hearing aid device occupies less area, is more energy efficient, and exhibits a noise level of 13 nV/$\sqrt{\text{Hz}}$. The design simulation is performed using LTspice software.

Keywords: Charge Amplifier, Analog Variable Gain Amplifier, Switched-Capacitor, Miller Multiplication Effect, Rerouting, LTspice

1. INTRODUCTION

Hearing loss is one of the most common human impairments. About 30 million people worldwide are currently suffering from hearing loss. Depending on the severity of hearing loss, most of these patients can be helped by a hearing aid device that just amplifies sounds coming into the ear [1]. The normal range of acoustic frequency is from 20 Hz to 20 kHz. With recent advances in VLSI technology, hearing aid devices are improving in terms of performance, size, and power dissipation. When dealing with a signal, the hearing aid can be divided into three types: analog, control, and digital. The front systematic structure of a hearing aid includes a preamplifier and an ADC for transferring an analog signal to digital data which is then further processed by a digital signal processor [2]. Fig. 1 shows the signal path of the hearing aid system. All signal processing elements, including the microphone, variable gain amplifier, ADC, digital signal processor, and digital-to-analog converter (DAC) are used to construct a hearing aid system [2]. Kuntzman *et al.* designed a superior piezoelectric microphone that mimics the auditory system of the Ormia ochracea [3]. With this device, sound pressure can be detected by using different orientations in the hearing aid. This type of piezoelectric microphone generates particularly low-level signals, and hence it is necessary to design a circuit that can amplify the signals efficiently [4]. The first signaling element is the preamplifier, consisting of a charge amplifier (CA) and an analog variable gain amplifier (AVGA). The preamplifier employs a universal opamp in the conventional and proposed switched-capacitor-based design, and compares them using LTspice simulation. The switched-capacitor technique consumes less area in the preamplifier circuit, exhibits low power dissipation, and less distortion.

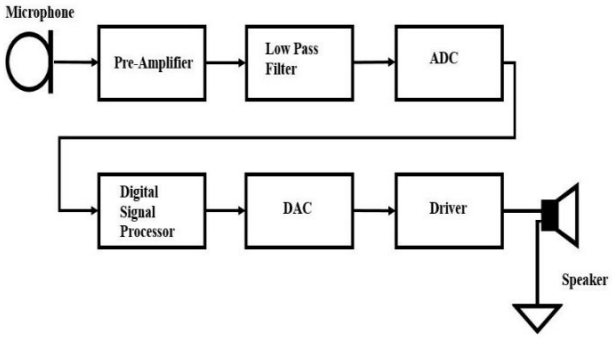

Fig. 1: *Signal flow path of the hearing aid.*

The analog switched-capacitor-based preamplifier topology proposed in this paper can provide good linearity in a large bandwidth range and wide gain variations, while achieving a hearing gain of 90 dB (desired specification). The paper is organized as follows: Section 2 describes the CA used in conventional and proposed hearing aid devices. Section 3 presents the design of an AVGA. Section 4 provides details of the preamplifier circuit (CA and AVGA), electrical interface, and frequency response. Finally, Sections 5 and 6 present the simulation results and conclusion along with a summary of the research.

Manuscript received on November 17, 2019 ; revised on September 22, 2020 ; accepted on November 25, 2020. This paper was recommended by Associate Editor Surachoke Thanapitak.

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Digital Object Identifier 10.37936/ecti-eec.2021192.225580

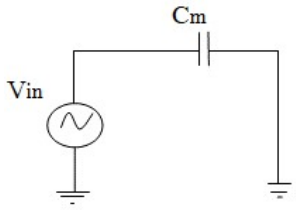


Fig. 2: *Circuit diagram of a piezoelectric based microphone.*

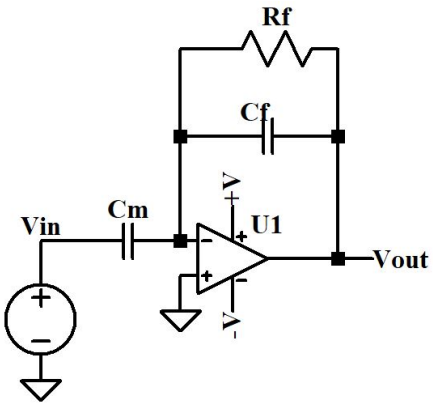


Fig. 3: *Circuit diagram of a charge amplifier.*

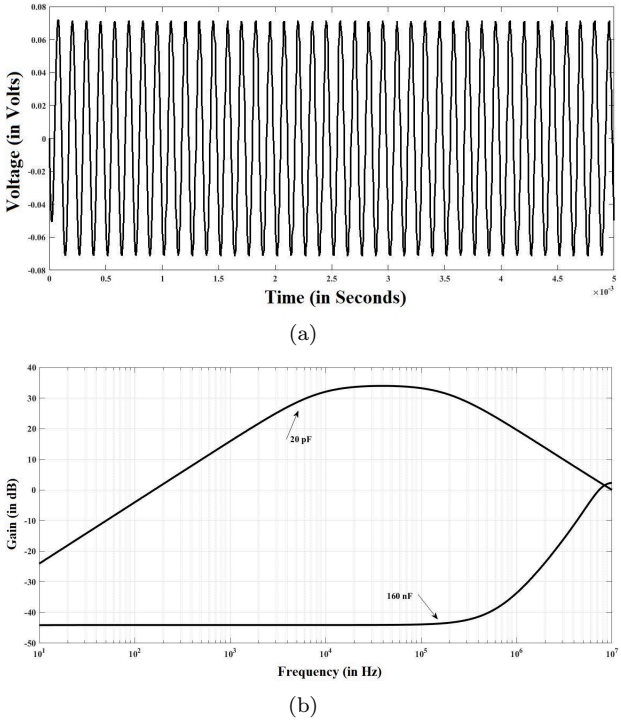


Fig. 4: *(a) Transient simulation result and (b) AC response of the conventional CA.*

2. CHARGE AMPLIFIER (CA)

2.1 Conventional CA

For human speech, a microphone requires good linearity in the frequency range of 400 Hz to 8 kHz [4]. Due to the linearity and circuit-to-circuit interfacing, piezoelectric sensors maintain high impedance, and therefore, a mega ohm range and microphone sensitivity of 10 μV/Pa at 8 kHz are selected for this study [4, 5].

A piezoelectric sensor produces a charge, based on the pressure applied which can be modeled as shown in Fig. 2. A charge amplifier (CA) is a special I/V converter intended for sensors with an electric charge proportional to a physical quantity and a predominantly capacitive equivalent output impedance such as piezoelectric sensors [5]. The CA is the intermediate stage between the sensor signal and subsequent processing blocks to convert the charge signal into a voltage signal [11]. Here, the CA is modeled using a voltage source and the capacitance of the microphone in series with it (Fig. 3) where C_m is the capacitance of the microphone, R_f is the bias resistor, and C_f provides the desired response. The frequency range of a human being is commonly stated to extend from 20 Hz to 20 kHz, whereas human speech is mostly constrained to between 250 Hz and 5 kHz. Assuming the microphone capacitance is 1 nF (neglecting loss and noise), the transfer function of the charge amplifier is given by

$$A_1(s) = -\frac{sR_fC_m}{1+sR_fC_f} \tag{1}$$

According to Eq. (1), the output voltage is inversely proportional to the value of the feedback capacitor. In the proposed design, the cut-off frequency for the CA is selected as 100 Hz or 8 kHz, determined by the values of R_f and C_f. For a general operational amplifier (opamp), the maximum value of the feedback resistor R_f is 1 MΩ due to the loading effect. The C_f can be calculated as 160 nF or 20 pF. The amplitude of the electrical speech signal from the microphone to CA will peak at a maximum of 5 mV. In LTspice, the power supply for the opamp U1 is $\pm$5 V (specification of opamp U1 in LTspice; Inst Name: U1, SpiceModel: level.2, Value2: Avol=1Meg GBW=10Meg Slew=10Meg, SpiceLine: ilimit=20m rail=0 Vos=0 phimargin=45, SpiceLine2: en=0 enk=0 in=0 ink=0 Rin=500Meg). The schematic of conventional CA is shown in Fig. 3, while Figs. 4(a) and 4(b) show the transient and frequency responses of a conventional CA for C_f 160 nF or 20 pF. It can be observed that the voltage gain is negative from 100 Hz to 20 kHz of 160 nF and positive for 20 pF. Hence, a feedback capacitor C_f of 20 pF is selected. In both cases, the response exhibits nonlinearity from 100 Hz to 10 kHz. At this range, it would behave like a high pass filter. Alternatively, due to the high value of R_f in the mega ohm range, i.e., the circuit generates a response noise within audible range frequencies. The voltage gain has a

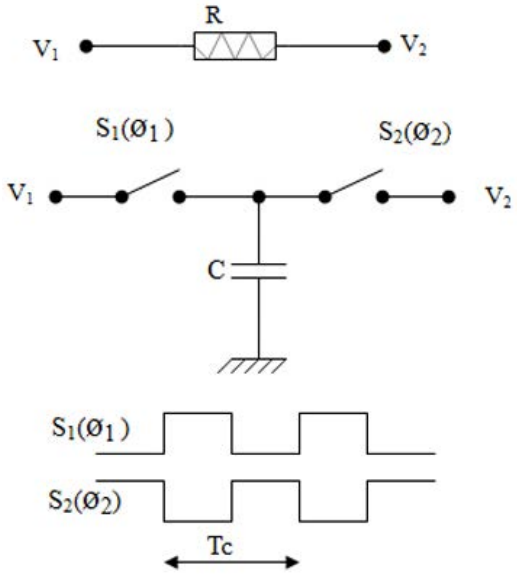


Fig. 5: *Switched-capacitor-based resistor.*

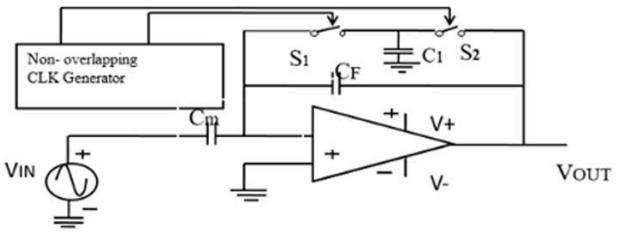


Fig. 6: *Circuit diagram of the proposed-1 charge amplifier.*

30 dB ranging from 7.5 kHz to 212 kHz (bandwidth). Furthermore, with an increase in frequency (beyond 250 kHz), an internal parasitic capacitance effect arises, and the gain decreases. Hence, the total response is a band pass filter structure which is a combination of low pass and high pass. Again, from the response (Fig. 4(b)), the system is observed to have good stability due to a phase margin (PM) of 89°. From an analog integrated circuit design perspective, the charge amplifier is limited by the large value of the feedback capacitor since it consumes a substantial fraction of the die area [11]. In the application of a biomedical device such as a front-end hearing aid, the charge amplifier is constructed using a switched-capacitor-based feedback resistor.

2.2 Switched-Capacitor-Based CA

The realization in Fig. 5, R is replaced with a "switched-capacitor" network. Here, capacitor C is periodically switched between two nodes with voltages of V_1 and V_2. In each cycle, C stores a charge of $Q_1 = CV_1$ while connected to V_1 and $Q_2 = CV_2$ while tied to V_2. For example, $V_1 > V_2$, C_2 absorbs the charge from V_1 and delivers it to V_2, thus approximating a resistor. It can also be observed that the equivalent value of this resistor decreases as the switching is performed at a higher rate because the amount of charge delivered from V_1 to V_2 per unit of time increases [6]. For the design specification, considering the conventional CA shown in Fig. 6, the feedback resistor R_f is replaced by a grounded capacitor C_1 together with two MOS transistors acting as switches. The two MOS switches in the figure are driven by non-overlapping two-phase clocks. The clock frequency f_{clk} ($f_{clk} = 1/T_{clk}$) is much higher than that of the input signal V_{in}. During clock phase ϕ_1, C_1 is connected to the virtual ground input of the opamp. The capacitor C_1 discharges and its previous charge q_{c1} is transferred to C_f.

During each clock period T_{clk}, the amount of charge $q_{c1} = C_1V_0$ is extracted from the output source and supplied to the capacitor C_f. Thus, the average current flowing between the output node and the virtual ground node is

$$I_{avg} = \frac{C_0V_0}{T_{clk}} = C_0V_0f_{clk} \tag{2}$$

If the T_{clk} is sufficiently short, this process may be almost continuous, defining an equivalent resistance R_f that is in effect present between the node output and virtual ground.

$$R_f = \frac{V_0}{I_{avg}} \tag{3}$$

Applying Eqs. (2) and (3), $C_1 = T_{clk}/R_f$, the maximum feedback resistor of the opamp is 1 MΩ. For biomedical circuits, the selected clock frequency is 10 kHz, with the value of C_1 at 100 pF. The time constant of the integrator circuit would be 20 μs ($T_{clk}C_f/C_1$). Fig. 7(a) gives the schematic of the proposed charge amplifier. It can be observed that the proposed charge amplifier has gained 34 dB from 10 Hz to 20 kHz with a PM of 91°, as depicted in Fig. 7(b). It can be suggested that the phase margin, in this case, is greater than that of the conventional charge amplifier. In order to have a good stable system, the PM should be greater than 45°, otherwise, it would take too long to maintain system stability. If the phase margin is greater or equal to 90°, the poles of the system transfer function would be on a real axis, i.e., no oscillation [6, 7].

2.3 Proposed-2 CA

In the schematic of Fig. 7, the switches are replaced with MOS transistors, driven by the appropriate clock signals. A clock feedthrough effect arises, thereby degrading the circuit performance. Every ground node creates a parasitic capacitance in a circuit. Both clock feedthrough and parasitic capacitance effects can be reduced by using rerouting interconnections. Fig. 8(a) shows the proposed-2

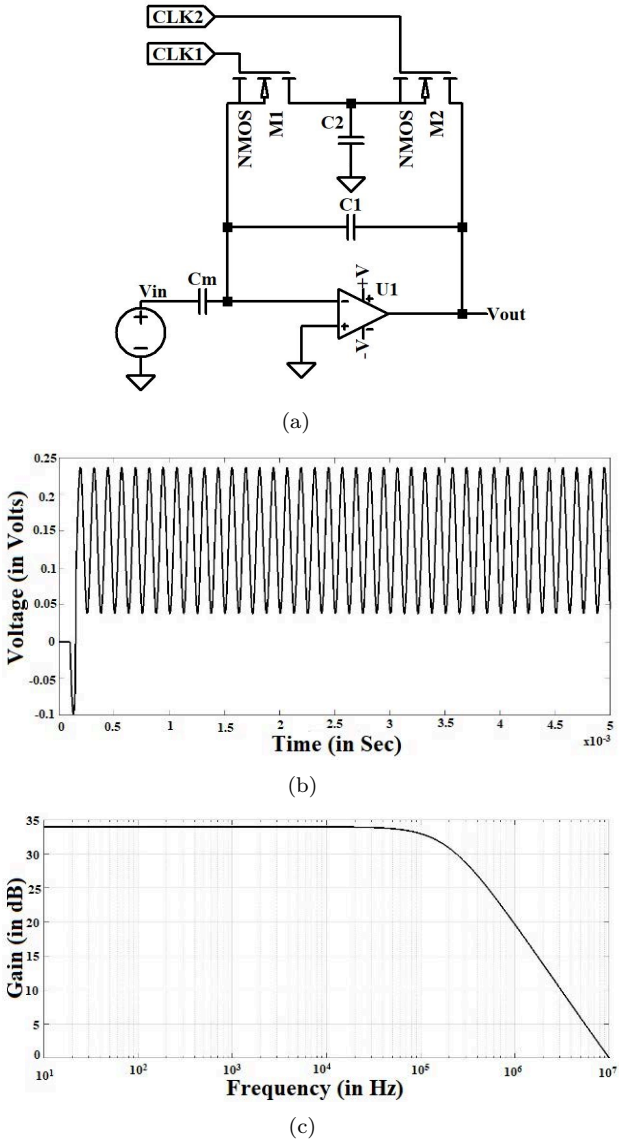


Fig. 7: *(a) Schematic diagram, (b) transient simulation result, and (c) AC response of the proposed-1 CA.*

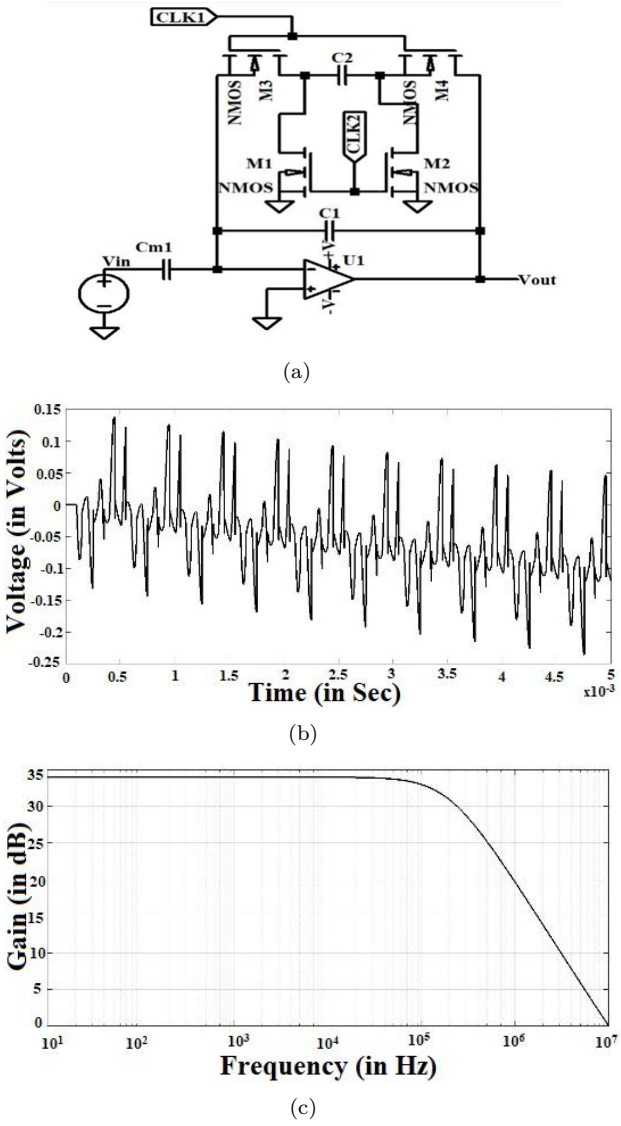


Fig. 8: *(a) Schematic diagram, (b) transient simulation result, and (c) AC response of the proposed-2 CA.*

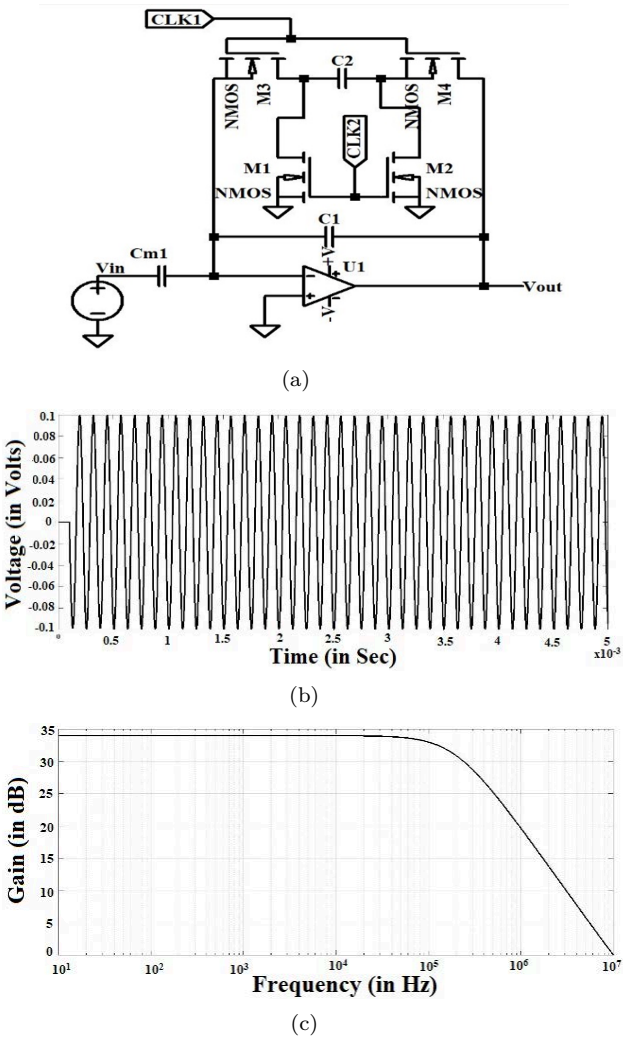
charge amplifier with a parasitic insensitive switched-capacitor integrator circuit. Prior to clock phase-1, the two plates of capacitor C_2 are discharged to signal ground, thereby removing all charges in the parasitic capacitors. By selecting the value of C_2 100 pF, the simulation does not give the proper output due to the Miller multiplication effect (see Fig. 8(b)) [7]. The proposed-2 amplifier shows the 33 dB at 8 kHz (Fig. 8(c)), which is the same as the proposed-1, but with a PM of $-90°$, resulting in system instability. During clock phase 1, C_2 is tied between two floating nodes. Compared to the proposed-1 charge amplifier, the new value of the capacitor is selected in the femtofarad (fF) range for the proposed-2 amplifier using the Miller capacitance effect. The new modified value C_2 of 10 fF with the proposed-2 charge amplifier is shown in Fig. 9. The voltage gain is 34 dB from 10 Hz to 40 kHz and the peak amplitude of the output signal 100 mV. Here, the PM is again 91°.

Table 1 presents a summary of the conventional, proposed-1, proposed-2, and modified proposed-2 charge amplifiers. The modified proposed-2 CA is suitable (less sensitive to parasitic effects) for designing an analog front-end hearing aid.

3. ANALOG VARIABLE GAIN AMPLIFIER (AVGA)

3.1 Conventional AVGA

As one of the critical components in a medical electronic system, the variable gain amplifier (VGA) is widely used to provide a fixed output power for different input signals to improve the dynamic range



(a)

(b)

(c)

Fig. 9: *(a) Schematic diagram, (b) transient simulation result, and (c) AC response of the modified proposed-2 CA.*

Table 1: *Conventional and proposed CA.*

Circuit	Input	Output	Cut-off frequency	Gain
Conventional	2 mV	70 mV	8 kHz	34 dB
Proposed-1	2 mV	240 mV	8 kHz	33 dB
Proposed-2	2 mV	N/A	8 kHz	33 dB
Modified Proposed-2	2 mV	100 mV	8 kHz	34 dB

[8]. The input signal amplitude always varies in a hearing aid. A variable gain is needed to compensate for differences in input signal levels. If the circuit nonlinearities are high, it is hard for the patient to understand conversational speech. High accuracy and good linearity are essential for analog front-end hearing devices. Therefore, the dB-linear characteristic must be achieved. In order to achieve an accurate dB-linear characteristic, the implementation of an exponential function is required. For an

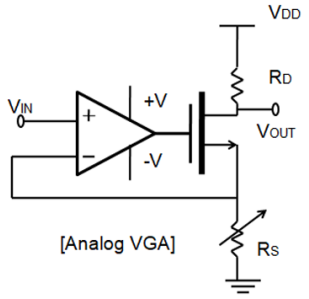


Fig. 10: *Circuit diagram of the conventional AVGA.*

accurate dB-linear, the VGA can be designed using bipolar technology since its intrinsic exponential characteristic is better implemented in a standard CMOS technology due to the low cost of integration [9, 12]. An analog variable gain amplifier (AVGA) is used to adjust the gain of the signal received from the charge amplifier. The last stage of an analog front aid hearing amplifier is the analog-to-digital converter (ADC). The VGA adjusts the signal level to an appropriate power level for the ADC. Here the VGA is a combination of the opamp and variable common source/emitter with a degeneration circuit as in Fig. 10 [12]. In the second stage of the VGA, a common emitter configuration is selected due to its better dB-linear characteristic. The value of R_C (R_1 in Fig. 11) is chosen as 5 kΩ. To improve the dynamic range, an emitter resistor R_E (R_2 in Fig. 11) ranging from 5 mΩ to 10 Ω is selected. The overall gain of VGA will therefore be

$$A_{\mathrm{VGA}} = \frac{(g_m R_C A)\,(1 + g_m R_E A)}{(1 + g_m R_E A)\,(1 + 2 g_m R_E A)} \qquad (4)$$

where g_m is the transconductance of the transistor, while A is the open-loop gain of the opamp. The schematic and simulation of a conventional amplifier are illustrated in Fig. 11. From the response, it can be observed that the output signal drastically attenuates, making it difficult to improve the dynamic range, while the PM is 79°. A positive voltage gain can be achieved by using the switch-capacitor-based technique.

3.2 SWITCHED-CAPACITOR-BASED AVGA (PROPOSED-1)

In the schematic of Fig. 12, resistors R_1 and R_2 are replaced using clock signals, capacitors, and two NMOS switches. The value of capacitors is selected with the help of the clock signal frequency (10 kHz), R_1 (5 kΩ), and R_2 (5 mΩ to 10Ω). The variable capacitor C_2 is used instead of the emitter resistor. The clock frequency f_{clk}, R_1, C_1 and R_2, C_2 can be represented by the following relation:

$$f_{clk} = \frac{0.159}{(R_1 C_1)} = \frac{0.159}{(R_2 C_2)} \qquad (5)$$

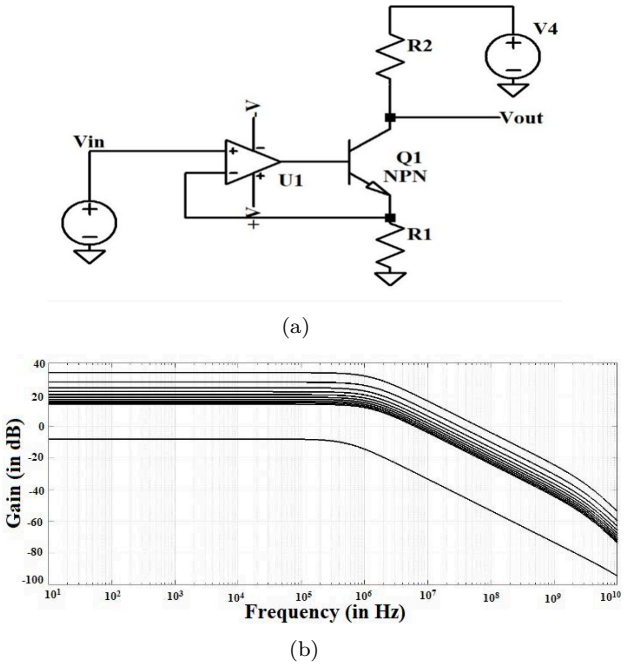


Fig. 11: *(a) Schematic diagram and (b) AC response of the conventional AVGA.*

From 10 Hz to 2 kHz, the response gain is 58 dB with a PM of 90° but this circuit is affected by parasitic capacitances.

3.3 SWITCHED-CAPACITOR-BASED AVGA (PROPOSED-2)

In the proposed-1 AVGA circuit, the stray capacitance is a combination of the switch capacitor CSW, and the top and bottom plate capacitance ($C_t + C_b$) of the capacitor. An integrated capacitor is typically constructed with polysilicon electrodes, separated by thin oxide on the IC chip. However, these parasitic values may be too large for a minimum size capacitor to accept [7]. The stray capacitance effect can be reduced by changing the capacitor position with the help of four NMOS switches and non-overlapping clock signals. Parasitic insensitive circuits make use of different configurations, preventing any parasitic capacitor charges from contributing to the useful signal [7].

During the CLK1 phase, the left plate of the capacitor connects with the voltage V_0 (collector) while the right plate is connected to the supply voltage during clock phase 2 (CLK2) as shown in Fig. 13. In this case, the PM is 91°, i.e., an improvement of 1° compared to the proposed-1 AVGA, hence, providing good stability. The maximum gain is 58 dB, the same as the proposed model. From the three types of AVGAs, the proposed-2 type is preferable for use in the preamplifier circuit.

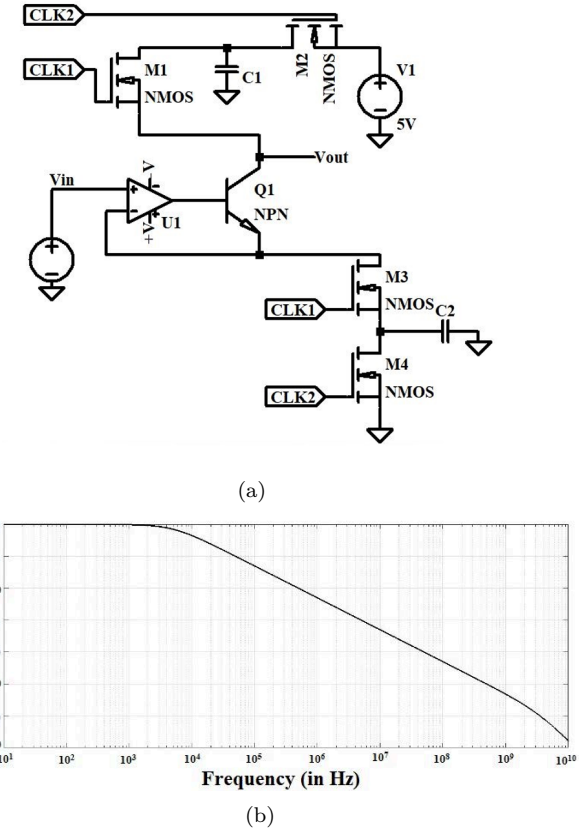


Fig. 12: *(a) Schematic diagram and (b) AC response of the switched-capacitor-based AVGA.*

4. PREAMPLIFIER CIRCUIT

4.1 Conventional Preamplifier Circuit

The preamplifier circuit consists of a variable gain amplifier with a charge amplifier. The schematic conventional preamplifier (Fig. 14(a)) has −55 dB gain, and a hearing range from 0 dB of sound pressure level (dB SPL) to 120 dB SPL. Below 0 dB SPL and above the 120 dB SPL threshold, hearing pain occurs. The hearing threshold is observed to be lowest at the middle frequency, rising at both low and high frequencies. Regular conversational speech occurs in the frequency range of 100 Hz to 10 kHz, and an amplitude range of 25 to 95 dB SPL [1, 15]. Hearing discomfort starts at 120 dB SPL while 140 dB SPL is the pain threshold. The designed hearing aid aims to cover the 120 dB dynamic range with frequencies up to 10 kHz for better hearing comfort. The response represents a combination of the high pass and low pass structure, with the harmonic noise component present in the circuit [10].

With the help of Fig. 14(b), the PM and gain also demonstrate negative values. For an audio amplifier design, the third harmonic distortion (HD_3) is used to quantify the level of harmonics and serve as a measure of system linearity [14, 15]. Modern power analyzers incorporate FFT-based algorithms to calculate HD_3

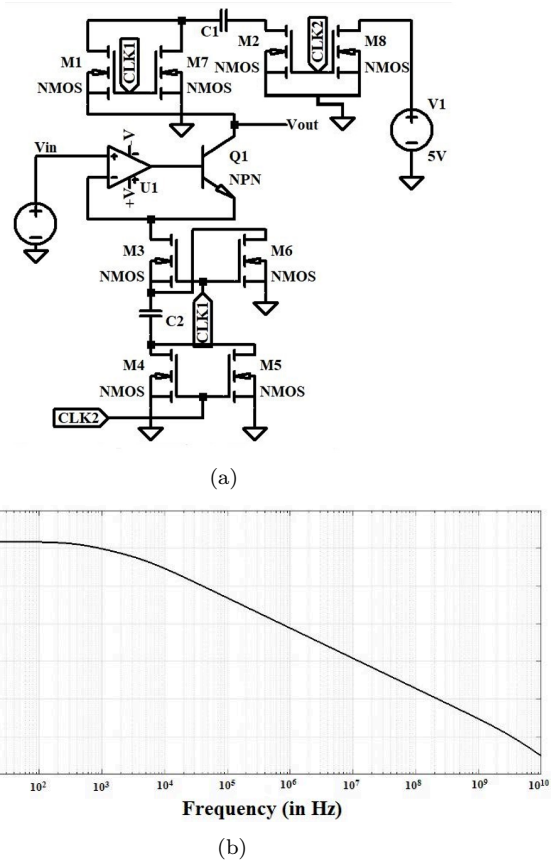


Fig. 13: *(a) Schematic diagram and (b) AC response of the proposed-2 AVGA.*

in dB. Fig. 14(c) shows the FFT analysis of a conventional preamplifier circuit, where HD_3 is followed by 31.66 dB. Furthermore, the performance of any system is limited by noise. The circuit noise consists of a combination of thermal and flicker noise. Since noise is random, it can be characterized in terms of power spectral density [13]. The input-referred noise is $7.5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ as mentioned in Fig. 14(d). The figure of merit (FOM) determines the overall system performance. Mathematically, the FOM can be defined as the ratio between the gain-bandwidth product and power consumption [6]. The maximum gain is -53 dB and bandwidth 905 Hz (Fig. 14(b)). The power consumption of the conventional circuit is 1.11 mW as shown in Fig. 14(e). The FOM of the conventional preamplifier is calculated as 1.825×10^3. From Table 2 and the foregoing discussion, it can be observed that the conventional preamplifier circuit contains more noise in the audible frequency range, and hence, is not suitable for use in a hearing device.

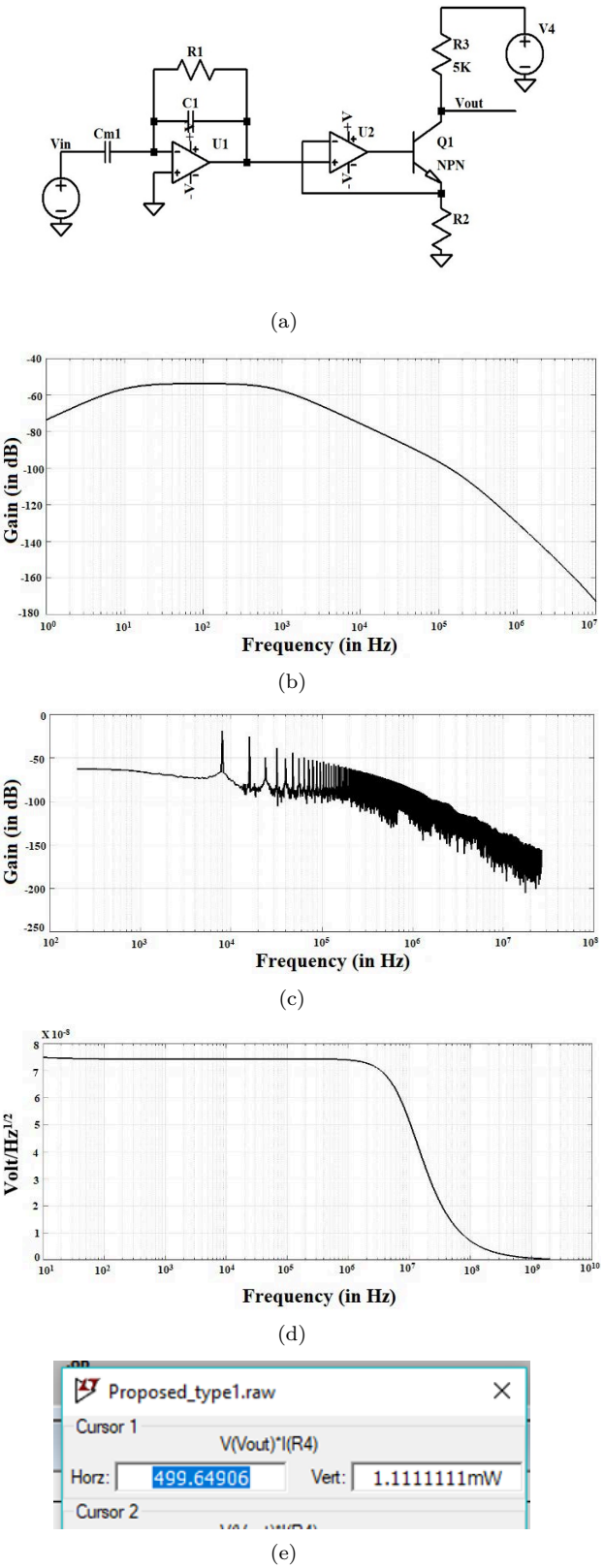


Fig. 14: *(a) Schematic diagram, (b) AC response, (c) FFT analysis, (d) noise analysis, and (e) power calculation of the conventional preamplifier.*

4.2 PROPOSED-2 SWITCHED-CAPACITOR-BASED PREAMPLIFIER CIRCUIT

The complete preamplifier circuit of the proposed-2 is depicted in Fig. 15. This circuit represents a cascading of the proposed-2 charge amplifier and

Table 2: *Conventional preamplifier circuit.*

Conventional preamplifier		Gain (dB) at 5 kHz	Gain (dB) at 8 kHz
CA		30	31
AVGA		−40	−40
Preamplifier	Theoretical	−10	−9
	Empirical	−65	−68

proposed-2 AVGA (Fig. 15 (a)). The response gain and PM are 91 dB and 132°, respectively, as shown in Fig. 15(b). Using the FFT analysis suggested in Fig. 15(c), the value of HD_3 gives 44.39 dB which is greater than the conventional preamplifier. The input-referred noise and total power dissipation are estimated as $13\,nV/\sqrt{Hz}$ and $1.093\,\mu W$, respectively (Figs. 15(d) and 15(e)). The FOM is 2.272×10^{13} using the gain-bandwidth product with power dissipation. The maximum gain is 91 dB (35481 V/V) and the bandwidth approximately 700 Hz (Fig. 15(b)), while the power dissipation of the proposed circuit is $1.093\,\mu W$ (Fig. 15(e)). In comparison to the conventional type, the proposed-2 preamplifier has far better FOM.

5. SIMULATION RESULTS AND ANALYSIS

The proposed-2 switched-capacitor-based preamplifier circuit can be designed and simulated using the LTspice simulation software. The total power consumed by the circuit is $1.093\,\mu W$. Specifically, the preamplifier achieves a gain of 61 dB at 8 kHz rather than 90 dB (theoretically) as illustrated in Table 3. The variation in gain is due to the loading effect in the next stage of the multistage amplifier circuit. There was a similar occurrence in the conventional case. The HD_3 ratio of 44.39 dB, exhibits more variation between fundamental and harmonic components. The fundamental component magnitude is much greater than the HD_3 component of the proposed-2 preamplifier circuit. The HD_3 of the conventional type is 31.66 dB less than that of proposed-2 type. The undesirable high-frequency component can be easily eliminated before applying to the ADC (Fig. 1), when using the proposed-2 preamplifier rather than the conventional circuit. From the HD_3 perspective, a low-order low pass filter may (or may not) be used between the preamplifier and ADC (Fig. 1), but a higher-order low pass filter is used in the conventional type. A higher-order filter requires more area and the circuit is difficult to design. From Fig. 14(d) and Fig. 15(d), it can be observed that the proposed-2 preamplifier exhibits more input-referred noise in comparison to the conventional type (10 Hz to 100 kHz). Since more MOSFETs are used in the proposed circuit for switching in the proposed circuit, the flicker

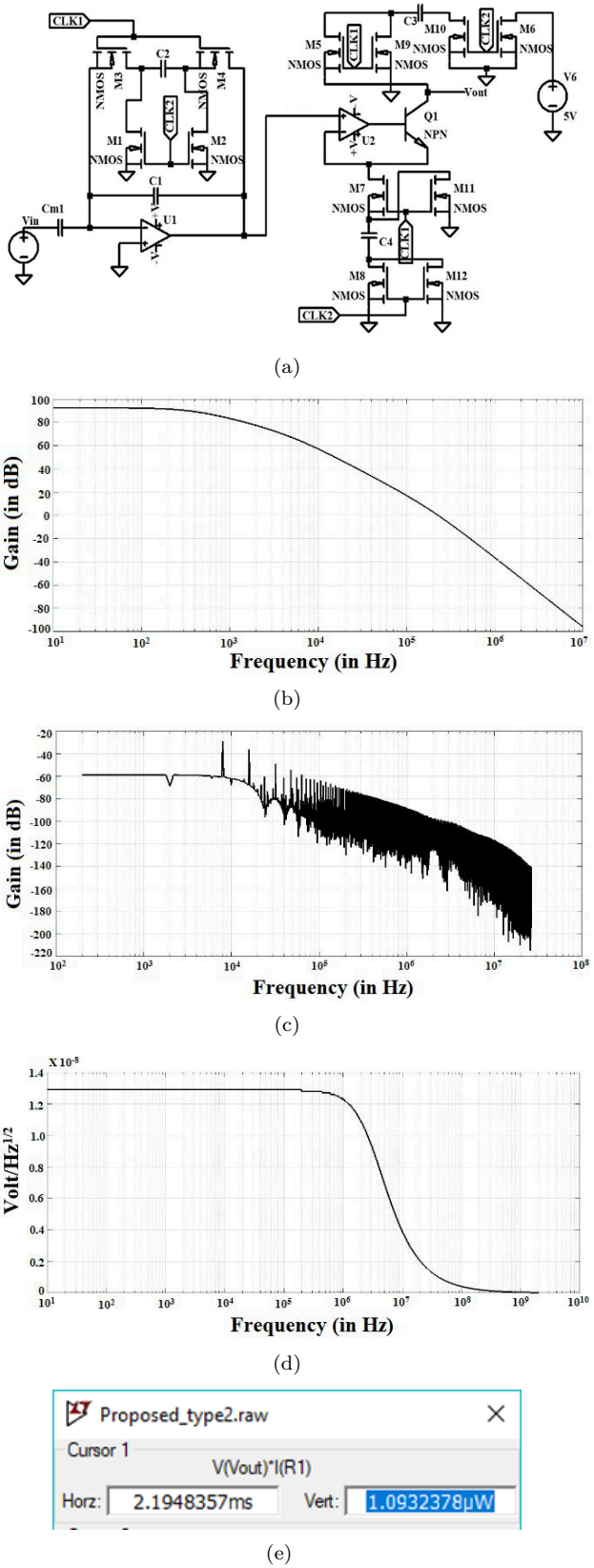


Fig. 15: *(a) Schematic diagram, (b) AC response, (c) FFT analysis, (d) noise analysis, and (e) power calculation of the proposed-2 preamplifier.*

Table 3: *Proposed-2 preamplifier circuit.*

Proposed preamplifier		Gain (dB) at 5 kHz	Gain (dB) at 8 kHz
CA		34	34
AVGA		58	56
Preamplifier	Theoretical	92	90
	Empirical	68	61

Table 4: *Performance comparison.*

Parameters	[2]	[4]	This work	
			Conventional	Proposed-2
Supply (V)	3	1.3	5	5
Power consumption (W)	216 μ	176 μ	1.11 m	1.093 μ
CMOS technology (μm)	0.35	0.13	N/A	N/A
HD_3 (dB)	N/A	N/A	31.66	44.39
FOM	N/A	N/A	1.825×10^3	2.272×10^{13}
Input-referred noise (nV/$\sqrt{\text{Hz}}$)	N/A	330	7.5	13

noise in the low-frequency region is increased [13]. Furthermore, the ideal opamp (mentioned in the specification of U1 in Section 2) is used in both types of preamplifier circuits.

6. CONCLUSION

A low power, low noise switched-capacitor-based preamplifier with a microphone is proposed in this study. The circuit can be designed to amplify low signals and attenuate loud signals while also achieving good linearity. Furthermore, the proposed system achieves an HD_3 ratio of 44.39 dB and hence, a low-order low pass filter is required between the preamplifier and ADC to improve the dynamic range of 120 dB for hearing comfort. The noise level can be minimized to the desired frequency range by the proposed-2 preamplifier circuit. The simulation results illustrate a maximum gain of 91 dB as well as a good PM of 132°. However, in contrast to the conventional type, the analog front-end switched-capacitor-based hearing aid is subject to flicker noise. Table 4 presents the advantages of this work compared to previously published studies.

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