Accurate Estimation of Power Consumption for a Binary Comparator System Using Backtracking

Mangal Deep Gupta† and **Rajeev Kumar Chauhan**, Non-members

ABSTRACT

This paper presents a binary comparator circuit design using minimum fan-in logic gates (NAND-NOR) to achieve a low power-delay product (PDP). A 2-bit binary comparator circuit is re-designed to minimize logic gate fan-in. Utilizing the concept of a 2-bit comparator, the general gate-level architecture of a comparator system is proposed for higher input operands. In this work, a backtracking model is proposed to estimate the worst-case performance in terms of delay and power for binary comparator circuits. It combines the advantages of the simulation-based method for power estimation and dynamic timing analysis (DTA) techniques for timing analysis. This work also extends to 20, 16, 14, 10, and 7-nm FinFET technology. The comparator circuits are simulated on the Pyxis Schematic tool using Mentor Graphics.

Keywords: Binary Comparator, Backtracking Model, Dynamic Timing Analysis, Power Dissipation, Power-Delay Product, FinFET, Very Large-Scale Integration

1. INTRODUCTION

A binary comparator is an essential part of the digital system. It is commonly used in various fundamental processes of computing and communication including data searching and string sorting [1]. Furthermore, it is widely used in data-intensive applications such as 3D graphics and image processing [2]. A digital comparator circuit should therefore be carefully optimized for fast and efficient electronic system development. The use of a binary comparator circuit is also observed in the arithmetic components of a random number generator (RNG) [3, 4], digital signal processor (DSP), application-oriented processors such as media processors [5], vision processors [2], etc.

The sorting operation involves various comparison steps to arrange a large amount of data in ascending or descending order and the object recognizes the algorithm by exhaustive use of the comparisons at its keypoint localization stage [6]. The proposed design of the fast and area-efficient digital comparator will significantly enhance system performance. In modern very large-scale integration (VLSI), the binary comparator circuit plays a key role in the design for testability (DFT) such as the design of the signature analyzer, parallel testing, and built-in self-test (BIST) [7] for the circuit under test (CUT). For these applications in VLSI circuits, higher operand comparator designs are now essential. Besides, comparison between two operands is a critical operation in high-speed supercomputing. Therefore, a high-speed, high fan-in comparator is required in modern VLSI design.

In the last decade, low power, high speed, and area-efficient digital comparators have been subject to numerous design challenges [8]. Power consumption and computational delay are important factors in digital circuits. High computational delay will degrade circuit performance. High power consumption adversely impacts on circuit reliability and shortens the circuit lifetime or increases the circuit failure rate [9]. Therefore, accurate estimation of power consumption and computational delay of VLSI circuits are major challenges.

For power estimation, commonly used techniques can be classified into two broad categories: simulation and non-simulation. The simulation-based method depends on a suitable set of input test vectors to identify the level of power consumption [10]. This method is more time-consuming and requires a larger memory for the simulation of complex circuits. Here, SPICE is used to precisely estimate power dissipation, but its main drawback is the large memory requirement and long simulation time [11]. Non-simulation-based study depends on input switching activity and the potential measure of input used to find the power consumption [12]. For gate-level analysis [13, 14], transition probability and signal probability are important parameters for power estimation. Although this technique is faster than simulation-based methods, it has the drawback of

Manuscript received on January 07, 2021 ; revised on February 26, 2021 ; accepted on March 29, 2021. This paper was recommended by Associate Editor Kriangkrai Sooksood.

The authors are with the Department of Electronics and Communication Engineering, Madan Mohan Malaviya University of Technology, Gorakhpur, Uttar Pradesh, India.

†Corresponding author: mangaldeepgcet@gmail.com

Digital Object Identifier 10.37936/ecti-eec.2021192.244122

providing only approximate power dissipation.

For time estimation, two techniques are used. Firstly, static time analysis (STA), in which gate and wire delays are considered in each path, and then compared against their required minimum and maximum constraint values. However, all paths in the circuit may not run continuously in the worst-case delay scenario, potentially leading to inaccurate timing. Secondly, the dynamic timing analysis (DTA) carried out through gate-level simulation depends on input test vectors. The effectiveness of the simulation depends on the quality of the test case or test vectors.

An adder circuit has been used to design a high-speed binary comparator [15]. However, it has the drawback of a slower response time. To increase the speed, a comparator with a high-speed adder was proposed by Lang *et al.* [16]. A high-performance binary comparator has also been designed [17] using the pipeline structure of dynamic CMOS logic. In this architecture, more than one clock cycle is required to complete the operation. The problem with this approach is the presence of cascading issues and a lack of synchronization. In [18], a single clock two-phase binary comparator employing a priority encoder was used to identify the first unequal bit from MSB to LSB of input data. Use of a binary comparator has been reported using a different type of priority encoder and multiplexer [19, 20]. However, comparators have high power dissipation and a greater number of transistors compared to earlier reported works.

In previous literature on binary comparator architecture, dynamic CMOS logic has been used to achieve high-performance operation. Besides delay, dynamic circuits have several drawbacks compared to the static logic design. It is not suitable for low power applications due to high data activity, synchronization problems (involving clock signals, input, and output data), cascading issues with the pipeline, and performance degradation at higher fan-in operation.

Recently, a tree-based binary comparator structure was proposed in [21–26], using the carry merge tree of the parallel prefix adder. In [27], a parallel binary comparator based on the prefix tree and XOR-XNOR circuit was proposed as a pre-encoder. This binary comparator design includes compare, pre-encoder, compression termination, and decision modules. The drawback of this architecture is its large logic gate fan-in, which increases according to the input operand size of the comparator circuit. Therefore, the computational delay and power dissipation of this architecture exponentially increase with the size of the binary comparator operands. In CMOS circuits with a high fan-in logic gate, the circuit performance degrades considerably, i.e., the circuit shows greater propagation delay and power dissipation. To improve the above architecture, the traditional CMOS-based AND-OR logic gates can be replaced with CMOS-based NAND-NOR logic.

In this work, a novel gate-level architecture for an efficient binary comparator circuit with minimum fan-in (2-input) logic gates is proposed. A 2-bit binary comparator circuit is re-designed to minimize the fan-in of logic gates. The highly efficient XOR circuit [28] is used in the proposed architecture for the first time. Utilizing the concept of a 2-bit comparator and the general gate-level architecture of a comparator system is also proposed for higher input operands. For the estimation of power consumption and propagation delay, the backtracking model is employed to identify the worst-case performance of the proposed circuit and previously reported work for the first time. The input test vector is obtained from this technique, involving the maximum possible transition at internal nodes to compute the maximum potential delay in the circuits. Utilizing this test vector, the comparator circuits are simulated using 180-nm CMOS technology for validation with previous work. This work also extends to 20, 16, 14, 10, and 7-nm FinFET technology.

2. PROPOSED BINARY COMPARATOR WITH MINIMUM FAN-IN LOGIC GATES

2.1 Basic Design Principle

The comparison of a 2-bit binary number A_1A_0 and B_1B_0 can be realized by the following Boolean expression for less 'L', greater 'G', and equal 'E' signals:

$$G = A_1P_1 + X_1A_0P_0 \tag{1}$$

$$E = X_1X_0 \tag{2}$$

$$L = \overline{E + G} \tag{3}$$

where $X = AB + \overline{A} * \overline{B}$, $P = \overline{A}B + A\overline{B}$.

For N-bit,

$$\begin{aligned} G_N = {} & A_{N-1}P_{N-1} + X_{N-1}A_{N-2}P_{N-2} \\ & + X_{N-1}X_{N-2}A_{N-3}P_{N-3} + \cdots \\ & + X_{N-1}X_{N-2}\ldots X_1A_0P_0 \end{aligned} \tag{4}$$

$$E_N = X_{N-1}X_{N-2}X_{N-3}\ldots X_0 \tag{5}$$

$$L_N = \overline{E_N + G_N} \tag{6}$$

Eqs. (1), (2), and (3) show the Boolean expression for the comparator output [27]. The gate-level architecture of the binary comparator from the above equations is shown in Fig. 1(b) and the fan-in of the logic gate used in this architecture is directly proportional to the input operand size of the binary comparator. It causes high power dissipation and large propagation delay. This circuit is designed using AND-OR logic gates, thus increasing the delay and reducing the packing density of the chip in

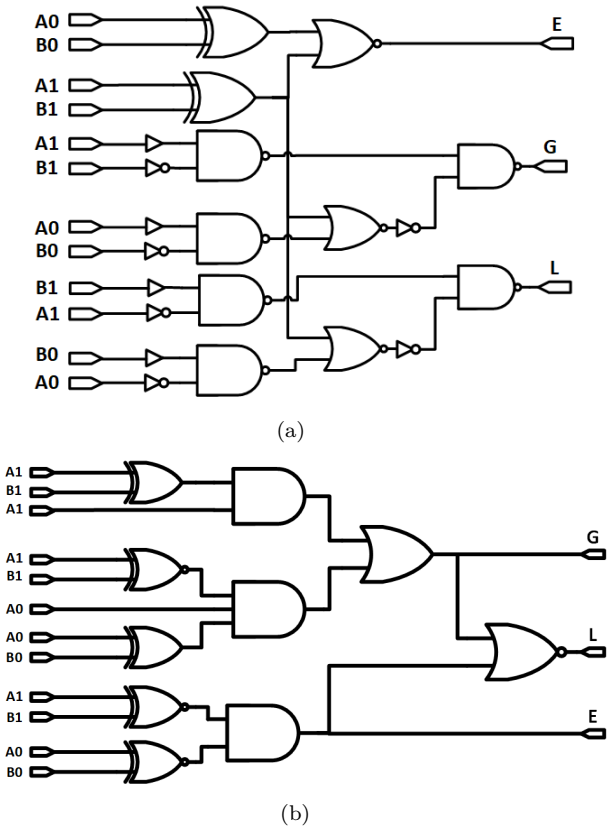


Fig. 1: *Gate-level schematics of (a) the proposed 2-bit binary comparator and (b) the previously reported 2-bit binary comparator [27].*

comparison to the CMOS-based NAND-NOR logic gate. In Eq. (3), Signal 'L' is given by $\overline{E+G}$. It is dependent on an equal and greater output signal so that the overall delay performance of the binary comparator circuit is increased.

To overcome the aforementioned drawbacks, a 2-bit elementary structure is proposed with a re-designed binary comparator, offering the independent fan-in of logic gates, free from the AND-OR logic gates that convert entire logic into NOR and NAND gates (except XOR-XNOR logic gates). The Boolean expression for the proposed 2-bit binary comparator is given by Eqs. (7), (8), and (9) for 'L', 'G', and 'E' signals:

$$E = \overline{P_1 + P_0} \tag{7}$$

$$G = \overline{\left(\overline{A_1}\overline{B_1}\right) \cdot \left(\overline{\left(\overline{A_0}\overline{B_0}\right) + P_1}\right)} \tag{8}$$

$$L = \overline{\left(\overline{A_1}B_1\right) \cdot \left(\overline{\left(\overline{A_0}B_0\right) + P_1}\right)} \tag{9}$$

Fig. 1(a) shows the proposed 2-bit binary comparator architecture with minimum fan-in (2-input) logic gate (NAND-NOR), which is designed by Eqs. (7), (8), and (9). It is generating all output independently.

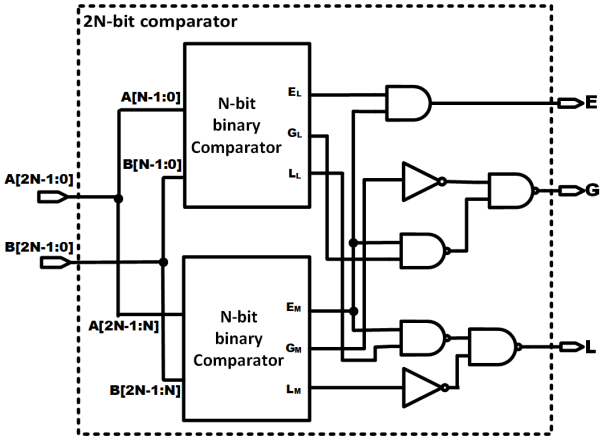


Fig. 2: *Proposed architecture for the 2N-bit binary comparator system.*

All comparator circuit drawbacks [27] are addressed by the proposed binary comparator. Therefore, the proposed comparator circuit provides efficiency in terms of performance for the digital comparison of binary operands.

3. GENERAL STRUCTURE OF PROPOSED BINARY COMPARATOR

An elementary 2-bit high-performance binary comparator is proposed in the previous section. In this section, a generalized model is proposed to compare high radix binary operands by utilizing the 2-bit comparator circuit. The methodology used to design this architecture combines two N-bit binary comparators to create a $2N$-bit version, following the Boolean expression presented in Eqs. (10), (11), and (12) for less 'L_{2N}', greater 'G_{2N}', and equal 'E_{2N}' signals, respectively.

$$E_{2N} = E_M \cdot E_L \tag{10}$$

$$G_{2N} = \overline{G_M \left(\overline{E_M \cdot G_L}\right)} \tag{11}$$

$$L_{2N} = \overline{L_M \left(\overline{E_M \cdot L_L}\right)} \tag{12}$$

Fig. 2 shows the proposed architecture of the $2N$-bit binary comparator, designed using two N-bit binary comparators, i.e., MSB and LSB. The operand inputs of the LSB comparator are $A\,[N-1:0]$ and $B\,[N-1:0]$. Similarly, the inputs of the MSB comparator are $A\,[2N-1:N]$ and $B\,[2N-1:N]$. While the outputs are E_M, G_M, and L_M for the MSB comparator and E_L, G_L, and L_L for the LSB. Finally, the outputs are combined according to Eqs. (7), (8), and (9). The final output of $2N$-bit binary comparator for less L_{2N}, greater G_{2N}, and equal E_{2N} signals is shown in Fig. 2.

Algorithm 1: Steps taken by the backtracking model to identify the input test vector

Input: Gate-level circuit with inputs A_1, A_2, A_3, ..., A_{n-1}, A_n and outputs Y_1, Y_2, ..., Y_{m-1}, Y_m
Initialization: Setting the transition value at the output node:
Case 1: $Y_1 = 0 \rightarrow 1$, $Y_2 = 0 \rightarrow 1$, ..., $Y_{m-1} = 0 \rightarrow 1$, $Y_m = 0 \rightarrow 1$
Case 2: $Y_1 = 1 \rightarrow 0$, $Y_2 = 1 \rightarrow 0$, ..., $Y_{m-1} = 1 \rightarrow 0$, $Y_m = 1 \rightarrow 0$
Output: Input test vector A_1, A_2, A_3, ..., A_{n-1}, A_n
Steps:

1	Nodes S_{11}, S_{12}, ... $\leftarrow$ Set the possible transition/value at the adjacent node (according to Table 1) based on output transition Y_1, Y_2, ..., Y_{m-1}, Y_m
2	Succeeding nodes S_{21}, S_{22}, ... $\leftarrow$ Set the possible transition/value at this node based on preceding nodes transition/value S_{11}, S_{12}, ...
	.
	.
	.
$i-2^{\text{nd}}$	Nodes S_{i-1_1}, S_{i-1_2}, ... $\leftarrow$ Set the possible value at this node based on the transition/value of the preceding nodes S_{i-2_1}, S_{i-2_2}, ...
$i-1^{\text{st}}$	Succeeding nodes S_{i_1}, S_{i_2}, ..., S_{in-1}, S_{in} $\leftarrow$ Set the possible value at this node based on the transition/value of the preceding nodes S_{i-1_1}, S_{i-1_2}, ...
i^{th}	$\{A_1, A_2, A_3, \ldots, A_{n-1}, A_n\} = \{S_{i_1}, S_{i_2}, \ldots, S_{in-1}, S_{in}\}$

End

4. BINARY COMPARATOR BACKTRACKING MODEL

The simulation-based method for power estimation depends on the employment of a suitable set of input test vectors. The significance of this technique is that it accurately estimates power dissipation in VLSI circuits but requires a large memory and long simulation time for big VLSI circuits due to input pattern dependency. For accurate delay estimation of VLSI circuits, dynamic timing analysis (DTA) is an appropriate approach. In this type of analysis, an input test vector can be used for validation, since DTA is dependent on input test vectors. The quality of the simulation depends on the quality of the test case or test vectors. Power analysis at the gate-level also depends on the switching activity of the entire node in a circuit due to input test vectors, since dynamic power dissipation is the most dominant factor in power consumption due to the short circuit and leaking current.

To combine the advantages of the simulation-based method (for power estimation) and the DTA technique (for delay analysis), the backtracking model developed in this section identifies the worst-case performance in terms of delay and power or power-delay product (PDP) for the binary comparator circuit. This technique provides the input test vector for DTA analysis and power estimation in gate-level VLSI circuits. To demonstrate this approach, the proposed and tree-based binary comparators are considered. Firstly, the transition value is set at the output node (i.e., $0 \rightarrow 1$ or $1 \rightarrow 0$), and backtracked at the adjacent input or fan-in node of a particular logic gate to identify the possible transition value at this node. This tracking will continue till the input node is reached and the possible input transition vectors corresponding to the output transition identified. In this process, the maximum possible transition is covered at all nodes in the entire circuit. The worst-case delay scenario along with the power dissipation of comparator circuits can then be identified.

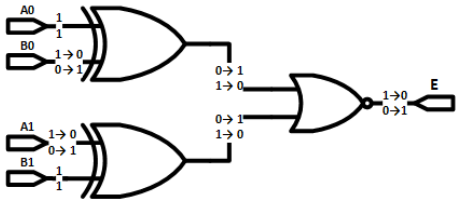
Table 1 presents the possible input and corresponding output activities for each logic gate using the backtracking model, summarizing all possible maximum switching activities corresponding to each basic logic gate. Algorithm 1 indicates the steps taken by the backtracking model to identify the input test vector corresponding to the gate-level VLSI circuits. The inputs for this algorithm are the gate-level circuit with n-inputs (A_1, A_2, A_3, ..., A_{n-1}, A_n) and m-outputs (Y_1, Y_2,..., Y_{m-1}, Y_m). Initially, the transition value is set at the output node in two cases with the circuit divided into i levels from the output to input node and the number of levels equal to the number of gates between the critical path from input to output. The transition value at each output node is set as $0 \rightarrow 1$ and $1 \rightarrow 0$ corresponding to cases 1 and 2. In the first step, the possible transition/value at the adjacent input node of logic gates (S_{11}, S_{12}, ...) is set to the corresponding output transition (Y_1, Y_2, ..., Y_{m-1}, Y_m), with S_{11} representing the first node transition/value in the first level corresponding to output Y_1 and so on. Similarly, in the second step, the possible transition/value is set at the adjacent input node equal to (S_{21}, S_{22}, ...) corresponding to the output transition (S_{11}, S_{12}, ...), with S_{21} representing the first node transition/value in the second level corresponding to output S_{11}. This process continues until the tracking reaches the input node. Finally, in the last

Table 1: *Possible input and corresponding output activities for each gate using the backtracking model.*

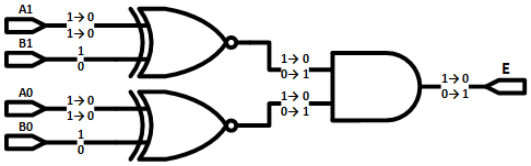
Two input logic gates	Output node activity	Input node activity		
NOT	$0 \rightarrow 1$	$1 \rightarrow 0$		
	$1 \rightarrow 0$	$0 \rightarrow 1$		
	1	0		
	0	1		
Buffer	$0 \rightarrow 1$	$0 \rightarrow 1$		
	$1 \rightarrow 0$	$1 \rightarrow 0$		
	1	1		
	0	0		
		Possible case	Input-1	Input-2
AND	$0 \rightarrow 1$	Case-1	$0 \rightarrow 1$	$0 \rightarrow 1$
		Case-2	1	$0 \rightarrow 1$
	$1 \rightarrow 0$	Case-1	$1 \rightarrow 0$	$1 \rightarrow 0$
		Case-2	1	$1 \rightarrow 0$
	1	Case-1	1	1
	0	Case-1	0	$1 \rightarrow 0$
		Case-2	0	$0 \rightarrow 1$
NAND	$0 \rightarrow 1$	Case-1	$1 \rightarrow 0$	$1 \rightarrow 0$
		Case-2	1	$1 \rightarrow 0$
	$1 \rightarrow 0$	Case-1	$0 \rightarrow 1$	$0 \rightarrow 1$
		Case-2	1	$0 \rightarrow 1$
	1	Case-1	0	$1 \rightarrow 0$
		Case-2	0	$0 \rightarrow 1$
	0	Case-1	1	1
OR	$0 \rightarrow 1$	Case-1	$0 \rightarrow 1$	$0 \rightarrow 1$
		Case-2	0	$0 \rightarrow 1$
	$1 \rightarrow 0$	Case-1	$1 \rightarrow 0$	$1 \rightarrow 0$
		Case-2	0	$1 \rightarrow 0$
	1	Case-1	1	$1 \rightarrow 0$
		Case-2	1	$0 \rightarrow 1$
	0	Case-1	0	0
NOR	$0 \rightarrow 1$	Case-1	$1 \rightarrow 0$	$1 \rightarrow 0$
		Case-2	0	$1 \rightarrow 0$
	$1 \rightarrow 0$	Case-1	$0 \rightarrow 1$	$0 \rightarrow 1$
		Case-2	0	$0 \rightarrow 1$
	1	Case-1	0	0
	0	Case-1	1	$1 \rightarrow 0$
		Case-2	1	$0 \rightarrow 1$
XOR	$0 \rightarrow 1$	Case-1	1	$1 \rightarrow 0$
		Case-2	0	$0 \rightarrow 1$
	$1 \rightarrow 0$	Case-1	1	$0 \rightarrow 1$
		Case-2	0	$1 \rightarrow 0$
	1	Case-1	$0 \rightarrow 1$	$1 \rightarrow 0$
	0	Case-1	$1 \rightarrow 0$	$1 \rightarrow 0$
		Case-2	$0 \rightarrow 1$	$0 \rightarrow 1$
XNOR	$0 \rightarrow 1$	Case-1	1	$0 \rightarrow 1$
		Case-2	0	$1 \rightarrow 0$
	$1 \rightarrow 0$	Case-1	1	$0 \rightarrow 1$
		Case-2	0	$0 \rightarrow 1$
	1	Case-1	$0 \rightarrow 1$	$0 \rightarrow 1$
		Case-2	$1 \rightarrow 0$	$1 \rightarrow 0$
	0	Case-1	$1 \rightarrow 0$	$0 \rightarrow 1$

iteration, the input test vector corresponds to two cases. The transition/value at each node is evaluated using Table 1. To demonstrate this algorithm, the 2-bit proposed and tree-based [27] binary comparator circuits are considered. It generates test vectors corresponding to two possible output transitions (i.e., $0 \rightarrow 1$ and $1 \rightarrow 0$) for the comparator circuits, as further explained in Fig. 3.

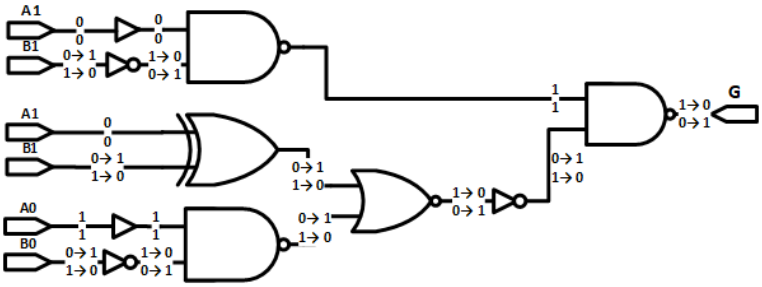
Two possible output transitions (i.e., $0 \rightarrow 1$ and $1 \rightarrow 0$) to generate the test vector for the



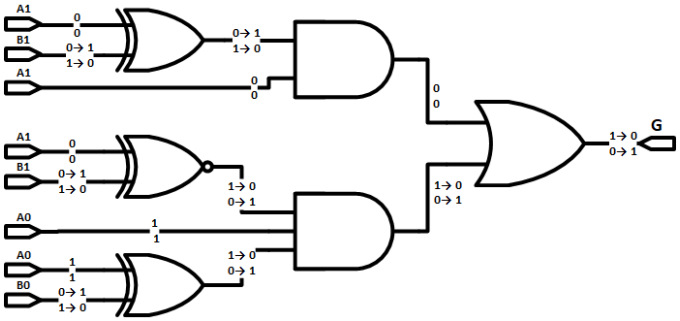
(a) Proposed circuit: 'E' signal



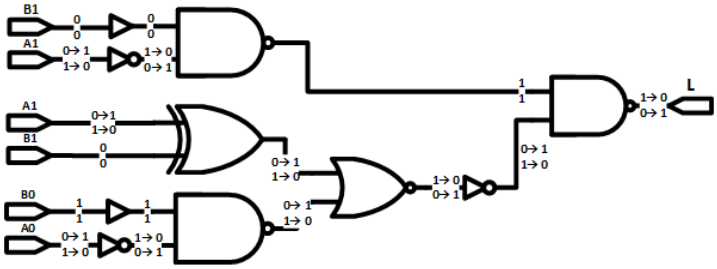
(b) Binary comparator [27]: 'E' signal



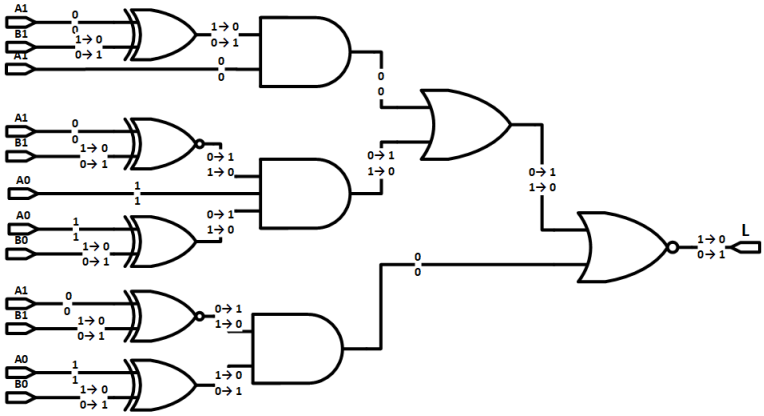
(c) Proposed circuit: 'G' signal



(d) Binary comparator [27]: 'G' signal



(e) Proposed circuit: 'L' signal



(f) Binary comparator [27]: 'L' signal

Fig. 3: *Node value representation through backtracking of a 2-bit binary comparator.*

Table 2: *Possible test pattern for the individual output signal of the proposed and tree-based 2-bit binary comparators.*

Output signal	Test pattern $A_1A_0B_1B_0$			
	Tree-based 2-bit binary comparator		Proposed 2-bit binary comparator	
	Case-1 $0 \rightarrow 1$	Case-2 $1 \rightarrow 0$	Case-1 $0 \rightarrow 1$	Case-2 $1 \rightarrow 0$
'E'	$1100 \rightarrow 0000$	$1111 \rightarrow 0011$	$0110 \rightarrow 1111$	$1111 \rightarrow 0110$
'G'	$0111 \rightarrow 0100$	$0100 \rightarrow 0111$	$0111 \rightarrow 0100$	$0100 \rightarrow 0111$
'L'	$0100 \rightarrow 0111$	$0111 \rightarrow 0100$	$1101 \rightarrow 0001$	$0001 \rightarrow 1101$

proposed and tree-based [27] binary comparators, and potential transition values at each node are shown in Fig. 3. In this model, the input test vectors corresponding to individual output signals (less than 'L', greater than 'G', and equal 'E') are obtained for the worst-case propagation delay and power dissipation scenarios. Fig. 3(a) shows the node value representation using backtracking for the 'E' signal of the 2-bit proposed binary comparator. Similarly, Fig. 3(b) presents the backtracking for the 'E' signal of the 2-bit binary comparator [27]. Fig. 3(c) shows the node value of the backtracking for the 'G' signal of a 2-bit proposed binary comparator, while Fig. 3(d) presents the backtracking for the 'G' signal of 2-bit binary comparator [27]. Fig. 3(e) shows the node value using backtracking for the 'L' signal of the 2-bit proposed binary comparator, and Fig. 3(f) presents the backtracking for the 'L' signal of the 2-bit binary comparator [27]. Table 2 indicates the possible input transition test pattern $A_1A_0B_1B_0$ for individual output signals less than 'L', greater than 'G', and equal to 'E' using the backtracking method. This test vector is employed to simulate both comparator circuits to identify the worst-case performance scenarios for comparison.

5. HIGH-PERFORMANCE XOR GATE

To design the binary comparator, XOR and XNOR circuits play a vital role. Therefore, their behavior prominently affects the circuit performance. Therefore, the design of XOR and XNOR circuits should be given top priority when considering their use in a comparator system. The XOR-XNOR gate [27] uses positive feedback to compensate for the output voltage level. This feedback increases output capacitance and delay, affecting energy consumption. The full swing XOR circuit proposed in [28] demonstrates efficiency in terms of mitigating delay. In all possible input combinations, the output of this structure is full swing voltage. Since no NOT gates are used in this circuit on its critical path, it offers minimum delay, and good driving capability compared to the other structures. This circuit has not previously been utilized in the design of binary

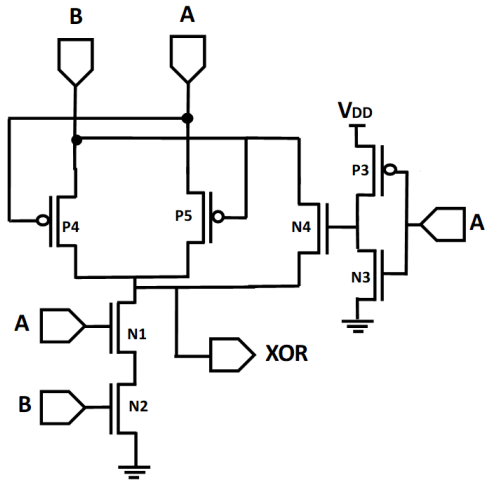


Fig. 4: *Energy-efficient, high-performance XOR circuit [28].*

comparators. In this current work, the XOR circuit (shown in Fig. 4) is used in the proposed binary comparator to enhance performance.

6. SIMULATION ENVIRONMENT

The proposed binary and tree-based binary comparators [27] are simulated using the Pyxis Schematics tool by Mentor Graphics. For simulation and validation, the 180-nm CMOS technology (TSMC) is used. Simulation is also carried out with the 20, 16, 14, 10, and 7-nm FinFET technology. Table 2 shows the typical simulation test vector to identify the worst-case performance scenario in the individual output signal of the elementary 2-bit binary comparator circuit, i.e., total power dissipation, delay, and PDP. This simulation uses the 3.3 V supply voltage for 180-nm CMOS technology and 0.9, 0.85, 0.8, 0.75, 0.7 V supply voltage, corresponding to the 20, 16, 14, 10, 7-nm high-performance FinFET technology. In the rise and fall time transition output, the delay is calculated using 50% of the input value level to 50% of the output voltage level. The PDP is calculated by multiplying the worst-case delay scenario by the total power dissipation exhibited in the circuit.

7. RESULTS AND DISCUSSION

In this section, the results of the simulation are discussed and the proposed 2-bit elementary binary comparator circuit performance compared with the previously reported architecture [27]. Table 3 shows the simulation results of the proposed comparator using 180-nm CMOS technology for validation with a tree-based structure [27]. Table 4 displays the device parameters. Table 5 presents the simulation results of the proposed and existing 2-bit binary comparator for an equal signal 'E' using high-performance FinFET technology with channel lengths of 20, 16, 14, 10, 7-nm. Similarly, Tables 6 and 7 show the simulation

Table 3: *Compression of the proposed and existing 2-bit binary comparators using 180-nm CMOS technology.*

180-nm CMOS technology		D_E (ps)	P_E (mW)	PDP_E ($\times 10^{-15}$ J)	D_G (ps)	P_G (mW)	PDP_G ($\times 10^{-15}$ J)	D_L (ps)	P_L (mW)	PDP_L ($\times 10^{-15}$ J)
2-bit comparator [5]	Case-1	114.50	1.5992	183.1084	189.61	1.6910	320.6305	133.95	1.6229	217.3874
	Case-2	266.80	2.514	670.7352	390.23	1.6229	633.3042	211.74	1.6910	358.0523
Proposed 2-bit comparator	Case-1	70.578	2.3382	165.0255	88.671	0.8233	73.00283	75.589	1.5149	114.5098
	Case-2	40.116	2.3365	93.73103	129.59	1.5152	196.3548	125.17	0.8233	103.0525

results for greater than 'G' and less than 'L' output signals to explore the worst-case performance scenario.

7.1 Performance of the Binary Comparator Using 180-nm CMOS Technology

Table 3 shows the simulation results for the proposed and existing 2-bit binary comparator using TSMC 180-nm CMOS technology with a 3.3 V power supply to validate the proposed work. In this simulation, the worst-case performance scenario is explored such as delay, power, and PDP for two possible input test vector transitions, corresponding to two cases (Case-1, where the output signal transition is from 0 to 1 and Case-2 where the transition is from 1 to 0). The test vectors corresponding to each output signal are shown in Table 2. In Table 3, D_E, P_E, and PDP_E represent the worst-case delay, power, and PDP for the equal signal 'E'. Similarly, D_G, P_G, and PDP_G for the greater signal 'G' and D_L, P_L, and PDP_L for the less than 'L' signal. From Table 3, it can be observed that the performance of the proposed 2-bit binary comparator is superior to the tree-based 2-bit binary comparator [27] since the circuit of the former uses minimum fan-in (2-input) logic gates, replacing the higher fan-in logic gate which suffers from a relatively poor performance in terms of signal delay and total power consumption. The NAND-NOR logic gate is used in the entire circuit while the high-performance XOR gate enhances performance.

7.2 Performance of the Binary Comparator Using FinFET Technology

Conventional bulk CMOS scaling beyond 45-nm is known to be severely constrained by its small geometry effect. Therefore, in recent IC technology, FinFET is used due to its extremely fast and power-efficient devices for overcoming the small geometry effects and enhancing performance. In this simulation, specific input test vectors are used for each output signal from the backtracking model and the worst-case performance corresponding to each output signal identified using the FinFET technology model. Table 4 shows the essential device parameters of the high-performance FinFET and the corresponding technology length.

Table 5 presents the simulation results of the proposed and existing 2-bit binary comparators for the equal signal using the high-performance FinFET with channel lengths of 20, 16, 14, 10, and 7-nm. The input test vector transition in Case-1, 0110 $\rightarrow$ 1111 for the proposed and 1100 $\rightarrow$ 0000 for the tree-based comparator, are employed. Similarly, the input test vector transition in Case-2, 0110 $\rightarrow$ 1111 for the proposed and 1100 $\rightarrow$ 0000 for the tree-based comparator, are used in the worst-case delay scenario and power estimation of the comparator circuits.

Table 6 shows the simulation results of the proposed and existing 2-bit binary comparators for the greater signal using high-performance FinFET with different channel lengths. For this simulation, the input test vector transition 0111 $\rightarrow$ 0100 is used for the proposed and 0111 $\rightarrow$ 0100 is used for the tree-based comparator in Case-1. Similarly, the test vector transition 0100 $\rightarrow$ 0111 for the proposed and 0100 $\rightarrow$ 0111 for the tree-based comparator [27] are used in Case-2.

Similarly, Table 7 shows the simulation results for the less signal of the proposed and existing 2-bit binary comparators using high-performance FinFET with different technology lengths. In this analysis, the possible input test vector is used in Case-1 1101 $\rightarrow$ 0001 for the proposed and 0100 $\rightarrow$ 0111 for the tree-based comparator, while in Case-2 0001 $\rightarrow$ 1101 is used for the proposed and 0111 $\rightarrow$ 0100 is used for the tree-based comparator [27].

The simulation results demonstrate that the performance of the comparator circuit is better than that reported in previous work [27]. It can also be observed that the impact of FinFET on the binary comparator circuit performance, i.e., the propagation delay exponentially decreases with a reduction in technology length while total power dissipates in accordance with a decrease in the channel length of FinFET because the current driving capability of the transistor is inversely proportional to the length of the channel. Therefore, an increase in the current capability of the FinFET device enhances the delay in the overall circuit. Thus, overall increases in the PDP of comparator circuits with technology length reduction can be clearly observed in Tables 5–7.

In recent IC technology, the 7-nm FinFET is widely used for IC fabrication. Fig. 5 presents a transient analysis of the proposed 2-bit binary comparator using 7-nm high-performance FinFET technology with a 0.8 V supply where A_1A_0 and B_1B_0

Table 4: *Device parameters of the high-performance FinFET [29].*

FinFET technology	Nominal Supply Voltage (V)	Gate length (L_G) (nm)	Fin height (H_{fin}) (nm)	Fin pitch (F_{pitch}) (nm)	Physical oxide thickness (T_{ox}) (nm)	S/D doping concentration (m^{-3})
20-nm	0.90	24	28	60	1.40	3×10^{26}
16-nm	0.85	20	26	42	1.35	3×10^{26}
14-nm	0.80	18	23	32	1.30	3×10^{26}
10-nm	0.75	14	21	28	1.20	3×10^{26}
7-nm	0.70	11	18	22	1.15	3×10^{26}

Table 5: *Compression of the proposed and existing 2-bit binary comparators for the 'E' signal using the high-performance FinFET.*

FinFET technology	2-bit comparator [27]						Proposed 2-bit comparator					
	Case-1			Case-2			Case-1			Case-2		
	D_E (ps)	P_E (μW)	PDP$_E$ ($\times 10^{-18}$ J)	D_E (ps)	P_E (μW)	PDP$_E$ ($\times 10^{-18}$ J)	D_E (ps)	P_E (μW)	PDP$_E$ ($\times 10^{-18}$ J)	D_E (ps)	P_E (μW)	PDP$_E$ ($\times 10^{-18}$ J)
20-nm	17.136	1.5627	26.77843	33.182	1.3623	45.20384	15.762	1.4122	22.2591	6.6403	1.4117	9.374112
16-nm	11.432	2.8176	32.2108	23.462	2.4498	57.47721	9.6484	2.5287	24.39791	4.3315	2.5277	10.94873
14-nm	7.5059	5.4618	40.99572	15.158	4.7373	71.80799	6.2269	4.8606	30.26647	2.8195	4.8585	13.69854
10-nm	6.8419	12.4029	84.8594	13.139	10.7194	140.8422	5.9571	10.7555	64.07159	2.6448	10.7448	28.41785
7-nm	6.1898	33.5741	207.817	11.766	28.5519	335.9417	5.5668	27.0456	150.5574	2.4953	26.9658	67.28776

Table 6: *Compression of the proposed and existing 2-bit binary comparators for the 'G' signal using the high-performance FinFET.*

FinFET technology	2-bit comparator [27]						Proposed 2-bit comparator					
	Case-1			Case-2			Case-1			Case-2		
	D_G (ps)	P_G (μW)	PDP$_G$ ($\times 10^{-18}$ J)	D_G (ps)	P_G (μW)	PDP$_G$ ($\times 10^{-18}$ J)	D_G (ps)	P_G (μW)	PDP$_G$ ($\times 10^{-18}$ J)	D_G (ps)	P_G (μW)	PDP$_G$ ($\times 10^{-18}$ J)
20-nm	29.011	1.3512	39.19966	33.758	1.3624	45.9919	14.468	1.3534	19.58099	22.475	1.4904	33.49674
16-nm	19.180	2.4285	46.57863	22.931	2.4494	56.16719	9.7316	2.3900	23.25852	14.477	2.6829	38.84034
14-nm	12.494	4.6885	58.57812	14.965	4.7366	70.88322	6.5018	4.5434	29.54028	9.3254	5.1776	48.28319
10-nm	11.405	10.5241	120.0274	13.479	10.7138	144.4113	5.8767	10.1546	59.67554	8.8519	11.4426	101.2888
7-nm	10.331	27.7440	286.6233	12.591	28.5070	358.9316	5.2745	26.3287	138.8707	8.5482	28.7796	246.0138

Table 7: *Compression of the proposed and existing 2-bit binary comparators for the 'L' signal using the high-performance FinFET.*

FinFET technology	2-bit comparator [27]						Proposed 2-bit comparator					
	Case-1			Case-2			Case-1			Case-2		
	D_L (ps)	P_L (μW)	PDP$_L$ ($\times 10^{-18}$ J)	D_L (ps)	P_L (μW)	PDP$_L$ ($\times 10^{-18}$ J)	D_L (ps)	P_L (μW)	PDP$_L$ ($\times 10^{-18}$ J)	D_L (ps)	P_L (μW)	PDP$_L$ ($\times 10^{-18}$ J)
20-nm	35.847	1.3624	48.83795	32.339	1.3512	43.69646	13.072	1.4135	18.47727	21.868	1.4303	31.2778
16-nm	24.318	2.4494	59.56451	21.375	2.4285	51.90919	8.7598	2.5023	21.91965	14.041	2.5705	36.09239
14-nm	15.899	4.7366	75.3072	13.842	4.6885	64.89822	5.8725	4.7676	27.99773	9.0635	4.9532	44.89333
10-nm	14.332	10.7138	153.5502	12.755	10.5241	134.2349	5.3113	10.6575	56.60518	8.6587	10.9402	94.72791
7-nm	13.328	28.5071	379.9426	11.764	27.7440	326.3804	4.7572	27.7707	132.1108	8.3779	27.3470	229.1104

are the input operands and three output signals, i.e., 'E', 'G', and 'L'. No glitches are observed in the output signals through input transition. Since the buffer is used in the proposed circuit to balance all input signals at each gate in the entire circuit, it can overcome the glitches in the previous comparator circuit caused by input signal imbalance.

Fig. 6 presents a graphical representation of the performance variation of a 2-bit binary comparator using high-performance FinFET technology. The worst-case delay experienced with FinFET technology is compared with the previous architecture as shown in Fig. 6(a), 6(b), and 6(c) for the 'E', 'G', and 'L' signals, respectively. Fig. 6(d), 6(e), and

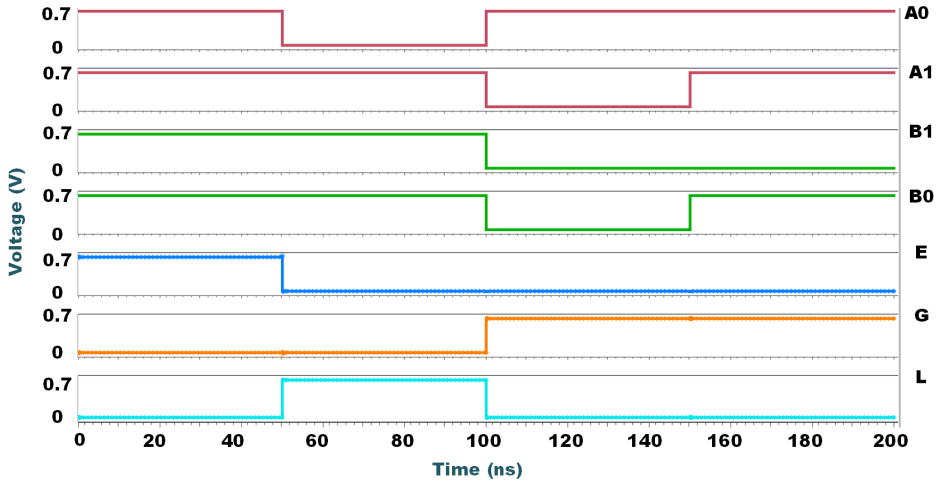
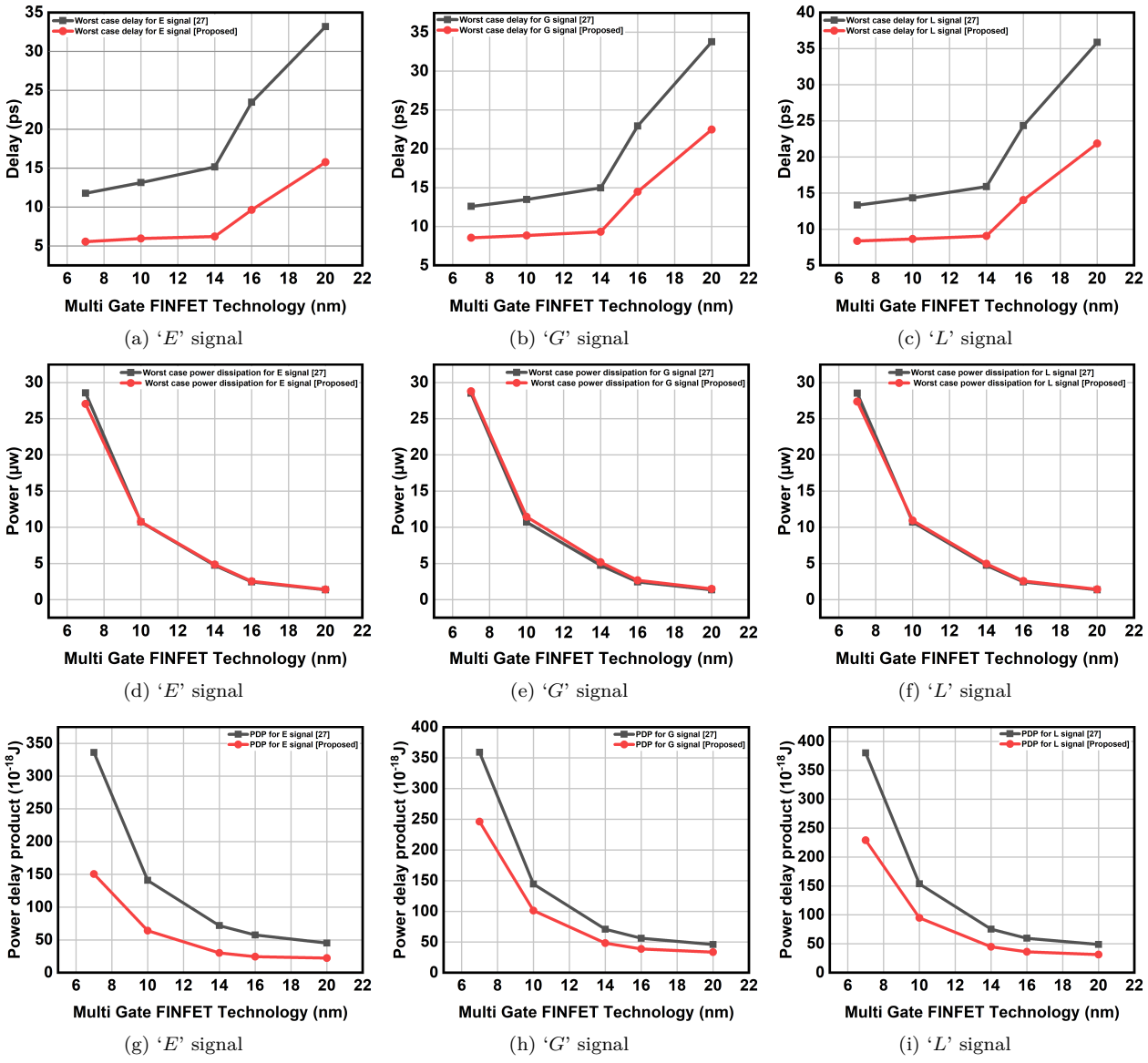


Fig. 5: *Transient analysis of the proposed 2-bit binary comparator using 7-nm FinFET technology.*



(a) '*E*' signal (b) '*G*' signal (c) '*L*' signal

(d) '*E*' signal (e) '*G*' signal (f) '*L*' signal

(g) '*E*' signal (h) '*G*' signal (i) '*L*' signal

Fig. 6: *Performance variation exhibited by the 2-bit binary comparator using FinFET technology with different channel lengths; (a), (b), and (c) worst-case delay; (d), (e), and (f) worst-case power dissipation; (g), (h), and (i) worst-case PDP.*

6(f) show the performance variation of worst-case power dissipation with FinFET technology for 'E', 'G', and 'L' signals, respectively. Finally, the graph in Fig. 6(g), 6(h), and 6(i) shows the worst-case PDP and FinFET technology length corresponding to the output signals 'E', 'G', and 'L'. It can be concluded from this graph that the impact of FinFET on binary comparator performance, i.e., propagation delay exponentially decreases with a reduction in technology length, and total power dissipates with a reduction in technology length because the current driving capability of the transistor is inversely proportional to the length of the channel. Thus, the PDP exhibits an overall increase when the FinFET technology length decreases. Furthermore, the proposed work demonstrates a better performance when FinFET technology is used in comparison to the conventional 180-nm CMOS technology.

8. CONCLUSION

In this work, an elementary 2-bit binary comparator circuit is proposed to minimize the fan-in of logic gates (NAND-NOR). A general $2N$-bit comparator structure is also proposed to operate high radix binary operands of the elementary binary comparator circuit, thereby overcoming the dependency of the operand size of logic gate fan-in. Thereafter, an accurate estimation is obtained of power dissipation and delay using the backtracking model to demonstrate that the worst-case performance of the proposed circuit is better than that of the previously reported architecture [27]. The input test vector is obtained from this method for two cases (for each output signal, involving the maximum possible transition at each node) to compute the maximum possible delay and power or PDP in the circuits. Initially, the proposed architecture is validated using 180-nm CMOS technology for comparison with the reported results [27]. The proposed architecture utilizes a high-performance energy-efficient XOR circuit to improve the performance of the comparator system. The overall PDP reduces by 68% compared to the earlier reported comparator circuit using the tree-based structure [27]. The performance of the comparator circuit, employing FinFET technology in varying channel lengths is also observed in this work. The simulation results show that the propagation delay exponentially decreases by 62% when the higher-order channel length is reduced by 50% (i.e., 20 nm to 10 nm) whereas, its power dissipates by 661%. The overall increase in PDP is observed to be 187%. During a similar analysis at a lower-order FinFET channel length (i.e., 14 nm to 7 nm) the decrease in propagation delay was only 11%, while its power dissipates by 456%. The overall PDP for such circuits increases by 397%. Therefore, it can be concluded that beyond 7-nm FinFET technology, the comparator circuit performance degrades significantly. The proposed 2-bit binary comparator is better in terms of performance when FinFET technology is used compared to conventional 180 nm CMOS technology.

REFERENCES

[1] S.-W. Cheng, "Arbitrary long digit integer sorter HW/SW co-design," in *Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2003, pp. 538–543.

[2] R. Woo, S. Choi, J. H. Sohn, S. J. Song, Y. D. Bae, and H. J. Yoo, "A low-power 3-D rendering engine with two texture units and 29-Mb embedded dram for 3G multimedia terminals," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1101–1109, July 2004.

[3] M. D. Gupta and R. K. Chauhan, "Efficient Hardware Implementation of Pseudo-Random Bit Generator Using Dual-CLCG Method," *Journal of Circuits, Systems and Computers*, Feb. 2021, Art. no. 2150182.

[4] M. D. Gupta and R. K. Chauhan, "Coupled Variable Input-LCG and Clock Divider based Large Period Pseudo-Random Bit Generator on FPGA," *IET Computers & Digital Techniques*, Apr. 2021.

[5] D. Kim, K. Kim, J. Y. Kim, S. Lee, and H. J. Yoo, "An 81.6 GOPS Object Recognition Processor Based on NoC and Visual Image Processing Memory," in *Proceedings of the IEEE 2007 Custom Integrated Circuits Conference (CICC)*, 2007, pp. 443–446.

[6] D. G. Lowe, "Distinctive image features from scale-invariant keypoints," *International Journal of Computer Vision*, vol. 60, pp. 91–110, 2004.

[7] W. San-Um and T. Masayoshi, "A Low-Cost High-Speed Pulse Response Based Built-In Self Test For Analog Integrated Circuits," *ECTI Transactions on Electrical Engineering, Electronics, and Communications*, vol. 8, no. 2, pp. 197–208, 2009.

[8] I.-C. Wey, T.-C. He, H.-C. Chow, P.-H. Sun, and C.-C. Peng, "A high-speed, high fan-in dynamic comparator with low transistor count," *Journal of Circuits, Systems and Computers*, vol. 101, no. 5, pp. 681–690, 2013.

[9] O. S. Fadl, M. F. Abu-Elyazeed, M. B. Abdelhalim, H. H. Amer, and A. H. Madian, "Accurate dynamic power estimation for CMOS combinational logic circuits with real gate delay model," *Journal of Advanced Research*, vol. 7, no. 1, pp. 89–94, Jan. 2016.

[10] A. S. Aldeen and H. Al-Asaad, "A new method for power estimation and optimization of combinational circuits," in *Proceedings of the International Conference on Microelectronics (ICM)*, 2007, pp. 395–398.

[11] S. M. Kang, "Accurate Simulation of Power

Dissipation in VLSI Circuits," *IEEE Journal of Solid-State Circuits*, vol. 21, no. 5, pp. 889–891, Oct. 1986.

[12] S. Bhanja and N. Ranganathan, "Switching Activity Estimation of VLSI Circuits Using Bayesian Networks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 4, pp. 558–567, Aug. 2003.

[13] H. Li, J. K. Antonio, and S. K. Dhall, "Fast and precise power prediction for combinational circuits," in *Proceedings of IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2003, pp. 254–259.

[14] F. MacHado, T. Riesgo, and Y. Torroja, "Disjoint region partitioning for probabilistic switching activity estimation at register transfer level," in *PATMOS 2008: Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation* (Lecture Notes in Computer Science, vol. 5349), L. Svensson and J. Monteiro, Eds. Berlin, Germany: Springer, 2009, pp. 399–408.

[15] G. Wang, S. Sheng, and L. Ji, "New efficient design of digital comparator," in *Proceedings of International Conference on ASIC*, 1996, pp. 263–266.

[16] D. Kythe and P. Kythe, "Digital Arithmetic," in *Algebraic and Stochastic Coding Theory.* San Francisco, CA, USA: Morgan Kaufmann Publishers, 2017, pp. 15–42.

[17] C.-C. Wang, C.-F. Wu, and K.-C. Tsai, "1GHz 64-bit high-speed comparator using ANT dynamic logic with two-phase clocking" *IEE Proceedings - Computers and Digital Techniques*, vol. 145, no. 6, pp. 433–436, 1998.

[18] C. H. Huang and J. S. Wang, "High-performance and power-efficient CMOS comparators," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 254–262, 2003.

[19] H.-M. Lam and C.-Y. Tsui, "High performance single clock cycle CMOS comparator," in *2006 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2006, pp. 779-782.

[20] J. Y. Kim and H. J. Yoo, "Bitwise competition logic for compact digital comparator," in *2007 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2007, pp. 59–62.

[21] K. Furuya, "Design methodologies of comparators based on parallel hardware algorithms," in *2010 10th International Symposium on Communications and Information Technologies (ISCIT)*, 2010, pp. 591–596.

[22] S. Veeramachaneni, M. K. Krishna, L. Avinash, P. Sreekanth Reddy, and M. B. Srinivas, "Efficient design of 32-bit comparator using carry look-ahead logic," in *2007 IEEE North-East Workshop on Circuits and Systems (NEWCAS)*, 2007, pp. 867–870.

[23] S. Perri and P. Corsonello, "Fast low-cost implementation of single-clock-cycle binary comparator," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 12, pp. 1239–1243, Dec. 2008.

[24] F. Frustaci, S. Perri, M. Lanuzza, and P. Corsonello, "A new low-power high-speed single-clock-cycle binary comparator," in *2010 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2010, pp. 317–320.

[25] P. Chuang, D. Li, and M. Sachdev, "A low-power high-performance single-cycle tree-based 64-bit binary comparator," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 2, pp. 108–112, 2012.

[26] P. I. J. Chuang, M. Sachdev, and V. C. Gaudet, "A 167-ps 2.34-mW single-cycle 64-Bit binary tree comparator with constant-delay logic in 65-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 1, pp. 160–171, Jan. 2014.

[27] C. Chua, R. B. N. Kumar, and B. Sireesha, "Design and analysis of low-power and area efficient N-bit parallel binary comparator," *Analog Integrated Circuits and Signal Processing*, vol. 92, pp. 225–231, 2017.

[28] H. Naseri and S. Timarchi, "Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 8, pp. 1481–1493, 2018.

[29] Nanoscale Integration and Modeling (NIMO) Group, Arizona State University. "Latest Model". `http://ptm.asu.edu/latest.html`

Mangal Deep Gupta is currently pursuing his Ph.D. degree in the field of Microelectronics & VLSI Design at the Department of Electronics and Communication Engineering, Madan Mohan Malaviya University of Technology, Gorakhpur, Uttar Pradesh, India. His research areas include design of VLSI circuits and systems.

Rajeev Kumar Chauhan is currently a Professor at the Department of Electronics & Communication Engineering, Madan Mohan Malaviya University of Technology, Gorakhpur, Uttar Pradesh, India. His research area includes modelling and Simulation of MOS based devices and circuits, Analog and Digital Integrated Circuits, VLSI Technology & Design.