

Geometrical Variation of a Conductive Filament in RRAM and Its Impact on a Single-Event Upset

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ABSTRACT

Resistive random access memory (RRAM) is a promising candidate for industry and academia from the research and development perspective. The resistance of RRAM depends on the geometrical dimensions, growth, and rupture of the conductive filament. In this work, the geometrical dimensions such as the length and width of the filament are varied to analyze the resistance. Moreover, the RRAM can be used in aerospace applications. Therefore, the impact of a single-event upset on resistance of RRAM is investigated by means of a double exponential current pulse. The performance of the device is compared in terms of resistance before and after irradiation. A decrease in its original resistance has been observed after radiation.

Keywords: Conductive Filament, Single-Event Upset, SEU, Resistive Random Access Memory, RRAM

1. INTRODUCTION

In the present and future world, the interaction between people and devices is likely to increase, potentially reaching approximately 4,800 times per day. Hence, data will be acquired from sensors and processed, which requires fast and voluminous data storage as well as real-time processing [1]. To accelerate the processing, emerging memory devices and technologies are promising candidates for non-volatile, low-power, high-speed, low-cost handling of big data [2]. The MRAM, FRAM, Nano-RAM, Racetrack, and RRAM are strong candidates from the family of memory devices [3]. Resistive switching memories are the leading solution for neuromorphic computing and upcoming storage systems [4]. The growth and rupture of the conductive filament modulate the RRAM's effectiveness. The formation and rupture of the conductive filament leads to a low-resistance state (LRS) and a high-resistance state (HRS), respectively [5].

Many researchers have extensively investigated the formation and shape of the nano conductive filaments

in the switching layer. Two main types of nano filaments are mainly observed in RRAM: oxygen vacancy nano and metal nano. Metal filaments are observed in RRAM systems like Ag/GeS₂/W [6], Ag/AgI/Pt [7], Ag/Ta₂O₅/Pt [8], and Nb/ZnO/Pt [9]. Oxygen vacancy nano filament RRAM devices consist of Pt/HfO₂/Pt [10], W/CeO_x/SiO₂/NiSi₂ [11], and Ti/TiO₂/SrTiO₃/n+ Si [12]. The metal filaments are more distinct than the oxygen vacancy filaments [13]. In the switching layer, the lack of uniformity in the formation of nano conductive filaments leads to instability in the RRAM switching performance [14–15]. Many approaches have been proposed to overcome the aforementioned problem such as employing bilayer structures [16–17], the placement of pyramid-shaped electrodes [18–19], implanting metal nano particles in the switching/insulating layer [20–22], and doping the switching layer [23–24]. Celano *et al.* [25] visualized three-dimensional conductive nano filaments. They employed an approach known as conductive atomic force microscopy (CAFM) to acquire information on the nano filaments, observing conical-shaped filaments and noting that the narrow end of the filament was nearer to the inert electrode. While Wu *et al.* [26] observed the formation of single as well as multiple nano filaments in the dielectric stack of Ni/HfO₂/SiO_x/Si RRAM device. In the case of multiple filaments, there is a large variation in the size of the nano filaments. The shape of the filament is in the form of truncated cones. In practice, the compliance current controls the growth of the conductive nano filament [27]. However, all the research referred to concentrates on controlling the nano filaments and their number but this work mainly focuses on the variation in geometrical dimensions of the nano filament to acquire RRAM resistance.

In this work, Section 2 deals with a single-event upset in RRAM. The simulation setup is described in Section 3 while Section 4 focuses on the results and discussion. The conclusion is presented in Section 5.

2. EFFECT OF A SINGLE-EVENT UPSET ON RRAM

The ionizing particles passing through the semiconductor memories induce soft errors or a single-event upset (SEU) [28]. These ionizing particles sometimes cause hard errors too. This is termed a single-event latch-up (SEL) [29]. The damage caused is temporary in the case of soft errors but permanent for hard errors. A reliability problem arises in the memories due to the influence of an SEU [30]. The factors governing the SEU in memories are the sensitive region of the device and

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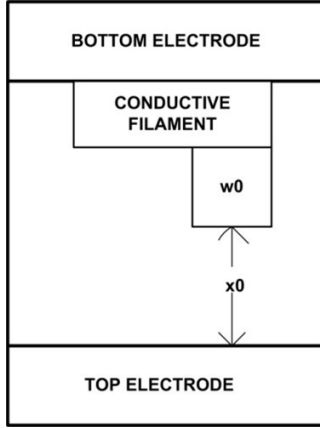


Fig. 1: Structure of the RRAM.

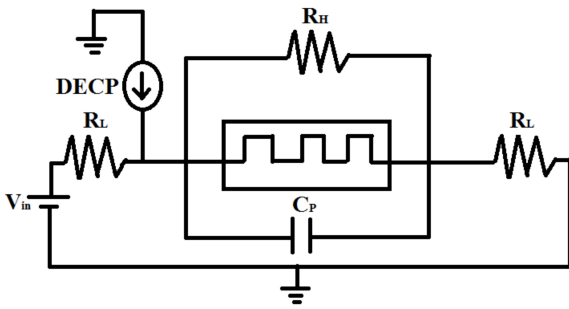


Fig. 2: Circuit setup for the simulation [37].

minimum ionization energy. The linear energy transfer (LET) and the critical charge (Q_C) are the parameters which assist threshold measurement [31]. The x-rays, heavy ions, particle accelerators, Cobalt-60, cyclotron, alpha particles, and gamma rays can be bombarded to study the SEU impact on memory devices [32].

Liu *et al.* [33] considered the 1T1R and the crossbar array in the investigation of single as well as multi-bit upsets. The susceptibility analysis is performed by means of simulations at the circuit level. In this work, it is evident that the maximum radiation tolerance is demonstrated by the crossbar array. The sensitive nodes are the driver circuits. Bennett *et al.* [34] employed TCAD for the modeling, incorporating the 1T1R array. The changes are induced in the array by modeling the irradiation. Changes in the RRAM performance can be observed to have an exponential relationship with the potential applied across the device. They also proposed that the radiation hardened the RRAM in space applications. Liu *et al.* [35] considered both the crossbar and 1T1R array for irradiation due to the heavy ions involved. The rate of upset, vulnerable time window, and the sensitive region are the factors imbibed in the susceptibility analysis. The minimum bit-error rate is observed in the crossbar structure. Bi *et al.* [36] carried out a total ionizing dose and single-event effects analysis on the HfO_2 -based 1T1R RRAM structure. The pulsed laser and Cobalt-60 are used in this work. The read

Table 1: Parameters used for the simulation [37].

RRAM Model Parameters	
Gap length (x_0)	0–3 nm
Width of the filament (w_0)	0.5–5 nm
Input voltage (V_{in})	2 V
Switching layer width (W_{CF})	5 nm
Electrode contact resistance (R_L)	20 Ω
Electrode parasitic capacitance (C_P)	20 fF
Oxide parasitic resistance (R_H)	200 M Ω
Initial switching layer length (L_0)	3 nm
Effective thermal resistance (R_{th})	5×10^5 k Ω
Effective width (W_{eff})	0.5 nm
DECP Parameters	
Minimum value	0 A
Maximum value	1 mA / 1 μ A
Rise time start	20 μ s
Rise time constant	500 ns
Fall time start	22 μ s
Fall time constant	250 ns

failures and bit errors are caused by irradiation. For space application, this analysis places greater emphasis on developing radiation-hardened RRAM. It can be observed that all the aforementioned works focus on either the crossbar or 1T1R arrays. Moreover, in our previous work, the SEU in RRAM was analyzed with respect to either the length or width of the conductive nano filament [37]. In the present work, the SEU on the RRAM device is analyzed with respect to the geometrical dimensions of the conductive nano filament, namely length and width.

3. SIMULATION SETUP

The RRAM structure used for analysis is shown in Fig. 1. It consists of a top electrode, switching material, and a bottom electrode. The filament width is represented by w_0 . If the w_0 increases, the filament will grow in the lateral direction. The length of the filament is modeled as an initial gap (x_0). If the filament length is longer than x_0 will be less and vice versa. If the x_0 is less, the filament grows in the vertical direction [37].

Fig. 2 shows the simulation setup to study the influence of an SEU on the RRAM. The circuit setup comprises mainly the RRAM device, the resistor (R_H) which models the parasitic resistance of the switching layer, and the capacitance between the bottom and the top contacts modeled by the capacitor (C_P). The resistor (R_L) represents the contact resistance of both the bottom and top electrodes. The double exponential current pulse (DECP) is injected at the junction of the top and switching layer to analyze the SEU. Table 1 presents the RRAM and DECP parameters incorporated in this work [37].

For the purpose of simulation, the Peking University-Stanford University RRAM spice model version 2.0-beta is being incorporated [38–41]. The single-event upset is modeled as a double exponential current pulse [42].

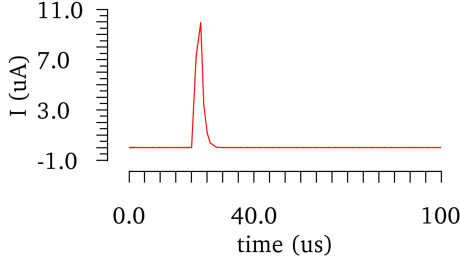


Fig. 3: Double exponential current pulse of 10 μA .

Table 2: Relationship between the DECP value and its equivalent charge [37].

DECP	Equivalent Charge
1 μA	1.469 pC
10 μA	14.69 pC
50 μA	73.5 pC
100 μA	146.9 pC
250 μA	367.2 pC
500 μA	734.5 pC

Fig. 3 shows the typical double exponential current pulse of 10 μA . All simulations are performed using Cadence EDA. In all our simulation work, the x_0 is varied from 3 to 0 nm whereas the w_0 is varied from 0.5 to 5 nm. Table 2 shows the DECP values and their equivalent charge [37]. For DECP values of less than 1 μA , the SEU has no influence on the RRAM resistance. Hence, a DECP range of 1 μA to 500 μA is considered for analysis purposes.

4. RESULTS AND DISCUSSION

Initially, without injecting the DECP, the resistance of the RRAM is evaluated with respect to x_0 and w_0 . Fig. 4 shows the variation in RRAM resistance versus x_0 and w_0 . As the value of x_0 reduces from 3 to 0 nm, a gradual increase occurs in the filament length. The width of the filament widens as w_0 increases from 0.5 to 5 nm. Therefore, the filament grows in both vertical and lateral directions. Hence, the resistance of the device shows a gradual decrement as depicted in Fig. 4. The device offers a resistance of 248 k Ω when x_0 is 3 nm while w_0 is 0.5 nm, representing its HRS. The resistance drops to 3.03 k Ω when x_0 is 2 nm and w_0 is 2 nm, representing the LRS of the device. The device remains in LRS when $x_0 \leq 2$ nm, while $w_0 \geq 2$ nm. When $x_0 \leq 2$ nm, while $w_0 \geq 2$ nm both lateral and vertical growth occurs in the switching layer. This leads to an increase in current. Therefore, the resistance will drop to 3.03 k Ω . The HRS to LRS ratio is 81.87, representing the ratio of 248.08 k Ω to 3.03 k Ω .

The current flowing through the RRAM cell (I_{cell}) is given by

$$I_{\text{cell}} = I_{\text{sub-oxide}} + I_{\text{CF}} + I_{\text{Pristine}} \quad (1)$$

where I_{CF} denotes the conduction caused by the nano

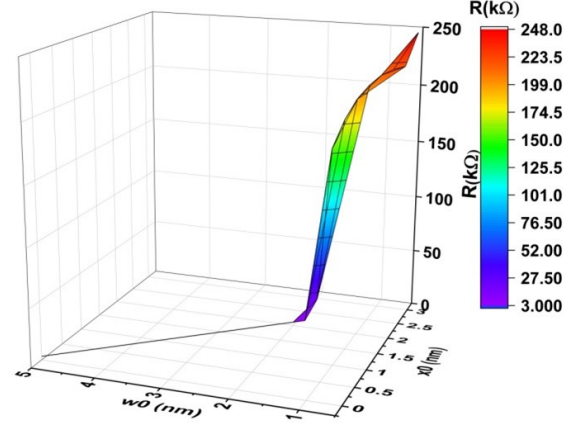


Fig. 4: 3D graph of resistance of the RRAM without injecting the DECP.

filament, I_{Pristine} represents the conduction due to unswitched pristine oxide, and $I_{\text{sub-oxide}}$ the conduction through switchable sub-oxide [42]. Since the growth of the nano conductive filament takes place both vertically and laterally, the I_{CF} term contributes significantly. Hence, the overall I_{cell} increases and the RRAM performance decreases.

The various currents in Eq. (1) can be elaborated as shown in Eqs. (2), (3), and (4), respectively.

$$I_{\text{CF}} = F\pi\sigma_{\text{CF}}r_{\text{CF}}^2 \quad (2)$$

$$I_{\text{sub-oxide}} = F\pi\sigma_{\text{OX}}(r_{\text{CFmax}}^2 - r_{\text{CF}}^2) \quad (3)$$

$$I_{\text{Pristine}} = S_{\text{cell}}AF^2 \exp\left(\frac{-B}{F}\right) \quad (4)$$

where

$$A = \frac{m_e q^3}{8\pi h m_e^{\text{OX}} \phi_b};$$

$$F = \text{electric field} = \left(\frac{V_{\text{cell}}}{L_x}\right);$$

$$B = \frac{8\pi\sqrt{2m_e^{\text{OX}}}}{3h q} \phi_b^{1.5};$$

h Planck constant;

S_{cell} section of the device;

ϕ_b metal-oxide barrier height;

r_{CF} radius of the conductive filament;

r_{CFmax} radius of the switchable oxide;

σ electrical conductivity;

m_e effective electron masses into the cathode;

m_e^{OX} effective electron masses into the oxide [43].

Firstly, to analyze the impact of an SEU on the RRAM, a DECP of 1 μA is injected. The initial gap length (x_0) and the width of the filament (w_0) are varied simultaneously. The current flowing through the RRAM is measured. The resistance of the device is evaluated by the ratio of the applied input voltage (V_{in}) to the current flowing. The graph of RRAM resistance is plotted with respect to x_0 and w_0 as shown in Fig. 5 when a DECP of 1 μA is injected. The injected current pulse causes more

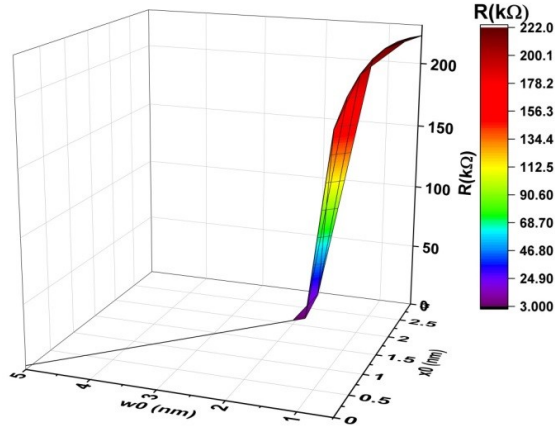


Fig. 5: 3D graph of an SEU on RRAM when the DEC = $1 \mu A$.

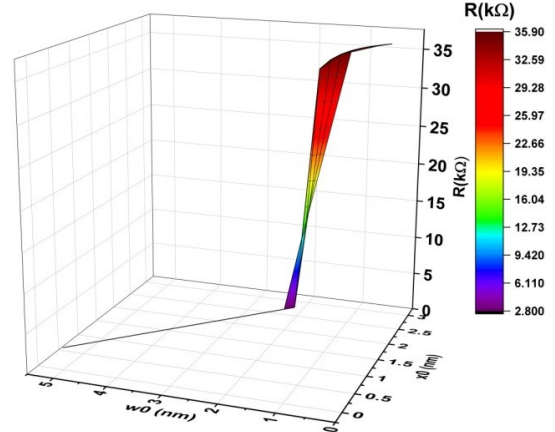


Fig. 7: 3D graph of an SEU on RRAM when the DEC = $50 \mu A$.

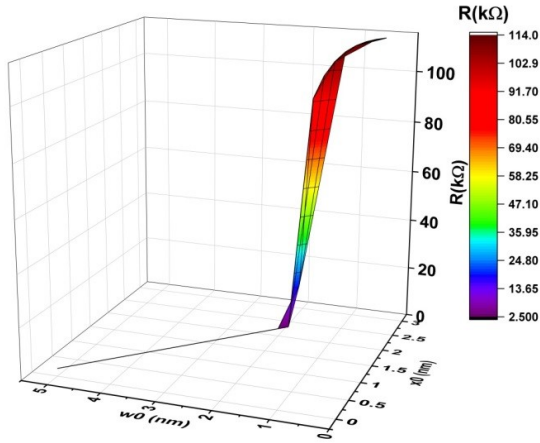


Fig. 6: 3D graph of an SEU on RRAM when the DEC = $10 \mu A$.

redox reactions inside the switching material of the device. Hence, an outgrowth of the filament will occur in both lateral and vertical directions. Therefore, there will be a drop in resistance compared to the state of RRAM without injecting the DEC. In this case, $222 \text{ k}\Omega$ corresponds to $x_0 = 3 \text{ nm}$ and $w_0 = 0.5 \text{ nm}$. This can be considered as the HRS, while the LRS of $3.03 \text{ k}\Omega$ corresponds to $x_0 \leq 2 \text{ nm}$ and $w_0 \geq 2 \text{ nm}$. The HRS to LRS ratio is 73.26 which is the ratio of $222 \text{ k}\Omega$ to $3.03 \text{ k}\Omega$.

The physical mechanism of the SEU on the RRAM can be explained as follows: excess holes and oxygen vacancies are generated due to irradiation. The space charge area within the switching layer is altered due to these excess charge carriers. These carriers tend to accumulate at the interface of the switching layer as well as near the top contact. This leads to the Schottky barrier bending and the height being lowered. The Schottky barrier height (Φ) and the current density (J) due to irradiation is given by

$$J = A^* T^2 \exp\left(\frac{q\sqrt{qE/4\pi\epsilon_i} - q\Phi}{kT}\right) \quad (5)$$

where A^* is the Richardson constant, q is the electron charge, ϵ_i is the insulator permittivity, k is the Boltzmann constant, T is the absolute temperature, and E is the applied electric field [44–45].

The development of the conductive nano filament in both the lateral and vertical direction is contributed by the newly generated oxygen vacancies due to irradiation. As well as the aforementioned process, there is also an increase in the number of conductive nano filaments. Therefore, a reduction in the RRAM resistance can be observed [44].

Secondly, a DEC of $10 \mu A$ is injected. Compared to the previous case (DEC = $1 \mu A$), the injected DEC further enhances the rate of redox reactions. This leads to the development of the length and width in the conductive filament. The graph of RRAM resistance versus x_0 and w_0 is presented in Fig. 6. The variation of the resistance is in terms of kilohms for $x_0 > 2 \text{ nm}$ and $w_0 < 2 \text{ nm}$. It can be observed that the resistance offered is $113.6 \text{ k}\Omega$ when $x_0 = 3 \text{ nm}$ and $w_0 = 0.5 \text{ nm}$. As the filament grows, the resistance drops to $2.99 \text{ k}\Omega$ for $x_0 \leq 2 \text{ nm}$, while $w_0 \geq 2 \text{ nm}$. The HRS to LRS ratio is 37.99 for which the ratio is $113.6 \text{ k}\Omega$ to $2.99 \text{ k}\Omega$.

Thirdly, a DEC of $50 \mu A$ is injected, which is equivalent to depositing a charge of 73.5 pC . Fig. 7 shows the plot of RRAM resistance versus x_0 and w_0 when a DEC of $50 \mu A$ is injected. Compared to the DEC of $10 \mu A$, the rate of redox reactions is enhanced by almost five times. Hence, for $x_0 = 3 \text{ nm}$ and $w_0 = 0.5 \text{ nm}$ itself, the device demonstrates a resistance of $35.88 \text{ k}\Omega$. This shows the impact of a DEC in the formation of a conductive filament to some extent. The resistance variation is only a few hundred ohms for $x_0 > 2 \text{ nm}$ and $w_0 < 2 \text{ nm}$. This contributes to a decrease in the resistance of the device. Finally, the device offers a resistance of $2.83 \text{ k}\Omega$ for $x_0 \leq 2 \text{ nm}$, while $w_0 \geq 2 \text{ nm}$. The HRS to LRS ratio is

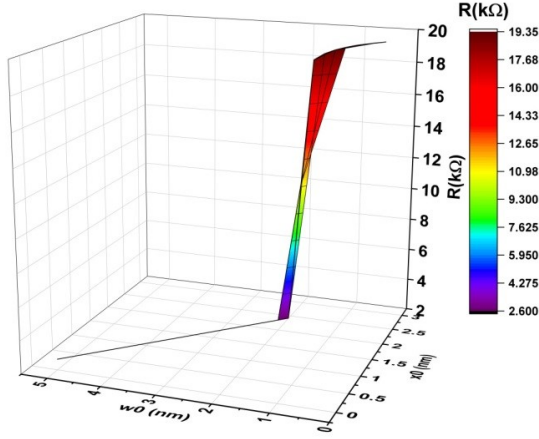


Fig. 8: 3D graph of an SEU on RRAM when the DECp = 100 μ A.

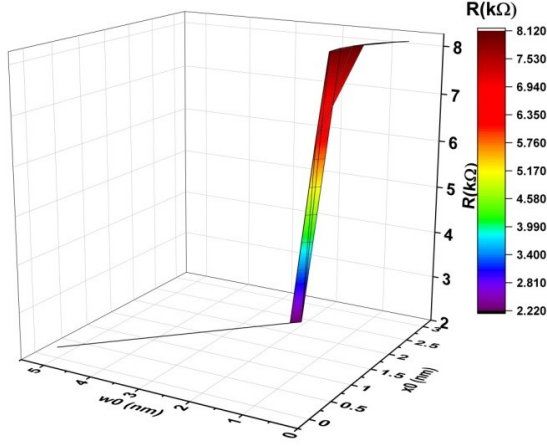


Fig. 9: 3D graph of an SEU on RRAM when the DECp = 250 μ A.

12.67 which is the ratio of 35.88 k Ω to 2.83 k Ω .

Furthermore, a DECp of 100 μ A is injected to observe the influence of an SEU on RRAM resistance. The 100 μ A corresponds to an equivalent charge of 146.9 pC. Fig. 8 shows the plot of RRAM resistance versus x_0 and w_0 . It can be observed that the filament has grown by 90% both in lateral and vertical directions. Hence, there is a greater reduction in resistance. Therefore, 19.34 k Ω of resistance is observed when $x_0 = 3$ nm and $w_0 = 0.5$ nm. As the x_0 decreases and w_0 increments, the resistance drops in terms of a few hundred ohms. Finally, the least resistance state of 2.65 k Ω is observed for $x_0 \leq 2$ nm while $w_0 \geq 2$ nm. The ratio of HRS to LRS is 7.3 which is the ratio of 19.34 k Ω to 2.65 k Ω .

In this case, a DECp of 250 μ A is injected. Fig. 9 shows the variation of RRAM resistance versus x_0 and w_0 with a DECp of 250 μ A. The 250 μ A corresponds to a charge of 367.2 pC. From the simulations, it can be observed that the resistance variation is limited to a few tens of ohms compared to the previous cases. The resistance observed is 8.114 k Ω for $x_0 = 3$ nm and $w_0 = 0.5$ nm. The device remains in a resistance of 2.23 k Ω for $x_0 \leq 2$ nm, while

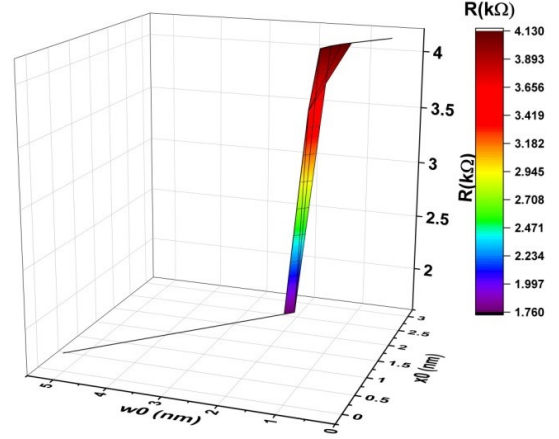


Fig. 10: 3D graph of an SEU on RRAM when the DECp = 500 μ A.

Table 3: Comparison of resistance of RRAM with respect to the dimensions of a conductive nano filament under different DECps.

x_0 (nm)	w_0 (nm)	RRAM Resistance (k Ω)						
		Without DECp	DECp 1 μ A	DECp 10 μ A	DECp 50 μ A	DECp 100 μ A	DECp 250 μ A	DECp 500 μ A
3	0.5	248.08	222	113.6	35.88	19.34	8.114	4.130
2.5	1.25	215.76	195	106	35.11	19.11	8.07	4.115
2	2	3.03	3.03	2.99	2.83	2.65	2.23	1.76
1.5	2.75	3.03	3.03	2.99	2.83	2.65	2.23	1.76
1	3.5	3.03	3.03	2.99	2.83	2.65	2.23	1.76
0.5	4.25	3.03	3.03	2.99	2.83	2.65	2.23	1.76
0	5	3.03	3.03	2.99	2.83	2.65	2.23	1.76

$w_0 \geq 2$ nm. The ratio of HRS to LRS will be 3.64 which is the ratio of 8.114 k Ω to 2.23 k Ω .

Lastly, a DECp of 500 μ A is injected. The 500 μ A corresponds to an equivalent charge of 734.5 pC. Fig. 10 shows the variation in RRAM resistance versus x_0 and w_0 when 500 μ A is injected. From the simulations, it can be observed that the filament has grown by 98%. Hence, the resistance is 4.130 k Ω when $x_0 = 3$ nm and $w_0 = 0.5$ nm, whereas the device offers resistance of 1.76 k Ω for $x_0 \leq 2$ nm, while $w_0 \geq 2$ nm. Therefore, the ratio of HRS to LRS still further reduces to 2.34. The resistance variations are limited to a few ohms for every decrement in x_0 and increment in w_0 . Table 3 presents an overall comparison of the entire work.

5. CONCLUSION

In this work, the impact of an SEU on RRAM is analyzed with respect to the dimensions of the conductive filament. The impact represents the resistance of the device changes from HRS to LRS. As well as the resistance, the HRS to LRS ratio has also been reduced from 81.87 to 2.34. The memory window size will be the lowest. Suitable hardening techniques are proposed to mitigate the SEU effects on the RRAM. Further analysis

can be carried out on multi-nano conductive filaments. Apart from the length and width variations, the thickness variation of the filament can also be considered in future work.

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