A Phase Lead-Lag Synchronous Reference Frame Phase-locked loop for Grid Synchronization of a Single-Phase Inverter

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ABSTRACT

In this study, a phase lead-lag synchronous reference frame phase-locked loop (SRF-PLL) is proposed for the grid connection of a single-phase inverter. A tuned filter is employed to enable the phase of the input voltage to be advanced or delayed by ±45 degrees with respect to the grid voltage. The generated orthogonal signals are fed into Park's transformation. Only the quadrature-phase signal is regulated to zero using a PI controller. Its output determines the estimated frequency. The phase angle is obtained by integrating the estimated frequency. The linearized model of the proposed SRF-PLL is developed and stability analysis is discussed. The viability of the proposed method is tested under computer simulation using MATLAB/Simulink. The method is then implemented on a 32-bit microcontroller and tested with a programmable AC source. The results positively confirm the effectiveness of the method.

Keywords: Phase Lead-Lag, Synchronization, Single-Phase Inverter, Phase-Locked Loop

1. INTRODUCTION

At present, electrical power systems are migrating from radial power systems toward the distributed generation (DG) paradigm. This provides an opportunity for alternative energy sources, such as wind turbines, water turbines, and solar cells to be integrated into the grid. The integration of DGs into the utility grid requires power inverters to control the real power and reactive power fed into the grid, as well as regulating harmonic currents compliant with the requirements. Fig. 1 shows a typical control structure for a single-phase grid-tied inverter. One of the most important parts in the control of a power inverter is the synchronization unit which monitors magnitude, frequency, and phase of the grid voltage. When the penetration level of the grid-tied power inverter is high, accurate and robust phase detection is essential.

Several methods for phase and frequency detection of a single-phase voltage have been proposed in previous works. Sakamoto *et al.* proposed quadrature two-phase estimation by delaying the single-phase grid voltage by one quarter of a period [1]. An SRF-PLL is applied to estimate the frequency and phase of the grid. If the frequency of the grid voltage varies, a nonzero average phase error and double frequency oscillatory error will occur, significantly degrading the performance of the method.

Golestan *et al.* presented a small signal model and discussed the performance enhancement of transfer delay based PLLs [2]. The phase error can be corrected by adding a linear phase compensator [3]. The use of two cascaded $\alpha\beta$-DSC operators can effectively reject the double frequency oscillatory error. Additional cascaded $\alpha\beta$-DSC operators with appropriate delay factors can improve filtering capability in the presence of harmonic voltages [4, 5]. The method performance under DC offset was not evaluated.

Amuda *et al.* proposed inverse Park's transformation to generate orthogonal two-phase voltage [6], employing low pass filters to improve filtering capability. However, these filters have an adverse effect on dynamic response. Hadjidemetriou *et al.* proposed an improvement by using inverse Park's transformation for each harmonic component [7]. It results in better immunity to distorted harmonic voltage, but had the drawbacks of detection inaccuracy and computational burden. Ciobotaru *et al.* proposed the second-order generalized integrator (SOGI) to create orthogonal two-phase voltage [8]. The method is frequency-adaptive and capable of detecting the phase under frequency variation. The DC offset cancellation process was implemented using a low pass filter [9], although the harmonic filtering capability is compromised at high frequency. Alternatively, the DC component can be estimated and rejected by an integrator loop [10]. High order harmonic filtering capability and DC offset rejection can be improved by cascading two SOGIs [11]. Rodriguez *et al.* proposed SOGIs operating in parallel, with each unit tuned specifically for each harmonic order [12]. A fast response can be achieved, but it is sensitive to inter-harmonics or subharmonics in the grid voltage.

Fang *et al.* proposed amplitude and phase estimation

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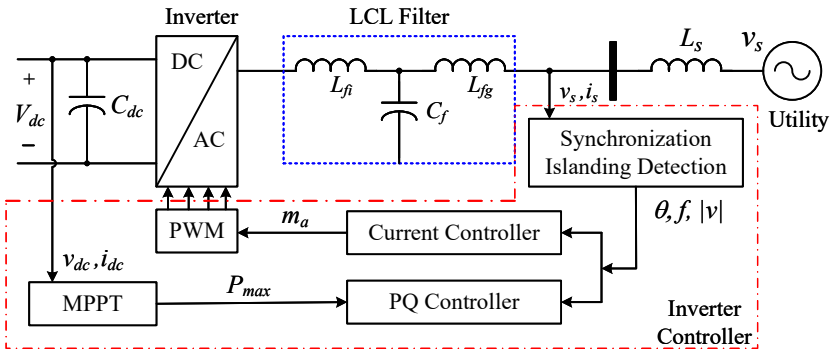


Fig. 1: *Control structure of a single-phase grid-connected inverter.*

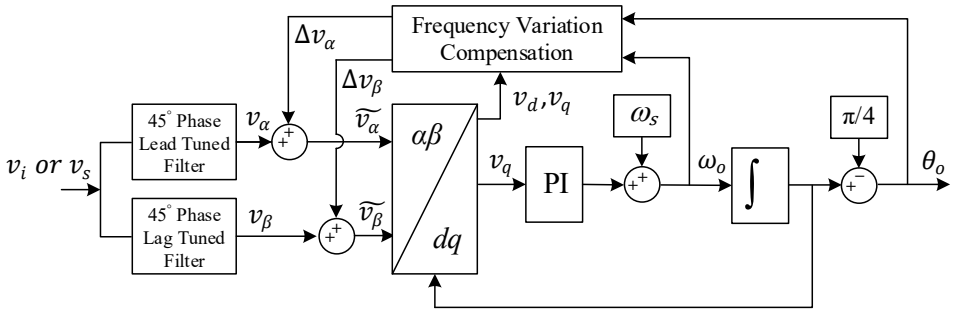


Fig. 2: *Proposed phase lead-lag SRF-PLL.*

for single-phase PLL [13]. The component orthogonal to the grid voltage is generated by utilizing the estimated amplitude and phase derived from the PLL output. In the case of a distorted harmonic voltage, amplitude and phase estimation can be implemented for each harmonic order. The method has a reasonable computational burden, while the DC offset rejection was not evaluated. Karimi-Ghartemani and Iravani proposed an enhanced single-phase PLL [14] to track the phase of the grid voltage even if phase jump occurs. In steady state, it can track the phase of the grid voltage with zero errors. In addition, the DC offset can be estimated by an integrator [10]. The detection of harmonic voltages was proposed in [15] to eliminate each harmonic component, but the computation is intensive.

As discussed, none of the solutions proposed comprehensive methods to ensure correct phase detection for practical utility grids. This paper proposes a phase lead-lag SRF-PLL. Orthogonal two-phase voltages are realized by a 45° phase-lead tuned filter and a 45° phase-lag tuned filter. In addition, frequency variation compensation is introduced to correct the estimated phase if the grid voltage frequency varies. The proposed algorithm is simple and the computation reasonable. It is robust against distorted harmonic voltage, DC offset, phase jump, and frequency variation.

This paper is organized as follows. The phase lead-lag SRF-PLL is proposed in Section 2 while the linearized model and controller design is discussed in Section 3. The feasibility of the proposed method is validated by simulation using MATLAB/Simulink in Section 4. The algorithm is implemented on a 32-bit microcontroller STM32F429ZIT6 and evaluated under six voltage conditions, while the results are discussed in Section 5. The conclusion is provided in Section 6.

2. PROPOSED PHASE LEAD-LAG SRF-PLL

The phase lead-lag SRF-PLL is proposed in Fig. 2. The single-phase grid voltage is filtered by a +45° phase-lead tuned filter and a −45° phase-lag tuned filter. Their output signals are compensated when the frequency of the grid differs from the power or nominal frequency of 50 Hz. They are fed into Park's transformation which receives the phase angle from the integrator. The quadrature-phase voltage v_q provides the phase error. It is then regulated to zero by a PI controller the output signal of which determines the frequency of the input voltage. The phase angle of the input voltage is obtained by integrating the frequency. However, the acquired phase advances the phase of the grid by +45°. It is necessary for the 45° phase to be subtracted from the integrator's output to yield the actual phase angle of the input voltage.

The basic idea of implementing +45° and −45° tuned filters is derived from a series *RLC* circuit as shown in Fig. 3. The relationship between the input voltage and the current through the *RLC* series circuit can be expressed by a transfer function in the frequency domain as

$$T(s) = k_L \frac{s}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \tag{1}$$

which for a series *RLC* circuit in Fig. 3,

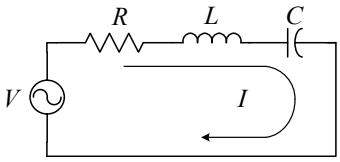


Fig. 3: *Series RLC circuit.*

$$k_L = \frac{1}{L}, \quad \omega_n = \frac{1}{\sqrt{LC}}, \quad \xi = \frac{1}{2Q}, \quad Q = \frac{1}{R}\sqrt{\frac{L}{C}},$$

where ω_n is the natural frequency, ξ is the damping ratio, and Q is the load quality factors.

2.1 45° Phase-Lead Tuned Filter

To design the phase-lead tuned filter, the relationship between the resonant frequency ω_n and the load quality factor Q must firstly be derived to achieve the unity gain and +45° phase-lead at the nominal frequency of 50 Hz. These are expressed as

$$\angle\, T(s)|_{s=j\omega_s} = \frac{\pi}{4} \tag{2}$$

$$|T(s)|_{s=j\omega_s} = 1 \tag{3}$$

where the nominal frequency is denoted by ω_s (rad/s). The natural frequency ω_n yielding the +45° phase lead at 50 Hz and the constant gain k_L yielding the unity gain can be expressed as

$$\omega_{n\alpha} = \frac{\dfrac{\omega_s}{Q_\alpha} + \sqrt{\left(\dfrac{\omega_s}{Q_\alpha}\right)^2 + (2\omega_s)^2}}{2} \tag{4}$$

$$k_{L\alpha} = \sqrt{\left(\frac{\omega_{n\alpha}^2 - \omega_s^2}{\omega_s}\right)^2 + \left(\frac{\omega_{n\alpha}}{Q_\alpha}\right)^2}. \tag{5}$$

It should be noted that the lower the chosen Q factor, the faster the tuned filter responds. However, if it is too small, the harmonic filtering capability of the tuned filter will be compromised. The tuned filter can achieve 45°phase displacement, harmonic filtering capability, and DC rejection.

2.2 45° Phase-Lag Tuned Filter

Designing the phase-lag tuned filter can be done in a similar way to the design of the phase-lead tuned filter. The achievement of the unity gain and −45° phase-lag at the power frequency 50 Hz can be satisfied by the following equations:

$$\angle\, T(s)|_{s=j\omega_s} = -\frac{\pi}{4} \tag{6}$$

$$|T(s)|_{s=j\omega_s} = 1. \tag{7}$$

Table 1: *Designed parameters.*

Parameters	Phase-Lead Tuned Filter	Phase-Lag Tuned Filter
Q	5	4
k_L	98	98
ω_n	347.14	277.33

The natural frequency and the constant gain k_L are solved and expressed as

$$\omega_{n\beta} = \frac{-\dfrac{\omega_s}{Q_\beta} + \sqrt{\left(\dfrac{\omega_s}{Q_\beta}\right)^2 + (2\omega_s)^2}}{2} \tag{8}$$

$$k_{L\beta} = \sqrt{\left(\frac{\omega_{n\beta}^2 - \omega_s^2}{\omega_s}\right)^2 + \left(\frac{\omega_{n\beta}}{Q_\beta}\right)^2}. \tag{9}$$

It is observed that the natural frequency of the phase lag tuned filter is slightly less than that of the phase lead one. The design of both filters is provided as examples in the following section.

2.3 Design Example

The phase lead and lag tuned filters are designed to satisfy phase displacement and unity gain constraints Eqs. (2), (3), (6), and (7). It is suggested that if harmonic filtering capability is of primary concern, the Q factor should be large and in a range of 4–5. This selection would result in the natural frequency being near to the nominal frequency and harmonics can be suppressed effectively, although it slows down transient response of the phase detection under sudden phase or frequency jump. If dynamic response becomes the first priority, the Q factor should be small and in a range of 0.05–0.1, though pre-filtering of harmonics may be required if the input voltage is highly distorted.

As suggested, the designed parameters are presented in Table 1. The natural frequency of the phase-lead tuned filters is slightly greater than the nominal frequency and vice versa for the phase-lag tuned filter. Fig. 4 shows frequency responses of the designed tuned filters. The unity gain and phase displacement of ±45° at the nominal frequency can be achieved. It is observed that both filters are able to evenly attenuate high-order harmonics and remove DC offset from the input voltage. The attenuation gain at the third harmonic is sufficient to effectively suppress harmonic voltage of the practical grid. For higher order harmonics, their gains proportionally decrease at a rate of −20 dB per decade. As a result, the proposed method is robust to harmonic voltage distortion as well as DC offset.

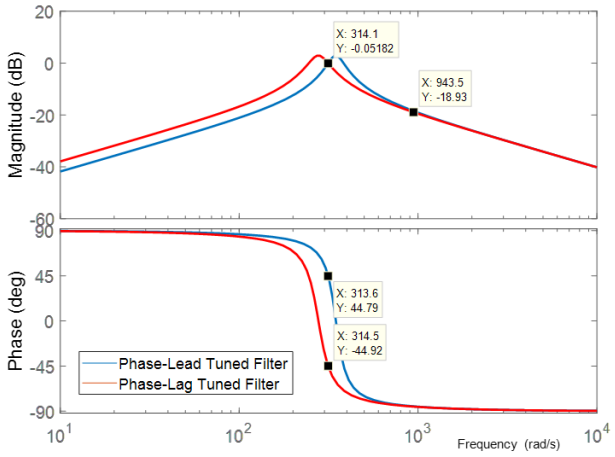


Fig. 4: *Frequency response of phase-lead and phase-lag tuned filters.*

3. LINEARIZED MODEL AND STABILITY ANALYSIS

A linearized model is derived involving Park's transformation in conjunction with phase-lead and phase-lag tuned filters. It should be noted that the effect of frequency variation compensation is not taken into consideration at the present time. For simplicity, it is assumed that the input voltage is purely sinusoidal with the nominal magnitude and frequency, defined by

$$v_i(t) = V_i \cos(\omega_i t + \phi_i) \tag{10}$$

where the voltage amplitude, frequency, and phase are denoted by V_i, ω_i and ϕ_i, respectively. After applying input voltage to both tuned filters, the orthogonal two-phase voltage v_α and v_β in Fig. 2 can be expressed as follows:

$$v_\alpha(t) = V_i \cos\left(\omega_i t + \phi_i + \frac{\pi}{4}\right) + A_\alpha \cos\left(\omega_{n\alpha}\sqrt{1-\left(\frac{1}{2Q_\alpha}\right)^2}\,t + \alpha\right) e^{-\frac{\omega_{n\alpha}}{2Q_\alpha}t} \tag{11}$$

$$v_\beta(t) = V_i \cos\left(\omega_i t + \phi_i - \frac{\pi}{4}\right) + A_\beta \cos\left(\omega_{n\beta}\sqrt{1-\left(\frac{1}{2Q_\beta}\right)^2}\,t + \beta\right) e^{-\frac{\omega_{n\beta}}{2Q_\beta}t} \tag{12}$$

where A_α, A_β are the amplitudes of the oscillating terms and α, β denote their corresponding phase shift. These are functions of V_i, ϕ_i, and Q. The oscillating terms will exponentially decay with a time constant which can be determined from roots of the characteristic equation (Eq. (1)).

Park's transformation is employed to transform the two-phase voltages v_α and v_β into the synchronous reference frame [16]. The quadrature-phase voltage v_q can be expressed as

$$v_q(t) = -v_\alpha(t)\sin(\theta_o) + v_\beta(t)\cos(\theta_o) \tag{13}$$

$$\theta_o(t) = \int \omega_o dt + \phi_o + \frac{\pi}{4} \tag{14}$$

the estimated frequency and phase are denoted by ω_o and θ_o, respectively. The mathematical expression of the transformed voltage v_q is given by

$$v_q(t) = V_i \sin((\omega_i - \omega_o)t + (\phi_i - \phi_o)) - g(t) + h(t) \tag{15}$$

where $g(t) =$

$$e^{-\frac{\omega_{n\alpha}}{2Q_\alpha}t}\left[A_\alpha \cos\left(\omega_{n\alpha}\sqrt{1-\left(\frac{1}{2Q_\alpha}\right)^2}\,t + \alpha\right)\sin\left(\omega_o t + \phi_o + \frac{\pi}{4}\right)\right]$$

and $h(t) =$

$$e^{-\frac{\omega_{n\beta}}{2Q_\beta}t}\left[A_\beta \sin\left(\omega_{n\beta}\sqrt{1-\left(\frac{1}{2Q_\beta}\right)^2}\,t + \beta\right)\cos\left(\omega_o t + \phi_o + \frac{\pi}{4}\right)\right].$$

Under a quasi-frequency locked state, the estimated frequency is nearly equal to that of the input voltage. The oscillating terms $g(t)$ and $h(t)$ will exponentially decay to zero with a time constant of $2Q/\omega_n$, while the quadrature-phase voltage $v_q(t)$ rises and approaches the steady state as approximated by

$$v_q(t) \approx V_i \sin(\phi_i - \phi_o). \tag{16}$$

If the phase error is small, the quadrature-phase voltage can be linearized based on Taylor's series as

$$v_q(t) \approx V_i(\phi_i - \phi_o). \tag{17}$$

Thus, the response due to a sudden phase jump or step phase change can be approximated by a first-order transfer function in the frequency domain as

$$\frac{V_q(s)}{\Phi_i(s) - \Phi_o(s)} = \frac{V_q(s)}{\Phi_e(s)} = \frac{V_i}{\tau s + 1} \tag{18}$$

$$\tau = \frac{2Q}{\omega_n} \tag{19}$$

where τ denotes the time constant of a tuned filter. In the case that two tuned filters have different time constants, it is suggested that the one with a slower time constant be adopted. Fig. 5 shows a linearized model of the proposed phase lead-lag SRF-PLL. The steady state effect of the input harmonics can be modeled as a disturbance using the Laplace transform,

$$V_{qh}(s) = \mathcal{L}\left\{\Sigma_{h=3,5,7,\ldots} - v_{\alpha h}\sin(\theta_o) + v_{\beta h}\cos(\theta_o)\right\} \tag{20}$$

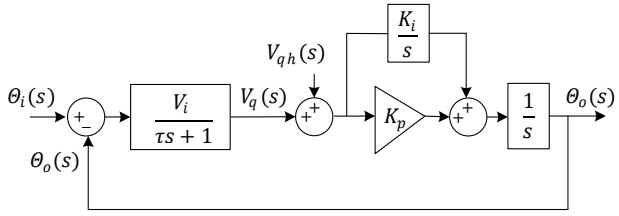


Fig. 5: *Linearized model of the proposed SRF-PLL.*

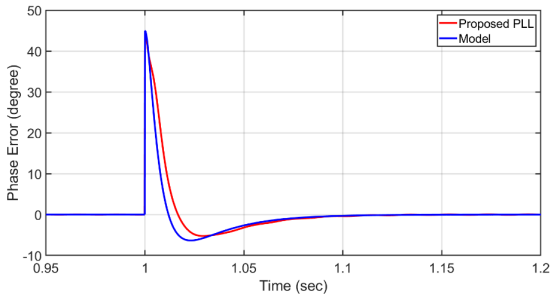


Fig. 6: *Validation of the linearized model.*

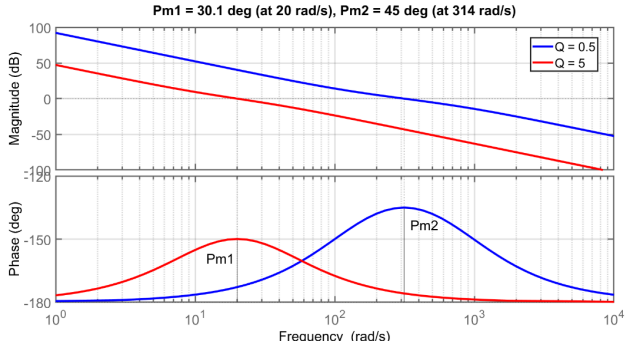


Fig. 7: *Frequency response of the open loop transfer function $G_{OL}(s)$.*

where $v_{\alpha h}$ and $v_{\beta h}$ denote the input harmonics after being attenuated by phase-lead and phase-lag tuned filters, respectively, whereas $\mathcal{L}$ denotes the Laplace operator. Fig. 6 shows the phase error response of the linearized model and the proposed SRF-PLL when a sudden phase jump of 45° occurs. The linearized model yields nearly comparable dynamic behavior to the proposed SRF-PLL. Thus, it can be used to design controller gains and guarantee stability.

If the effect of the disturbance is ignored, the open loop transfer function with the normalized input voltage can be expressed as

$$G_{OL}(s) = \frac{\Phi_o(s)}{\Phi_e(s)}\bigg|_{V_{qh}(s)=0} = K_I \frac{(\tau_z s+1)}{s^2(\tau_p s+1)} \tag{21}$$

where $\tau_p = 2Q/\omega_n$ and $\tau_z = K_p/K_I$. It has double poles at the origin and one pole ($p = -1/\tau_p$) and one zero ($z = -1/\tau_z$) on the left half-plane. A zero-pole pair in Eq. (21) can provide a phase boost in the same way as a typical phase-lead controller. Based on the symmetrical optimum method [17], maximum phase boost can be achieved at the gain crossover frequency given as

Table 2: *PI controller parameters.*

	$Q = 5$	$Q = 0.5$
K_P	25	314
K_I	360.2	40 882
PM	30°	45°
ω_{cf}	25	314

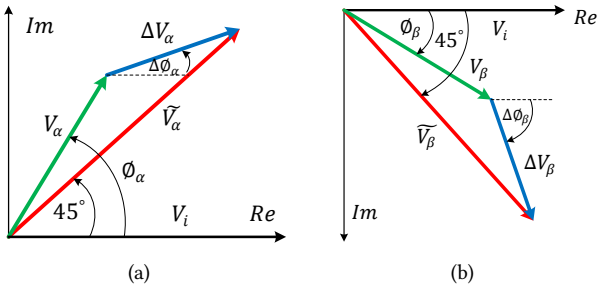


Fig. 8: *Phasor of the input voltage after filtering by the tuned filters (a) phase-lead voltage and (b) phase-lag voltage.*

$$\omega_{cf} = \frac{1}{\sqrt{\tau_z \tau_p}} \tag{22}$$

whereas, proper selection of the PI controller gains is obtained by

$$K_P = \omega_{cf}, \tag{23}$$

$$K_I = \tau_p K_p^3. \tag{24}$$

Fig. 7 shows the frequency response of the open loop transfer function with the load factor Q equal to 0.5 and 5. The PI controller gains are given in Table 2. It should be noted that the high load factor Q results in a low bandwidth and better harmonic filtering capability but the slow response is a trade-off.

A good compromise could be achieved when the load factor Q is about 0.5. A good stability margin should then be obtained with a phase margin of 45° at the crossover frequency of 314 rad/s.

It is worthwhile mentioning that the transfer function Eq. (21) has double poles. It is classified as a Type-II system and capable of tracking a step phase or step frequency change with zero steady state error, although a constant phase error exists while it tracks a frequency ramp.

4. FREQUENCY VARIATION COMPENSATION

With the practical grid, power frequency may vary slightly from 50 Hz, potentially causing phase displacement and loss of magnitude in both tuned filters unequal to 45° and unity, respectively. Fig. 8(a) shows a phasor of the input voltage after being filtered by the phase-lead tuned filter. Its magnitude differs from that of the input voltage and a phase shift of 45° can no longer be achieved.

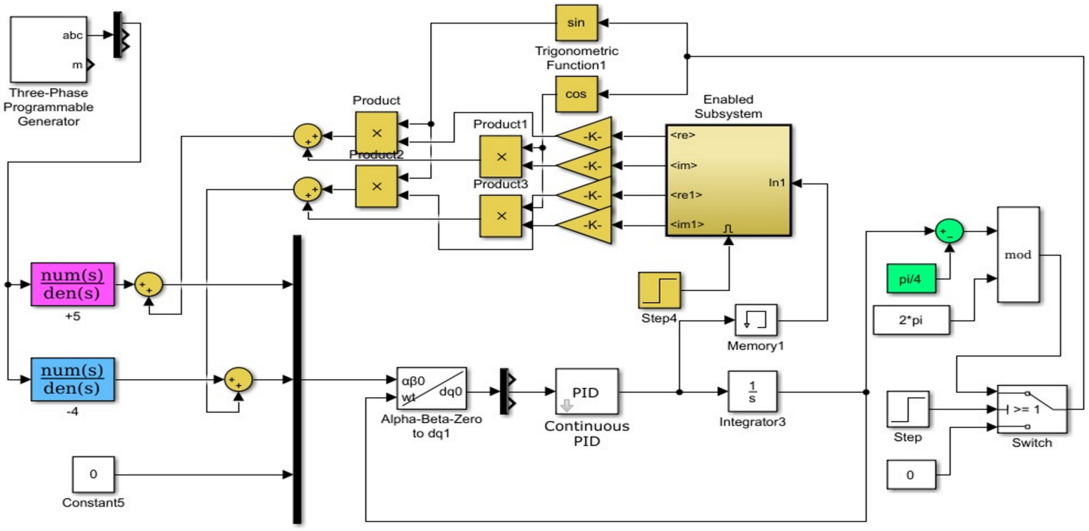


Fig. 9: *Simulation block diagram using MATLAB/Simulink.*

In order to correct the magnitude and phase, the error voltage phasor ΔV_α is added vectorially to the phasor of the phase-lead voltage V_α. The compensated phase-lead voltage $\widetilde{V_\alpha}$ can be expressed as

$$\widetilde{V_\alpha} = V_\alpha + \Delta V_\alpha. \tag{25}$$

Let the phase-lead voltage v_α and the error voltage Δv_α be expressed in the following sinusoidal functions:

$$v_\alpha = |V_\alpha| \sin(\omega_i t + \phi_\alpha) \tag{26}$$

$$\Delta v_\alpha = |\Delta V_\alpha| \sin(\omega_i t + \Delta\phi_\alpha) \tag{27}$$

$$\Delta v_\alpha = \mathrm{Re}\left\{|\Delta V_\alpha| e^{j\Delta\phi_\alpha}\right\} \sin(\omega_i t) + \mathrm{Im}\left\{|\Delta V_\alpha| e^{j\Delta\phi_\alpha}\right\} \cos(\omega_i t) \tag{28}$$

where ω_i is an instantaneous value of the input frequency obtained from the phase detector. Their expressions for the real and imaginary parts are given as

$$\mathrm{Re}\left\{|\Delta V_\alpha| e^{j\Delta\phi_\alpha}\right\} = |V_i| \left(\frac{1}{\sqrt{2}} - \left| \frac{\omega_i k_{L\alpha}}{\left(\omega_{n\alpha}^2 - \omega_i^2\right) + j\frac{\omega_{n\alpha}\omega_i}{Q_\alpha}} \right| \cos(\phi_\alpha) \right)$$

$$\mathrm{Im}\left\{|\Delta V_\alpha| e^{j\Delta\phi_\alpha}\right\} = |V_i| \left(\frac{1}{\sqrt{2}} - \left| \frac{\omega_i k_{L\alpha}}{\left(\omega_{n\alpha}^2 - \omega_i^2\right) + j\frac{\omega_{n\alpha}\omega_i}{Q_\alpha}} \right| \sin(\phi_\alpha) \right) \tag{29}$$

Fig. 8(b) shows a phasor of the phase-lag voltage. Its magnitude and phase need to be corrected in a similar manner to that previously mentioned. The compensated phase-lag voltage phasor $\widetilde{V_\beta}$ can be expressed as

$$\widetilde{V_\beta} = V_\beta + \Delta V_\beta \tag{30}$$

$$\Delta v_\beta = \left|\Delta V_\beta\right| \sin\left(\omega_i t + \Delta\phi_\beta\right) \tag{31}$$

$$\Delta v_\beta = \mathrm{Re}\left\{\left|\Delta V_\beta\right| e^{j\Delta\phi_\beta}\right\} \sin(\omega_i t) + \mathrm{Im}\left\{\left|\Delta V_\beta\right| e^{j\Delta\phi_\beta}\right\} \cos(\omega_i t) \tag{32}$$

where ω_i is the frequency value of the input voltage obtained from the phase detector. Their expressions for the real and imaginary parts are given as

$$\mathrm{Re}\left\{\left|\Delta V_\beta\right| e^{j\Delta\phi_\beta}\right\} = |V_i| \left(\frac{1}{\sqrt{2}} - \left| \frac{\omega_i k_{L\beta}}{\left(\omega_{n\beta}^2 - \omega_i^2\right) + j\frac{\omega_{n\beta}\omega_i}{Q_\beta}} \right| \cos(\phi_\beta) \right)$$

$$\mathrm{Im}\left\{\left|\Delta V_\beta\right| e^{j\Delta\phi_\beta}\right\} = |V_i| \left(\frac{1}{\sqrt{2}} - \left| \frac{\omega_i k_{L\beta}}{\left(\omega_{n\beta}^2 - \omega_i^2\right) + j\frac{\omega_{n\beta}\omega_i}{Q_\beta}} \right| \sin(\phi_\beta) \right) \tag{33}$$

The input voltage magnitude can be calculated as follows:

$$|V_i| = \sqrt{v_d^2 + v_q^2} = \sqrt{v_\alpha^2 + v_\beta^2} \tag{34}$$

In the event that the input voltage does not vary widely, its magnitude can be approximated by the nominal voltage.

5. SIMULATION RESULTS

The feasibility of the proposed method is verified by computer simulation. Fig. 9 shows a block diagram implemented on MATLAB/Simulink. Six different voltage scenarios, i.e., normal, distorted harmonic, DC offset, frequency variation, phase jump, and frequency jump are simulated and the results illustrated.

Fig. 10(a) shows the waveforms of the voltages for the ideal grid, phase-lag, and phase-lead. The estimated phase angle catches up with the reference phase in less than half a period. Fig. 10(b) shows the distorted harmonic voltage, containing 5 percent of the third harmonic voltage. It is attenuated effectively by the phase-lead and phase-lag tuned filters while their magnitude and phase are correctly preserved. The method can precisely track

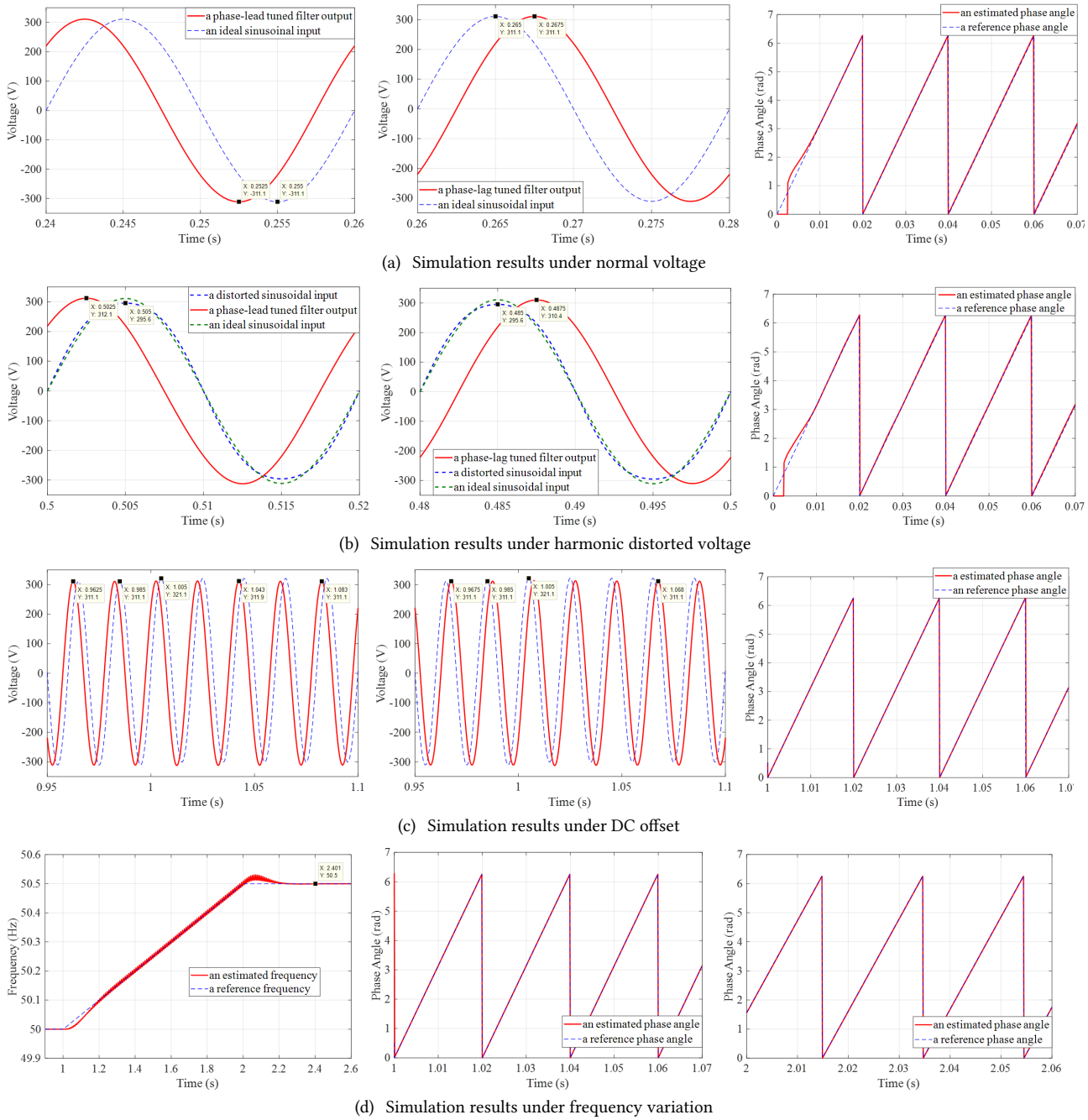
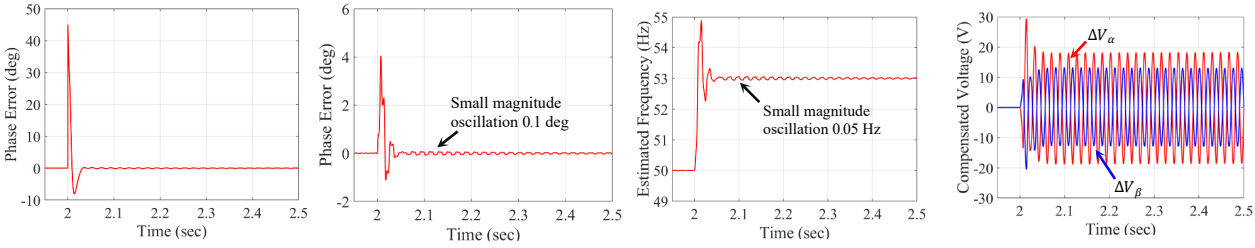


Fig. 10: *Simulation results under four different voltage scenarios.*

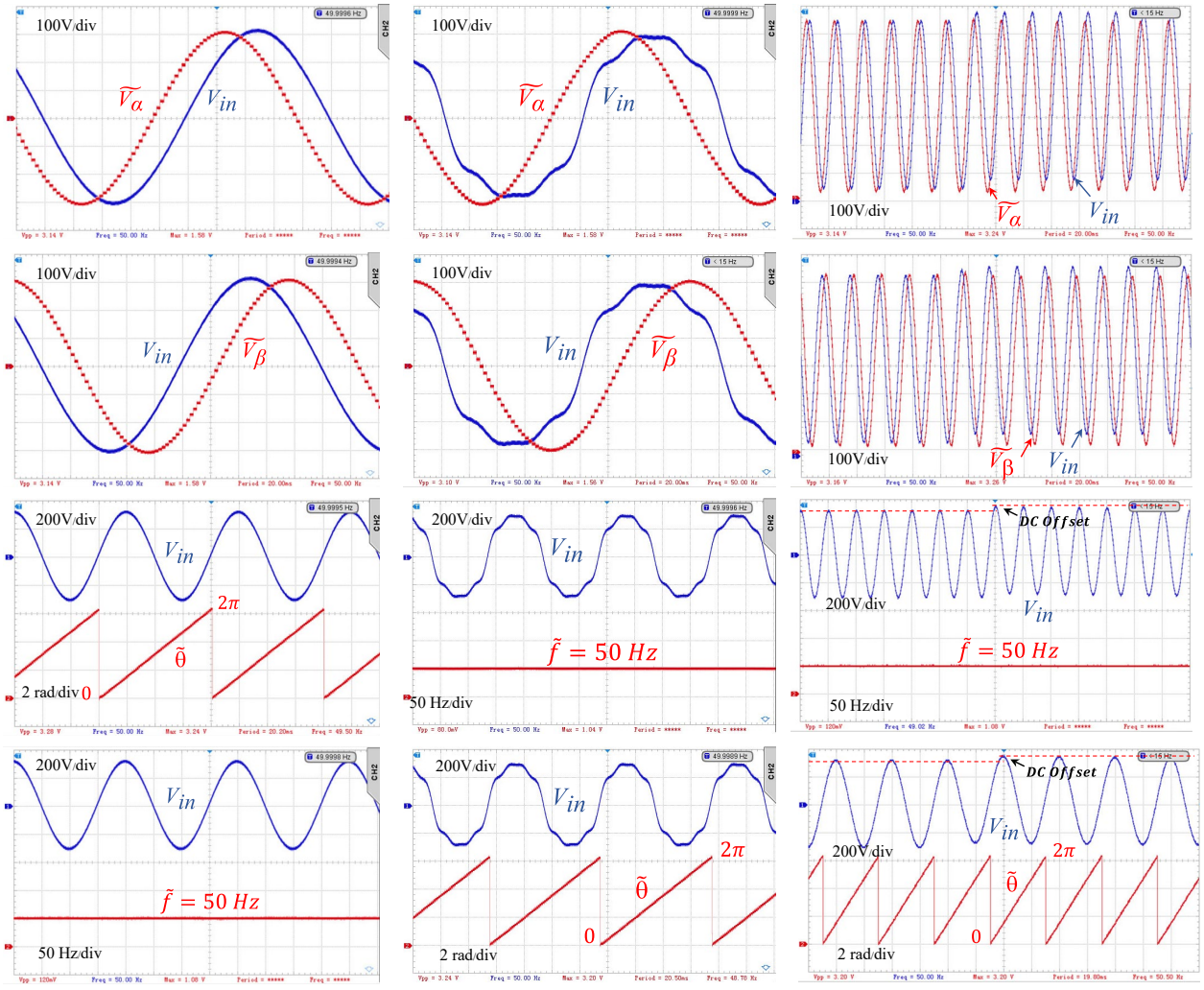
the phase of the grid. Fig. 10(c) shows waveforms of the grid voltage superimposed by 10 V DC offset at time 1.0 s. It disturbs the frequency slightly but has a noticeable effect on the estimated phase. Fig. 10(d) shows the grid voltage, the frequency of which changes slowly from 50 Hz to 50.5 Hz over a short period of time from 1 to 2 s. While frequency variation occurs, the proposed method can track the reference frequency, though there is a small magnitude of oscillation present on the estimated frequency. It does not cause any significant effect on the estimated phase because it is filtered out by the low bandwidth integrator. At the beginning of frequency variation at time 1.0 s, the phase of the grid voltage can be estimated since it is essentially identical to the reference phase. After the frequency remains constant at 50.5 Hz, the estimated phase correctly tracks the reference phase.

In Fig. 11(a), when a sudden phase jump of +45° occurs, the phase error abruptly rises to +45°, before rapidly returning to zero within two cycles with a small undershoot of 6°. Fig. 11(b) shows the response of the phase error and estimated frequency under a frequency jump of +3 Hz. The frequency variation compensation can correct the magnitude and phase of the phase-lead and phase-lag voltage. The zero phase error and accurate frequency estimation can be achieved within two cycles. A small magnitude of oscillation subsequently takes place



(a) Sudden phase jump +45° (b) Sudden frequency jump +3 Hz

Fig. 11: *Simulation results under (a) sudden phase and (b) frequency jumps.*



(a) (b) (c)

Fig. 12: *Experimental results of voltage, estimated frequency, and phase angle under (a) normal voltage, (b) distorted harmonic voltage, and (c) voltage with DC offset.*

on the estimated phase and frequency at a magnitude of 0.1° and 0.05 Hz, respectively, but will decay to near zero in half a second.

6. EXPERIMENTAL RESULTS

The proposed method is implemented on a 32-bit microcontroller STM32F429ZIT6 and the algorithm executed repeatedly at 4 kHz. The input voltage is sampled via an ADC module and digitally filtered by the phase-lead and phase-lag tuned filters. Fig. 12(a) shows the triangular waveform phase of the grid voltage under normal voltage. At zero crossing, the phase counter is reset to zero. It then increases by 4.5 degrees with every step. Until the counter reaches 80, it is reset to zero and begins to count the phase for the next cycle. Fig. 12(b) shows a severely distorted waveform of the grid

voltage. It contains 10% of the third harmonic voltage, 7% of the fifth harmonic voltage, and 5% the seventh harmonic voltage. Despite the presence of harmonics, the method can detect the frequency and phase of the grid voltage correctly. The detected phase linearly increases and coincides with the fundamental component phase of the distorted grid voltage. Fig. 12(c) shows the grid voltage; superimposed instantly by the 10 V DC offset. Due to the nature of the capacitor in a series *RLC* circuit, the DC offset is blocked or quickly attenuated. Thus, the phase of the grid voltage can be detected precisely and seamlessly.

7. CONCLUSION

The phase lead-lag SRF-PLL is proposed in this paper to synchronize the grid of a single-phase inverter. The analysis and design example of the phase-lead and phase-lag tuned filters and phase detection algorithm have also been presented. The linearized model and controller design used to achieve good stability margin were discussed. The magnitude and phase compensation were detailed due to the frequency variation. Viability of the method was verified by the simulation based on MATLAB/Simulink platform. The algorithm was implemented on a 32-bit microcontroller and tested under various voltage conditions. According to the simulation and experimental results, it can be confirmed that the proposed method is robust and capable of accurately detecting the phase of the practical grid.

At the time of publication, the effect of the frequency variation compensation on the estimated quadrature-phase voltage and control loop stability is being investigated and the analysis results will be presented in a future paper.

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