Development of Open Switch Fault-Tolerant Capability in CCS-MLI Topology

Dhananjay Kumar[1†], **Rajesh Kumar Nema**[1],
Sushma Gupta[1], and **Niraj Kumar Dewangan**[2], Non-members

ABSTRACT

Multilevel inverters (MLIs) are very popular in renewable energy applications and other DC to AC conversion systems due to their reliability, reduced voltage stress, low total harmonic distortion (THD), reduced filter size, low electromagnetic interference, etc. Consequently, the photovoltaic (PV) generation systems, mainly installed in remote areas, require highly reliable systems. The high failure rate of sources and power semiconductor devices results in very low reliability for inverters used in PV generation systems. The aim of this study is to develop a five-level MLI topology with fault-tolerant (FT) characteristics. Therefore, a highly resilient fault-tolerance topology, based on a cross-connected source-based MLIs (CCS-MLI) structure, is proposed in this paper. The developed CCS-MLI topology can tolerate open switch faults in any single switch failure. The proposed system and results developed in a MATLAB/Simulink environment are discussed under normal and faulty states. The simulation results are validated experimentally. Finally, the quantitative and qualitative superiority of the proposed CCS-MLI is demonstrated through the comparative analysis of other recent topologies.

Keywords: Cross-Connected Source, Fault-Tolerant, Multilevel Inverter, Photovoltaic, Reliability, Total Harmonic Distortion

1. INTRODUCTION

In the current scenario, due to environmental issues and limited fossil fuel systems, renewable energy is gaining significant attention. Solar, fuel cells, and wind energy systems are being widely discussed among researchers and industrial communities in an attempt to reduce dependence on varying environmental conditions [1]. Nowadays, the continuous enhancement of semiconductor devices for photovoltaic (PV) cells has resulted in increased efficiency and extensive usage of PV systems [2, 3]. The configuration of a PV generation system equipped with the MLI is shown in Fig. 1.

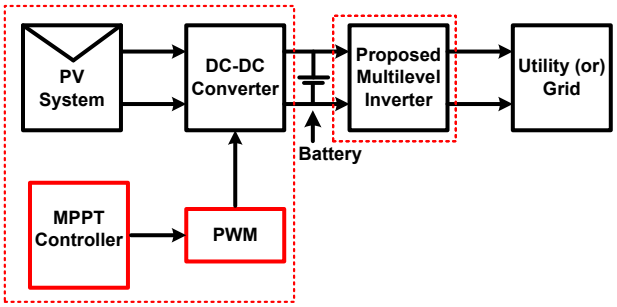

***Fig. 1**: Schematic diagram of a PV generation system equipped with the MLI.*

The inclusion of an MLI in the PV system has several benefits, such as (i) the low voltage stress on switches corresponds to the operating voltages and (ii) the harmonic profile is better than that of a conventional two-level inverter [4]. The obligatory need for a high-quality power supply has recently brought the multilevel inverter into the limelight. Basically, MLIs can be classified into three types: neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge multilevel (CHB) MLI [5]. Among these traditional topologies, the CHB is the most popular because of its modularity and easy extension for higher voltage requirements [6]. However, traditional CHBs are currently facing challenges due to the significant increase in the number of power semiconductor devices.

Nowadays, the focus is on reducing the number of devices to create the same voltage level as in traditional topologies. To overcome these challenges, several new topologies have recently been proposed, such as reduced device count MLIs (RDC-MLIs) [7 8], which minimize the conduction losses in the system, reducing the overall system cost. In addition, the harmonic profile of the system can be enhanced with different pulse width modulation techniques. Several emerging structures of the multilevel inverter with FT ability have recently been introduced in RDC-MLI [9]. Fault-tolerant MLIs require multiple switching states capable of realizing the same level of inverter output. Such multiple switching states in the literature are termed "redundant states" [10]. The RDC-MLI would certainly be less likely to become a full fault-tolerant topology due to the availability of fewer "redundant states". The redundant path can then be

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[1]The authors are with the Department of Electrical Engineering, Maulana Azad National Institute of Technology, Bhopal, India.

[2]The author is with the Department of Electrical Engineering, National Institute of Technology, Raipur, India.

[†]Corresponding author: dhananjaymanit23@gmail.com

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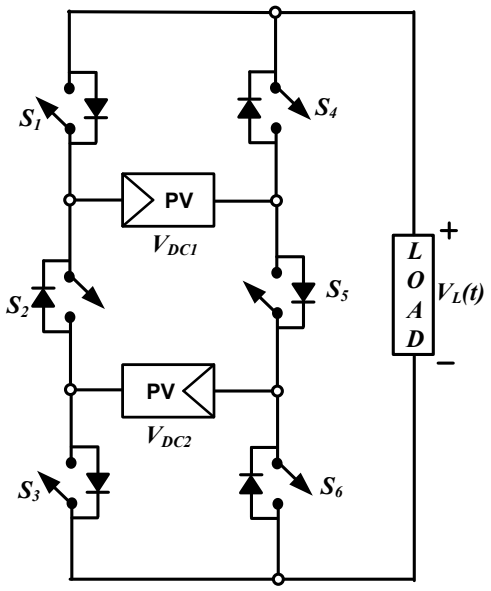


***Fig. 2**: A single-phase five-level traditional CCS-MLI topology as proposed in [9].*

realized by the addition of one or more power devices in series/parallel to the existing RDC-MLI topologies.

Recent topologies proposed for fault-tolerance (FT) in the RDC-MLI configuration [10, 11] are not suitable for capacitor charge balance due to their symmetric shape. The topologies presented in [12, 13] propose zero use of the DC sources associated with faulty cells. The recent topology of the MLI appears to be aimed at FT capability, with various solutions proposed [14–17]. Although the use of power electronic converters is becoming widespread, the reliability of power electronics has also increased [18–21]. Recent research indicates that reliability is the main concern in power electronics converters. The power switch is the most delicate part, resulting in low MLI reliability and system malfunctions.

Since FT topology can be used on all switches, the proposed inverter topology can offer certain advantages. It can tolerate an open-switch fault caused by the failure of any single switch in the proposed CCS-MLI topology. This configuration is more effective at reducing the number of switching devices than the traditional five-level MLIs.

This paper is organized as follows: the CCS-MLI operating principle of the proposed topology is presented in Section 2. Section 3 provides details of the switching scheme design for the MLI during normal and FT conditions. It also discusses the modulation scheme, Simulink results, and the proposed CCS-MLI topology. Section 4 presents the experimental validation of the proposed CCS-MLI topology, while Section 5 presents a quantitative and qualitative comparative analysis of the proposed CCS-MLI topologies. Finally, the conclusions of the paper are summarized in Section 6.

***Table 1**: Valid switching state for traditional cross-connected source-based MLIs [9].*

State	Switching Combination (On state)	$V_L(t) = V_o(t)$ $[E_1 = E_2 = V_{dc}]$
α_0	S_1, S_5, S_3	$E_1 + E_2 = 2V_{dc}$
α_1	S_1, S_5, S_6	$+E_1 = +V_{dc}$
α_2	S_4, S_5, S_3	$+E_2 = +V_{dc}$
α_3	S_1, S_2, S_3	0
α_4	S_4, S_5, S_6	0
α_5	S_4, S_2, S_3	$-E_1 = -V_{dc}$
α_6	S_1, S_2, S_6	$-E_2 = -V_{dc}$
α_7	S_4, S_2, S_6	$-E_1 - E_2 = -2V_{dc}$

***Table 2**: Analysis of any single switch failure in CCS-MLI.*

Failed Switch	Available States	Number of Levels in Output
S_1	$\alpha_2, \alpha_4, \alpha_5, \alpha_7$	Three-level
S_2	$\alpha_0, \alpha_1, \alpha_2, \alpha_4$	Shutdown
S_3	$\alpha_1, \alpha_4, \alpha_6, \alpha_7$	Three-level
S_4	$\alpha_0, \alpha_1, \alpha_3, \alpha_6$	Three-level
S_5	$\alpha_3, \alpha_5, \alpha_6, \alpha_7$	Shutdown
S_6	$\alpha_0, \alpha_2, \alpha_3, \alpha_5$	Three-level

2. OPERATING PRINCIPLE OF THE PROPOSED CCS-MLI TOPOLOGY

In this research, a CCS-MLI with fault-tolerance capability is proposed, representing the modification of the topology contained in [9]. The traditional CCS-MLI structure is illustrated in Fig. 2, constituting two symmetrical DC source and six semiconductor switches.

The FT strategy in the proposed CCS-MLI topology can be classified into three types: (i) switch-level, (ii) module-level, and (iii) system level. In this CCS-MLI topology, despite a reduction in the semiconductor device count, failure in any single device may cause the overall system to shut down and take longer to return to a healthy condition. Due to these limitations, the traditional CCS-MLI topology needs a fault-tolerance strategy to maintain continuous operation by supplying power to the load.

The different switching configurations of the traditional CCS-MLI topology, namely α_i ($i = 0, 1, 2, 3, 4, 5, 6, 7$), are shown in Table 1.

An analysis of the open circuit fault(s) with any single switch failure in the traditional CCS-MLI topology is presented in Table 2. If one switch in the group S_1, S_3, S_4 and S_6 encounters a failure (OC fault), the topology can continue to operate with a three-level output voltage. On the other hand, if the switch S_2 or S_5 undergoes an OC fault, then no operating MLI states will allow the synthesis of output voltage across the load, and the corresponding condition will be equivalent to a shutdown.

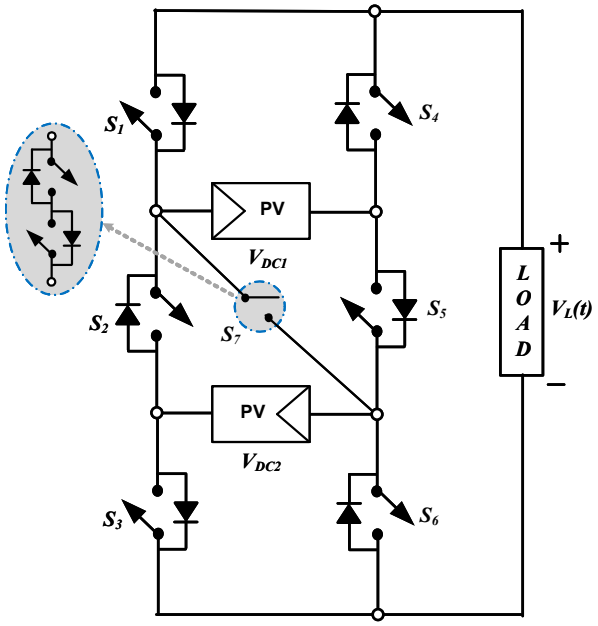


***Fig. 3**: Proposed single-phase five-level fault-tolerant CCS-MLI topology.*

Therefore, the traditional CCS-MLI topology requires a fault-tolerance feature to obstruct the output for faults in the switches. An additional bidirectional switch S_7 is added to the traditional CCS-MLI to obtain the proposed single-phase five-level CCS-MLI topology with the fault-tolerance feature as shown in Fig. 3. With this modification, the number of redundant "switching-states" also increases. Each switching state in the proposed CCS-MLI topology synthesizes one output level and consolidates all such levels, producing five-level periodic outputs across the load.

Although various switching states for the proposed fault-tolerant CCS-MLI topology can be explored, this paper focuses on the MLI topology and the energy balancing technique between source and load. The various switching combinations for the available level-formation in the case of an open switch fault are shown in Table 3.

According to Table 3, if any one of the switches S_2 and S_5 encounters a failure, the power conversion still continues with reduced voltage levels (*from five-level to three-level*) and reduced magnitude in output voltage and load current.

3. SIMULATION RESULTS

The fault-tolerant CCS-MLI topology simulation studies were performed using MATLAB /Simulink software. The gate pulse generation for the switches was provided by a multicarrier sinusoidal PWM (SPWM) scheme. Since the carrier waveforms in the level-shifted carrier PWM (LSC-PWM) do not have phase displacement on each other, the lower voltage spectra were improved with lower THD than for the phase-shifted carrier PWM (PSC-PWM). The level-shifted carrier PWM was used in the proposed modulation scheme for the generation of

***Table 3**: Required switching combination for the available level-formation in the case of open switch fault in S_2 and S_5.*

	Switching Combination (On state)	Voltage Level	Number of Levels in Output
If open circuit fault occurs in S_2	S_4, S_5, S_6	0	Three-level
	S_1, S_7, S_6		
	S_1, S_5, S_6	$+V_{dc}$	
	S_1, S_7, S_3		
	S_4, S_7, S_6	$-V_{dc}$	
If open circuit fault occurs in S_5	S_1, S_2, S_3	0	Three-level
	S_1, S_7, S_6		
	S_1, S_7, S_3	$+V_{dc}$	
	S_4, S_7, S_6	$-V_{dc}$	
	S_1, S_2, S_6		

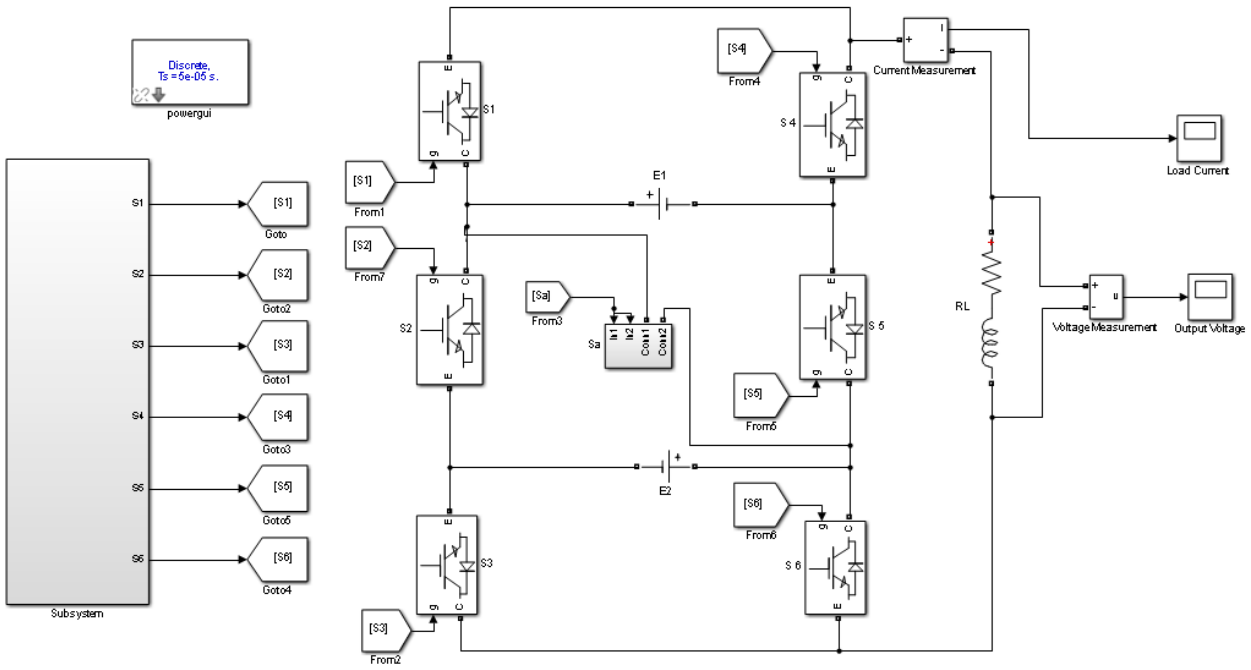
***Table 4**: Simulation and experimental parameters of the proposed CCS-MLI topology.*

Parameters	Value
Input DC source ($E_1 = E_2$)	48 V
Power switch (S_1–S_7)	GW30NC120HD
Gate driver circuit	M57962L
Modulating wave frequency (f_m)	50 Hz
Switching frequency (f_s)	3000 Hz
Modulation index (m_a)	0.85
Load resistance (R)	20 Ω
Inductance value (L)	20 mH

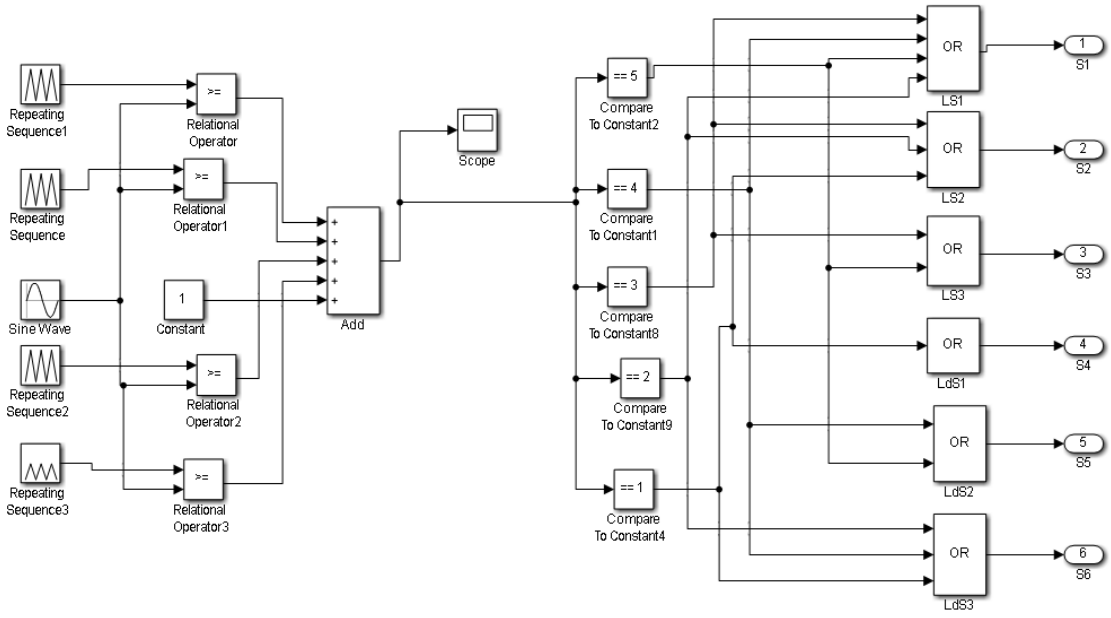
gate pulse. Using the multicarrier SPWM strategy, the triangular carrier signal was compared to the sinusoidal reference signal and the received pulses. Therefore, the control signal for the power semiconductor switches was used to obtain the suitable multilevel PWM waveform [5, 9]. For better understanding, the MATLAB/Simulink block of the five-level CCS-MLI topology is shown in Fig. 4(a), while the control scheme is illustrated in Fig. 4(b).

A schematic diagram of the modulation control strategy is shown in Fig. 5(a). The corresponding reference and level shifted carrier PWM (LSC-PWM) waveform are shown in Fig. 5(b). The modulation index (m_a) of 0.85 and the modulating wave frequency (f_m) of 50 Hz were used for both simulation and experimentation. For five-level waveforms, four triangular carriers at a frequency (f_c) of 3000Hz were used as carrier signals and established in the level-shifted carrier PWM (LSC-PWM). To examine the performance of the proposed CCS-MLI topology, it is simulated using MATLAB/Simulink, and demonstrated experimentally through an RL load of $R = 20\,\Omega$ and $L = 20$ mH. The simulation and experimental parameters for the proposed fault-tolerant CCS-MLI topology are presented in Table 4.

The proposed fault-tolerant CCS-MLI topology, simulated waveforms, output voltage, and output current



(a)



(b)

Fig. 4*: MATLAB/Simulink blocks: (a) proposed single-phase five-level fault-tolerant CCS-MLI topology; and (b) control strategy.*

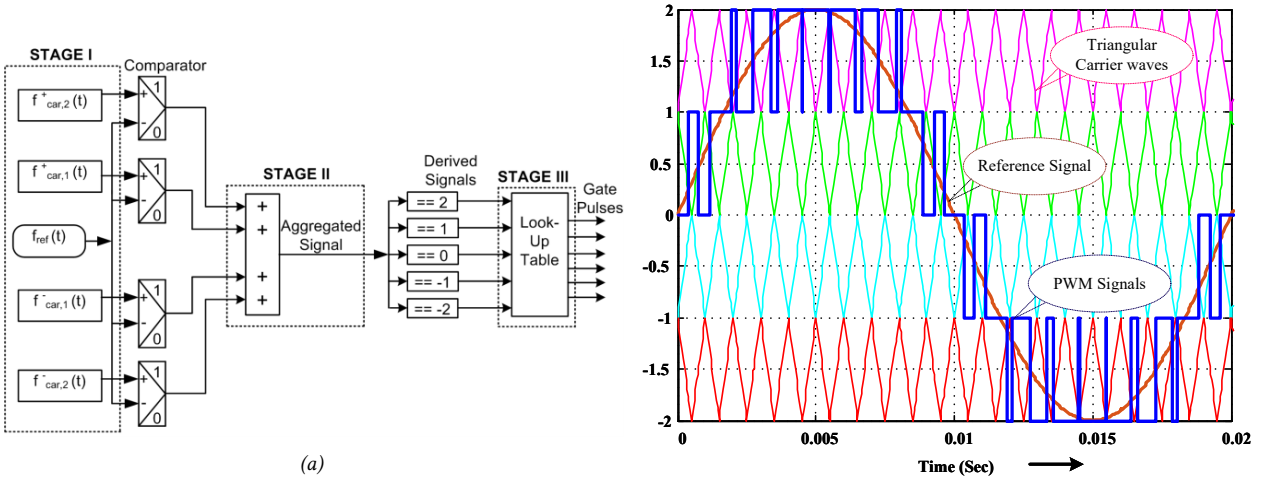
waveforms through the *RL* load are shown in Fig. 6. The output voltage waveform is expected to be five-level under healthy state conditions.

Fig. 6 also shows the output voltage and load current waveform for all CCS-MLI conditions: (i) Healthy state for $t < 0.94$ s, (ii) Faulty state for $t > 0.94$ s, and (iii) Fault cleared state for $t = 1$ s. In the event of an open-circuit fault occurring at $t = 0.94$ s in switches S_1, S_2, S_3, S_4, S_5 and S_6 , the fault-tolerant capability of the proposed CCS-MLI topology reduces from a five-level to a three-level output with a simultaneous reduction in peak magnitude.

The simulation results show that the proposed fault-tolerant CCS-MLI topology can be reconfigured to obtain a fault-tolerant structure in open-switch fault conditions.

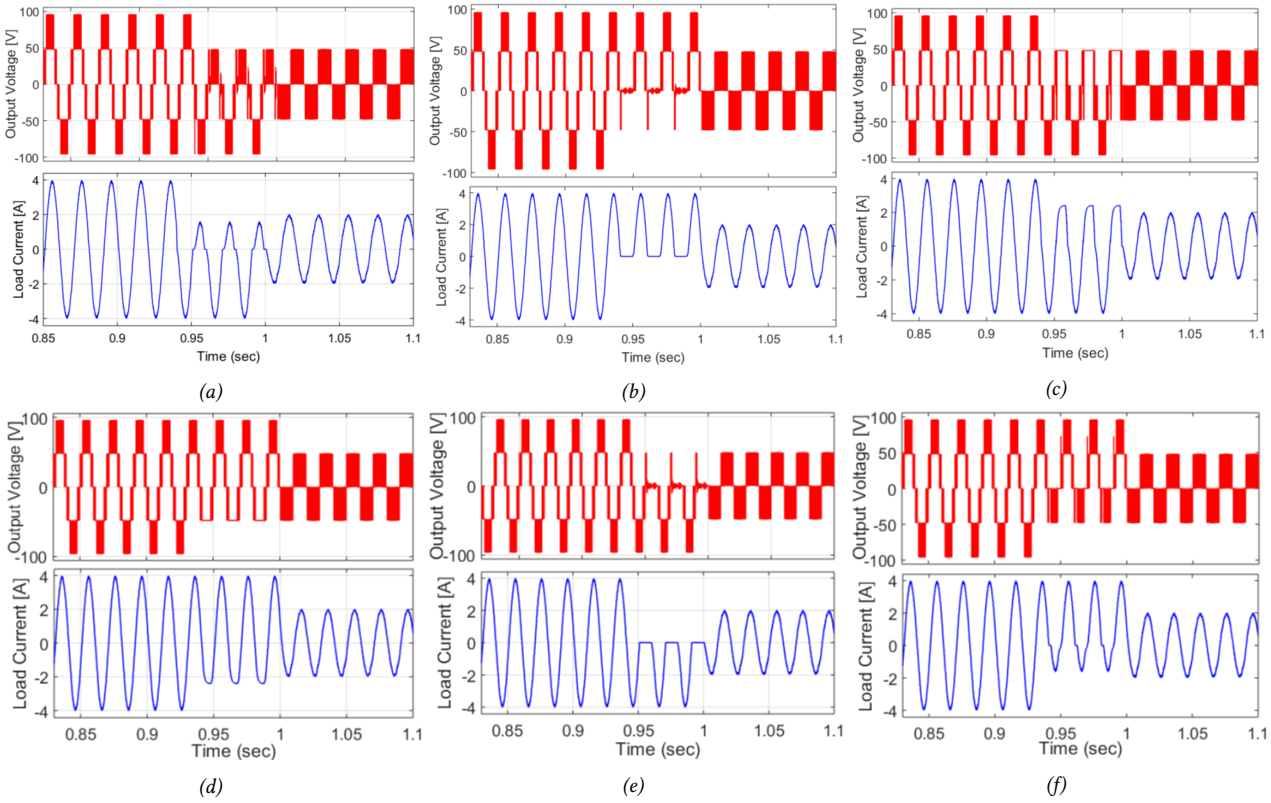
4. EXPERIMENTAL VALIDATION

A prototype has been developed experimentally to validate the performance of the proposed five-level



(a) (b)

***Fig. 5**: (a) A schematic diagram of the modulation control strategy; and (b) reference and LSC-PWM carrier technique waveform with $m_a = 0.85$.*



(a) (b) (c) (d) (e) (f)

***Fig. 6**: Simulation results under healthy state, faulty state, and fault cleared state conditions when an open switch fault occurs in (a) S_1, (b) S_2, (c) S_3, (d) S_4, (e) S_5, and (f) S_6.*

CCS-MLI topology. Fig. 7 shows a snapshot of the experimental setup and control signals for discrete power switching modules (with appropriate gate drives and IGBTs) generated using dSPACE (DS-1104), which acts as a real-time controller and an interface with the MATLAB/Simulink model in the host PC. All the waveforms in the experimental results were recorded and measured with the help of a ScopeCorder YOKOGAWA DL750E.

The experimental output voltage and load current waveforms through the *RL* load for the proposed topology are illustrated in Fig. 8. All operating conditions (healthy state, faulty state, and post fault) in switches S_2 and S_5 of the proposed MLI were examined for fault-tolerance in the experiment.

The waveform shows the five-level voltage and almost

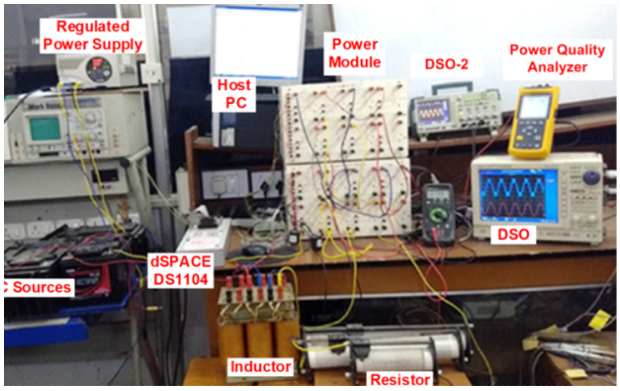
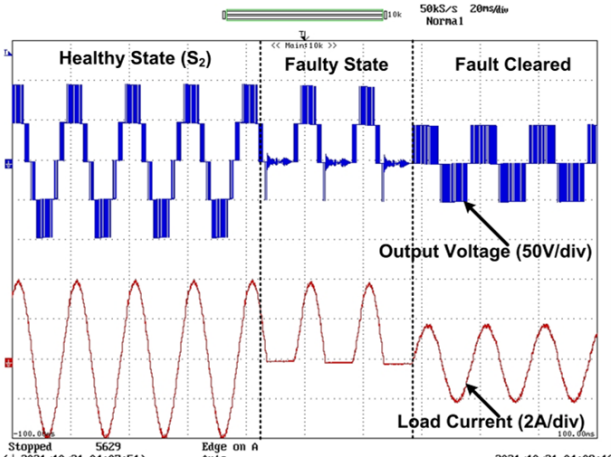
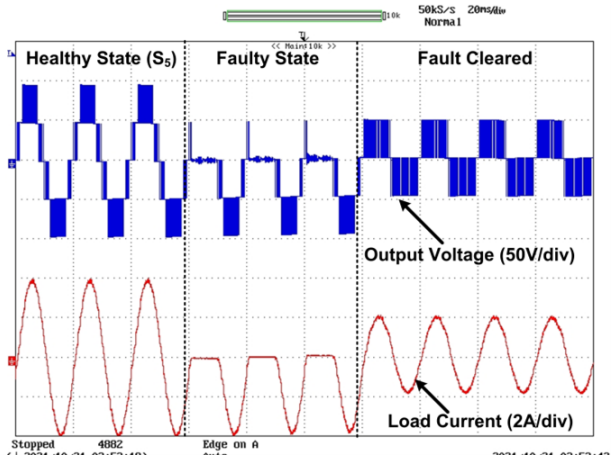


***Fig. 7**: Snapshot of the experimental setup.*



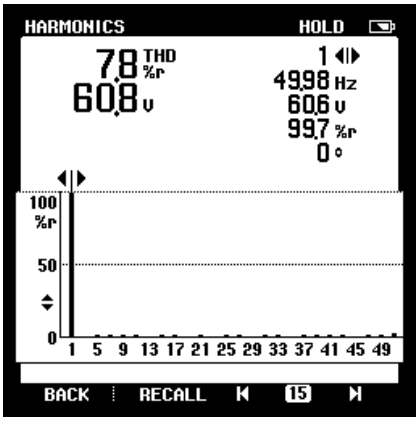
(a)



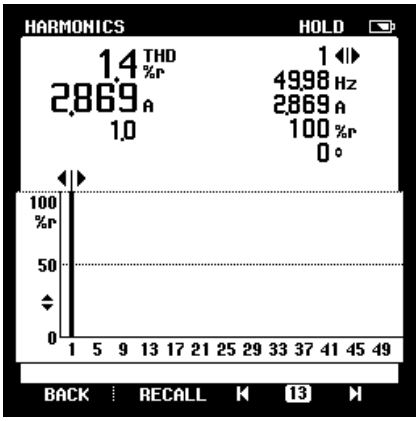
(b)

***Fig. 8**: Experimental results for the proposed CCS-MLI topology. Output voltage (50 V/div) and load current (2 A/div) waveforms under healthy state, faulty state, and fault cleared state: (a) S_2 open circuit fault and (b) S_5 open circuit fault at 3 kHz.*

sinusoidal load current waveform. The experimental results for rated output voltage indicate that the proposed CCS-MLI topology equates to 96 V at the frequency of 50 Hz as shown in Fig. 8 prior to the open switch fault condition. Under healthy operating conditions this topology voltage waveform was five-level, demonstrating the *RL* nature of the current waveform load.



(a)



(b)

***Fig. 9**: Experimental results for the proposed CCS-MLI topology under healthy conditions: (a) output voltage THD spectrum and (b) current THD spectrum.*

Moreover, sometime after the fault was initiated, the voltage changed from five to three-level, as shown in Fig. 8, and further exhibited a decrease in voltage and current magnitude. The results prove that after the fault, the inverter for the load voltage reconfigured to operate with a three-level output voltage. The operating output voltage decreased along with the current magnitude. It can be verified that the proposed CCS-MLI topology satisfactorily provided the fault-tolerance feature of the original CCS-MLI topology.

The proposed CCS-MLI was also tested for THD under the *RL* load, resulting in a good performance. Under this condition, the recorded output voltage and load current THD were 7.8% and 1.4% under healthy (before the open-circuit fault) conditions, as illustrated in Figs. 9(a) and (b), respectively.

Similarly, the proposed CCS-MLI was tested for THD under fault-cleared conditions. The recorded output voltage and load current THD were 19.6% and 13.6% under fault cleared (after the OC fault) conditions as illustrated in Figs. 10(a) and (b), respectively.

Notably, the value of THD can be elevated by 5%

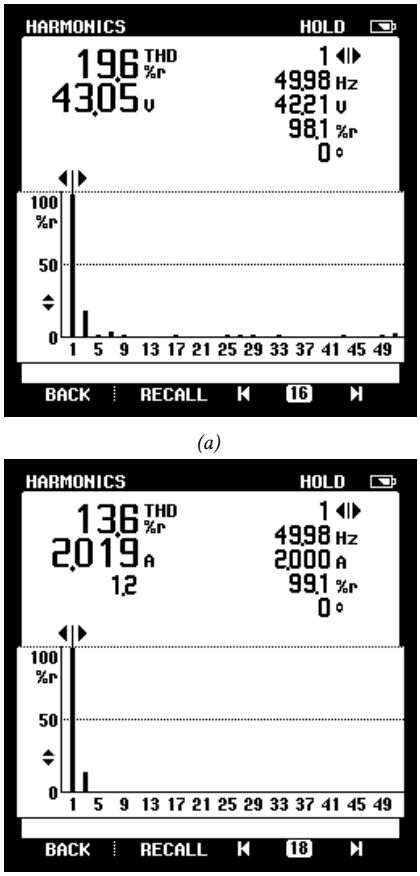


***Fig. 10**: Experimental results for the proposed CCS-MLI topology under fault cleared conditions: (a) output voltage THD spectrum and (b) current THD spectrum.*

by increasing the number of levels at the output or the switching frequency, although with the limitations of increased switching losses and reduced efficiency.

5. COMPARISON OF TOPOLOGIES

This section compares the proposed CCS-MLI with traditional MLI topologies and some recently proposed five-level MLI topologies. Table 5 presents a detailed comparison of five-level MLIs in terms of essential parameters, such as the number of DC sources, diodes, switches, drivers, along with their reliability and fault-tolerant ability. As can be observed, except for the clamping diode and flying capacitor, all the recently proposed topologies exhibit fault-tolerant features. The proposed CCS-MLI topology has greater reliability because it requires a reduced device count (RDC) compared to the remaining five-level MLI topologies examined in Table 5. The proposed CCS-MLI topology is superior on some generalized basis of comparison due to its simple structure and the requirement for fewer power semiconductor devices.

The comparative analysis presents the quantitative and qualitative superiority of the proposed CCS-MLI topology with the other equivalent recently developed

***Table 5**: Comparison between the topology parameters and recently published single-phase five-level MLIs.*

MLI Topology	DC Sources	Capacitors	Main Diodes	Power Switches	Driver Circuits	Output Voltage
Proposed	2	0	0	7	7	5
Clamping diode	4	0	12	8	8	5
Flying capacitor	4	6	0	8	8	5
Cascaded H-bridge	2	0	0	8	8	5
[14]	1	8	0	22	22	5
[15]	4	0	0	20	20	5
[16]	2	0	2	8	7	5
[17]	1	2	2	8	7	5

fault-tolerant topologies. The proposed CCS-MLI topology also offers enhanced reliability by virtue of its requirement for fewer devices such as IGBTs, diodes, and drivers in circuit realization, along with added fault-tolerant capability.

6. CONCLUSION

A five-level single switch fault-tolerant cross-connected source-based multilevel inverter (CCS-MLI) is proposed in this paper. The minimal addition of the redundant switch with the traditional CCS-MLI topology helps to smooth the output voltage level under healthy state and fault-cleared conditions. The working principle is explained, analyzed, and verified using simulation in a MATLAB/Simulink environment. The LSC-PWM technique has been adapted in this study for the generation of a five-level output voltage, pulse, and switching control combination to balance energy between sources. The major advantage of the proposed topology is that it does not require complex calculations or any additional hardware. Finally, the topology has been tested experimentally under healthy and faulty conditions for a five-level inverter, providing satisfactory validation of the proposed topology.

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Dhananjay Kumar received the BE degree in electrical and electronics engineering from the Lakshmi Narain College of Technology, Bhopal, India, in 2014 and M.Tech degree in Electrical Drives from Maulana Azad National Institute of Technology (MANIT), Bhopal, India, in 2017. Since, august 2017, he has been working toward the Ph.D. degree in electrical engineering from MANIT, Bhopal, India. His research interests include power electronics applications, including renewable energy systems, electrical drives and multilevel inverters, and their applications in renewable energy systems.

Rajesh Kumar Nema received Ph.D. degree in electrical engineering from Barkatullah University, Bhopal, in 2004. Since 1986, he has been a Faculty Member at MANIT Bhopal. He has published more than 150 papers in journals and conference proceedings. His research interests include design and control of dc–dc converters and multilevel inverters, Solar PV controller, and renewable energy systems.

Sushma Gupta received the Ph.D Degree from Indian Institute of Technology, Delhi. She was a Lecturer in the Electronic Engineering Department, Government Engineering College, Rewa, India, from 1994 to 1997. Currently, she is working as Professor in Electrical Engineering Department, MANIT Bhopal. India. Her main research interests are multilevel inverters and self-excited induction generator.

Niraj Kumar Dewangan received the Ph.D. degree in Department of Electrical Engineering, National Institute of Technology, Raipur in 2020. Currently, He is working as an Assistant Professor at the Dept. of Electrical engineering in NIT Raipur. His research fields of interest are multilevel inverters, power electronics for renewable energy and modulation strategies for power converters.