Single Phase Multilevel Inverter Based on Single Carrier Pulse Width Modulation Algorithm

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ABSTRACT

High frequency pulse width modulation techniques play very important role in multilevel inverter MLI applications where those techniques overcome the problems associated with their low frequency modulation counterpart techniques. Multicarrier sinusoidal pulse width modulation (MC-SPWM) is a common technique for achieving high frequency modulation and control in MLIs. Several difficulties are found when implementing MC-SPWM technique in real time such as complexity and synchronization between carrier signals in their frequency and voltage levels. This paper presents a simple, high effective algorithm to overcome the problems and difficulties associated with MC-SPWM. The proposed algorithm employs a unique carrier signal instead of multicarrier waveforms thus significantly reduce the complexity and cost as well. Experimental verification of the proposed algorithm utilizing a low cost microcontroller is carried out. The algorithm is applied to 15-level, 7-level and 13-level multilevel inverters to prove its effectiveness. Simulation and experimental validation of the system verify the high performance of the proposed algorithm and consequently the proposed technique can replace MC-SPWM technique not only in the aforementioned MLIs but also in any other MLI that operates based on MC-SPWM.

Keywords: Multi Level Inverter, Pulse Width Modulation, MC-SPWM, Single Carrier PWM

1. INTRODUCTION

Multilevel inverters (MLIs) have gained great interests in power electronics applications in recent years. MLIs are considered as high power quality systems as they can provide inverter output voltage that is very close to sinusoidal shape. MLI can operate either at low or high switching frequency. The current and voltage stresses on the power switches can be diminished in MLIs. In addition, MLIs provide good harmonic characteristics of the output voltage in addition to lower switching losses. MLIs have been widely utilized in several applications such as medium and high speed regulation, high-voltage DC transmission, renewable energy grid systems, railway and electric vehicles, energy storage systems, etc. [1-4].

The modulation technique in multilevel inverters play a crucial role to get precise and high quality waveforms of MLI output voltage and current. According to the operating frequency of power switches, the common modulation techniques of MLIs can be classified into high frequency and low frequency modulation techniques. The most common low frequency modulation techniques are selective harmonic elimination (SHE) [5] and staircase wave synthesis [6]. These low frequency modulation techniques have lower switching losses than the high frequency modulation techniques. However, the dynamic response performance with low frequency modulation is poor where achieving variable modulation index is very difficult because solving nonlinear transcendental equations associated with low frequency modulation is very difficult during dynamic operations. High-frequency modulation techniques overcome the aforementioned disadvantages of low frequency modulation techniques. The most common type of high frequency modulation techniques is the triangular multicarrier based sinusoidal pulse width modulation, SPWM which can be subdivided into level shift pulse width modulation (LS-PWM) [7] and phase shift pulse width modulation (PS-PWM) [8]. In addition, space vector pulse width modulation (SVPWM) can also be applied as a high frequency modulation technique [9].

When applying multicarrier sinusoidal pulse width modulation (MC-SPWM), the control process involves a comparison between high frequency multicarrier signals with a reference sinusoidal signal. In addition, certain hardware logic circuits are employed to generate the required control signals of power switches. When medium and high voltage applications are considered, employing many triangular carrier signals is inevitable. However, those several triangular carrier signals have many problem issues. Computational delays, sampling issues and memory constraints represent difficulties of achieving accurate synchronization of the multicarrier signals in real-time digital implementation and thus the dynamic performance of the MLI become poor, [10], [11]. When applying MC-SPWM in MLIs, several efforts to overcome the problems of MC-SPWM in many applications have been reported in the literature. The authors in [12] simplify the sequence of operation of power switches using logic gates. However still the

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multicarrier signals are required, and many logic gates are utilized to achieve the required pattern. In [13], the authors presented an improved multicarrier pulse width modulation (MCPWM) approach which reduces the 5^{th}, 7^{th}, and 11^{th} order harmonics from the inverter output voltage and they offered an efficient algorithm to estimate the switching angles of the MCPWM pulse-train in real-time operation. However, multicarrier signals are employed with additional complex hardware. A phase shifted double group multicarrier based phase disposition PWM is presented in [14] to eliminate the dc-link high frequency current ripple of modular multilevel converters (MMCs). Several computational algorithms and complexity of the system are recognized due to the double group multicarrier calculation requirements. In [15], another application of multicarrier PWM technique is applied to multilevel boost power factor correction (PFC) rectifier. The main aim is reducing the active semiconductor switches regardless the complexity of multicarrier implementation.

Low number of multicarrier signals is employed in [16] by applying hybrid multicarrier PWM (H-MCPWM) to reduce leakage current produced in a transformerless cascaded MLI in photovoltaic (PV) energy systems. Modified phase-shifted multicarrier PWM scheme is introduced in [17] where the main target is to reduce the switching losses of power switches in cascaded H-bridge multilevel inverter by injecting a clamping period into the sinusoidal reference voltage. The authors in [18] applied a modified multicarrier PWM scheme to a reconfigurable single-phase inverter. The modified multicarrier PWM scheme is implemented either by modifying the wave shape of the carrier signals or by modifying the modulating signals and phase-shifting the carrier waves. A Single carrier based PWM scheme for CHB-MLI is presented in [19] as a modification version for single carrier based PWM scheme in [20]. The modulation technique is based on creating multi-level waveform template, MWT, from which the power switches are controlled. To achieve single triangular carrier signal operation, virtual carrier bands are created that mimic the adjacent bands that the real multicarrier signals occupy in the level shifted SPWM scheme. Additional computations are required to create the virtual carrier bands. This paper presents a novel and simple algorithm for generating the control signals for power switches in single phase MLI based on single carrier pulse width modulation rather than the multicarrier signals. Hence the drawbacks of multicarrier based PWM such as complexity, time delay and synchronization are overcome when applying the proposed algorithm. The proposed algorithm is a general solution for multi-level inverters, with 'N' levels, operating at sinusoidal pulse width modulation. Analysis of the proposed algorithm is presented then the algorithm is applied to three different multi-level inverters; 15-level MLI, 7-level MLI and 13-level MLI as study cases. Total harmonic distortion THD of inverter output voltage and current is calculated and compared with corresponding values in literature to verify the correct operation of the proposed algorithm. Simulation and experimental results are presented to verify the proposed algorithm. The paper is organized as follows: Section 2 presents the operation principle of the considered multi-level inverters. Conventional MC-SPWM is introduced in section 3. Analysis of the proposed algorithm is presented in section 4. Application of the proposed algorithm to the three MLIs through simulation is presented in section 5 and experimental verifications in case of 15-level MLI and 7-level MLI are presented in section 6. Section 7 gives the conclusion.

***Table 1**: States of switches and corresponding inverter output voltage level (15-level MLI).*

State No.	Q_1	Q_3	Q_5	Q_7	V_o
1	0	1	1	1	$7V_d$
2	0	1	1	0	$6V_d$
3	0	1	0	1	$5V_d$
4	0	1	0	0	$4V_d$
5	0	0	1	1	$3V_d$
6	0	0	1	0	$2V_d$
7	0	0	0	1	V_d
8	1	1	1	1	0
9	1	1	1	0	$-V_d$
10	1	1	0	1	$-2V_d$
11	1	1	0	0	$-3V_d$
12	1	0	1	1	$-4V_d$
13	1	0	1	0	$-5V_d$
14	1	0	0	1	$-6V_d$
15	1	0	1	0	$-7V_d$

2. OPERATION OF THE CONSIDERED MLIS

Three different MLI topologies namely 15-level MLI, 7-level MLI and 13-level MLI are considered as study cases where the proposed single carrier PWM algorithm will be applied to each topology. The considered MLIs are presented in Fig. 1. The 15-level MLI circuit is presented in Fig. 1(b) where the circuit includes 4 cells although it can be rearranged to achieve an MLI with 'N' levels by employing 'y' cells according to the relation:

$$N = 2^y - 1. \tag{1}$$

The switches in each cell are turned on or off in a compliment mode. The voltage sources from left cell to right cells are set to V_d, $2V_d$, and $4V_d$, The voltage source in the far-right cell is set to V_R where,

$$V_R = [\frac{N-1}{2}]V_d. \tag{2}$$

V_R is set to $7V_d$ in this case of 15-level MLI. The states of switches Q_1 , Q_3, Q_5 and Q_7 are given in Table 1 with the corresponding values of inverter output voltage V_o. The zero-output voltage is realized by turning on the switches Q_1 , Q_3, Q_5 and Q_7. The negative state

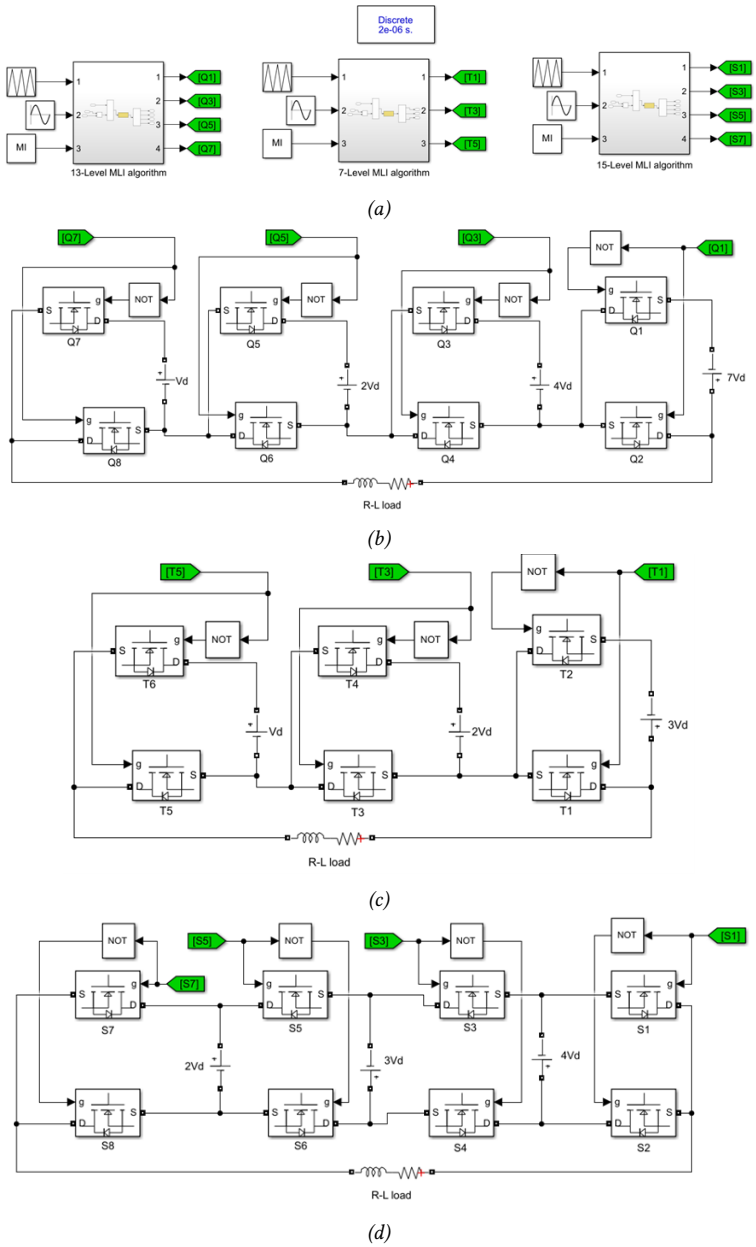


***Fig. 1**: (a) Control signals generation for the considered MLIs (b) 15-Level MLI circuit, (c) 7-Level MLI circuit, (d) 13-Level MLI circuit.*

for a certain V_o is realized if all power switches in the corresponding positive state are inverted. For instant, the state 0100 provides $4V_d$ while the state 1011 will yield $-4V_d$.

The 7-level MLI is obtained if the far-left cell in Fig. 1(b) is omitted and the three power supplies are set to V_d, $2V_d$, and $3V_d$ as can be illustrated in Fig. 1(c). The states of switches T_1 , T_3 and T_5 are given in Table 2 with the corresponding load voltage V_o. Compliment signals of switches T_1 , T_3 and T_5 are assigned to switches T_2 , T_4 and T_6 respectively. The 13-level MLI is presented in Fig. 1(d). The odd switches S_1, S_3, S_5 and S_7 operate in the compliment modes with the even switches S_2, S_4, S_6 and S_8 The states of switches S_1, S_3, S_5 and S_7 are presented in Table 3 with the corresponding values of inverter output voltage V_o.

For the three considered MLIs, negative state for any inverter output V_o is achieved if all power switches in the corresponding positive state are inverted. For instant, in the 13-level MLI, the state 0011 provides $3V_d$ while the state 1100 will yield $-3V_d$.

3. CONCEPT OF CONVENTIONAL MC-SPWM

The conventional MC-SPWM concept is based on the comparison between a reference sinusoidal signal (or a reference rectified sinusoidal signal) having an amplitude (A_{ref}) with an "M" carrier signals to generate the inverter control signals thus achieving output voltage

***Table 2**: States of switches and corresponding output voltage level (seven level inverter).*

State No.	T_1	T_3	T_5	V_o
1	0	1	1	$3V_d$
2	0	1	0	$2V_d$
3	0	0	1	V_d
4	1	1	1	0
5	1	1	0	$-V_d$
6	1	0	1	$-2V_d$
7	1	0	0	$-3V_d$

***Table 3**: States of switches and corresponding inverter output voltage level (13-level MLI).*

State No.	S_1	S_3	S_5	S_7	V_o
1	0	1	1	0	$6V_d$
2	0	0	1	0	$5V_d$
3	0	1	1	1	$4V_d$
4	0	0	1	1	$3V_d$
5	1	1	1	0	$2V_d$
6	0	1	0	0	V_d
7	1	1	1	1	0
8	1	0	1	1	$-V_d$
9	0	0	0	1	$-2V_d$
10	1	1	0	0	$-3V_d$
11	1	0	0	0	$-4V_d$
12	1	1	0	1	$-5V_d$
13	1	0	0	1	$-6V_d$

with 'N' levels. The number of the required carrier signals 'M' for rectified sinusoidal signal operation is defined as:

$$M = (N - 1)/\,2. \tag{3}$$

The higher the desired inverter output levels, the higher the required carrier signals. This is a crucial issue in MLI operating under multi carrier PWM. Many problems arise when implementing multi carrier signals.

a- All carrier signals must be synchronized together.
b- Amplitudes of each carrier signals and voltage shifting between adjacent signals must be adjusted correctly.
c- Many comparator circuits are required to compare the reference signal with the carrier signals.
d- Additional hardware circuits are needed to utilize the outputs of the comparator circuits in such a way to finally generate the control signals to the power switches in the MLI circuit.

As a result of these problems, the system becomes very complicated through simulation and experimental implementation as well.

4. ANALYSIS OF THE PROPOSED SINGLE CARRIER PWM

The proposed algorithm can be considered as a general solution for any MLI with 'N' levels, operating at sinusoidal pulse width modulation. Only one carrier signal

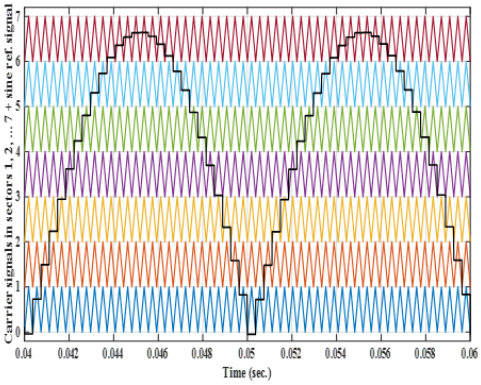


***Fig. 2**: Reference signal and seven carrier signals for 15 levels MLI.*

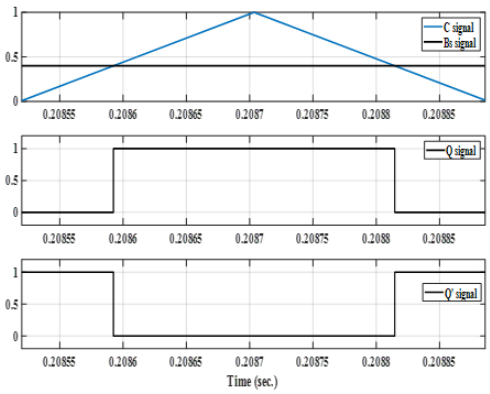


***Fig. 3**: Comparison between C and B_s signal and its outputs Q and $\overline{Q}$.*

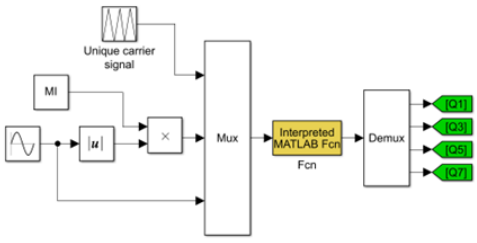


***Fig. 4**: Details of the proposed algorithm.*

is utilized which significantly reduce the aforementioned drawbacks of multi-carrier signals. Fig. 2 only helps the description of the proposed algorithm which is based on single carrier signal rather than multicarrier signals drawn in the figure. The carrier signals in the figure are utilized for 15-level MLI where seven carrier signals are employed in this case. For 7-level MLI and 13-level MLI, three carrier signals and six carrier signals are employed respectively. Referring to Fig. 2, the rectified sine-wave signal is sampled with "i" samples per half cycle where:

$$i = 0.5\ f_c\ /\ f_m, \tag{4}$$

where f_m is the fundamental frequency and f_c the carrier frequency.

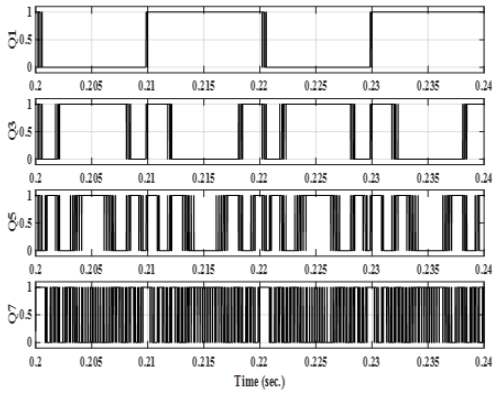


***Fig. 5**: 15-level MLI. Control signals of odd-numbered switches Q_1, Q_3, Q_5 and Q_7 at MI=0.9.*

Each discrete sine-wave sample has the same period as the carrier signals' period. Seven carrier signals occupy seven sectors to achieve 15-level MLI. The following are the basic notations for the proposed algorithm:

A_c: is the amplitude of the carrier signal in the first sector. A_c equals the level shifted value between adjacent carrier signals.

Counter (k): changes from 1 to 54 over one fundamental cycle.

m: denotes the sector in which the inverter output voltage alternates between $(m-1)A_c$ *and* mA_c

$A_s(k)$: is the discrete value of the reference signal (sine-wave signal) during sector 'm' with its actual level.

$B_s(k)$: is the discrete value of the reference signal (sine-wave signal) during sector 'm' with output <= A_c.

Note that $B_s(k)$: is the reference signal which is compared with a single carrier signal in the proposed algorithm.

C: is the carrier signal in the first sector which has an amplitude equal A_c

MI: is the desired modulation index.

The proposed algorithm utilizing single carrier PWM can be described in the following steps:

1) Store the values of $A_s(k)$ corresponding to MI=1, k=1,2,3,... 54 then set 'k' to 1 as an initial value.
2) Set the modulation index 'MI' to the desired value 'MI <=1' then calculate the values of $A_s(k)$ corresponding to MI as follows:

$$A_s(k) = MI \,.A_s(k) \qquad k = 1, 2, 3, \ldots 54 \qquad (5)$$

3) Acquire $A_s(k)$
4) Determine the sector 'm' in which $A_s(k)$ lies.
5) Calculate $B_s(k)$ according to:

$$B_s(k) = A_s(k) - (m-1)\,.A_c \qquad (6)$$

6) Compare $B_s(k)$ with 'C' then generate the control signals of the power switches based on the following rules:
   - The output of the comparison gives the signals 'Q' and '$\overline{Q}$' which are presented in Fig. 3. These two complimentary signals are delivered to the power switches whose states alternate during the present sector.
   - The rest of power switches are kept in the 'off' or 'on' states according to the present sector and present half cycle.
7) Increment 'k' by '1' and go to step 3. If there is any new 'MI' then go to step 2.

As an example of the proposed algorithm, let A_c = 1 V and suppose that at a certain instant related to the 15-level MLI, we have:

$k = 17$, $A_s(17) = 5.4\ V$

Hence 5.4 V lies in the 6^{th} sector, then m=6

$B_s(17) = A_s(15) - (6-1)\,.A_c = 0.4\ V$

Hence compare the 0.4 V with the carrier signal 'C'

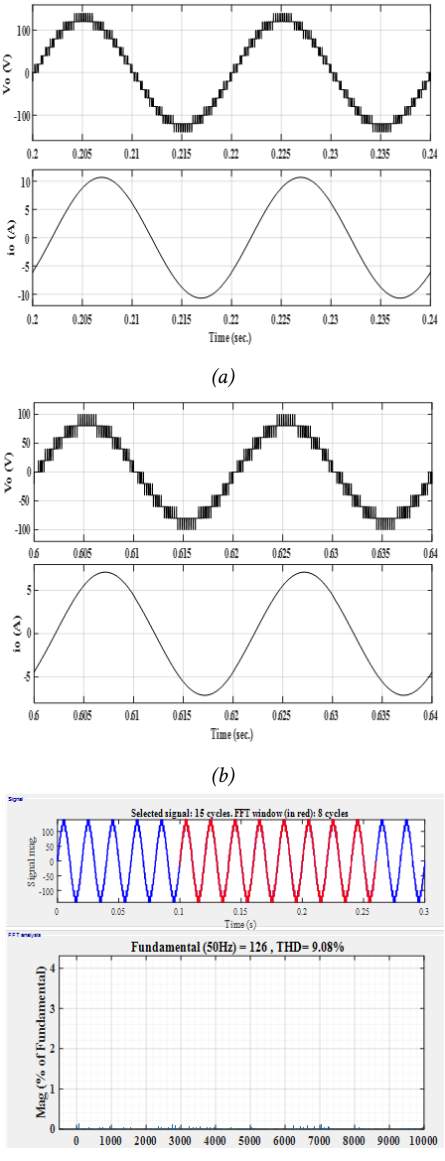


***Fig. 6**: 15-level MLI. Inverter output voltage (V) and load current (A) (a) MI=0.9 (b) MI=0.6, (c) spectrum analysis of v_o at MI = 0.9.*

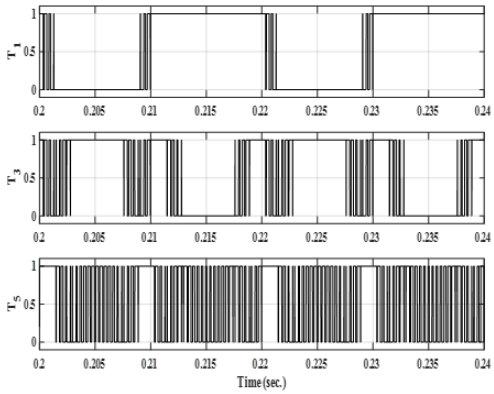


***Fig. 7**: 7-level MLI. Control signals of odd-numbered switches T_1, T_3, and T_5 at MI=0.9.*

to get 'Q' and '$\overline{Q}$' as presented in Fig. 3.

Referring to Table 1, the required control signals of switches Q_1, Q_2, … Q_8 are 01101001 and 01100110 to get $6V_d$ and $5V_d$ respectively.

Hence the control signal 'Q' is assigned to switches Q_5 and Q_8 while '$\overline{Q}$' is assigned to switches Q_6 and Q_7 The states of the other switches are kept without changes; Q_2 and Q_3 are kept 'on' while Q_1 and Q_4 are kept 'off'.

5. SIMULATION RESULTS

This section presents the application of the proposed algorithm to the aforementioned MLIs. Sine-wave signals with amplitude equals $7A_c$, $3A_c$ and $6A_c$ are utilized for 15-level MLI, 7-level MLI and 13-level MLI respectively. A single carrier signal with amplitude equals A_c and modulation index are the other two inputs for each MLI. The three input signals for each MLI are presented in figure 1a. Details of the (15-Level MLI algorithm) in figure 1a are shown in Fig. 4. The sine-wave signal is rectified then multiplied by the modulation index to give the reference signal. The unique carrier signal, reference signal and the non-rectified sine-wave signal are delivered to the interpreted MATLAB function (Fcn). The non-rectified sine-wave signal is utilized to recognize the positive and negative half cycles. The MATLAB function generates the required control signals through an m-file which is written based on the proposed technique (described in section 4). By the same manner, the proposed algorithm is applied to the 7-Level MLI and 13-Level MLI. The control signals of the odd-numbered switches are the outputs of the proposed algorithm. Q_1 , Q_3, Q_5 and Q_7 for the 15-level MLI, T_1 , T_3 and T_5 for the 7-level MLI, S_1 , S_3, S_5 and S_7 for the 13-level MLI. control signals of the even-numbered switches are the compliment states of odd-numbered switches for all MLIs as were described in Section 2. The proposed algorithm can generate the required control signals at any value of modulation index achieving real time operation for wide range of modulation indexes.

For all MLIs, the fundamental frequency is set to 50 Hz. 54 carrier cycles are used over one fundamental period.

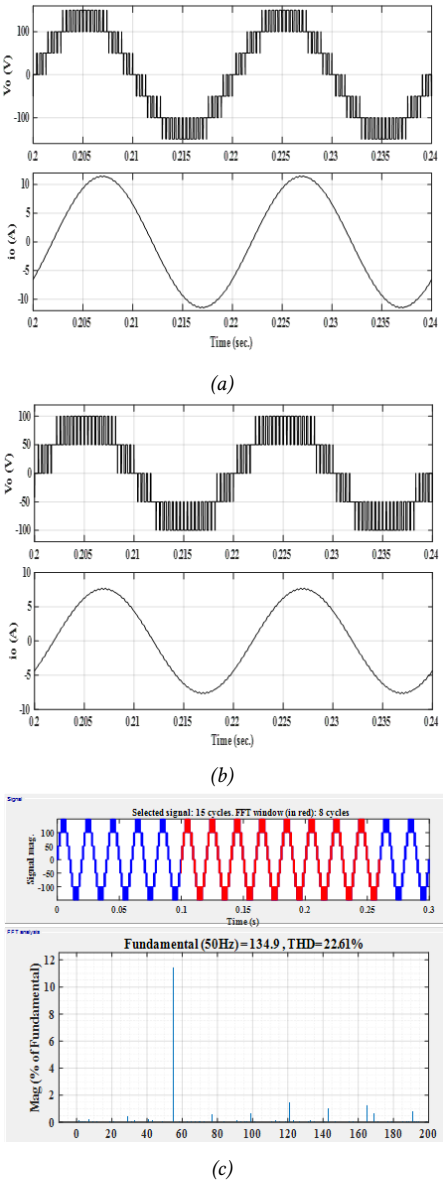


***Fig. 8**: 7-level MLI. Inverter output voltage (V) and load current (A) (a) MI=0.9 (b) MI=0.6, (c) spectrum analysis of v_o at MI = 0.9.*

RL load is selected with R = 10 Ω and L = 20mH. In case of 15-level MLI, V_d is set to 20V. This leads to an output voltage that ranges from -140V to +140V. Regarding to 7-level MLI, V_d is set to 50V which leads to an output voltage that ranges from -150V to +150V. In case of 13-level MLI, V_d is set to 25V. This leads to an output voltage that ranges from -150V to +150V. The control signals of the odd-numbered switches Q_1 , Q_3, Q_5 and Q_7 are given in Fig. 5 at a modulation index of 0.9. Fig. 6 presents the inverter output voltage and load current at modulation indexes of 0.9 and 0.6 in addition to spectrum analysis of v_o at MI = 0.9. The control signals of the odd-numbered switches T_1 , T_3 and T_5 are given in Fig. 7 at a modulation index of 0.9 and Fig. 8 introduces the inverter output voltage and load current at modulation indexes of 0.9 and

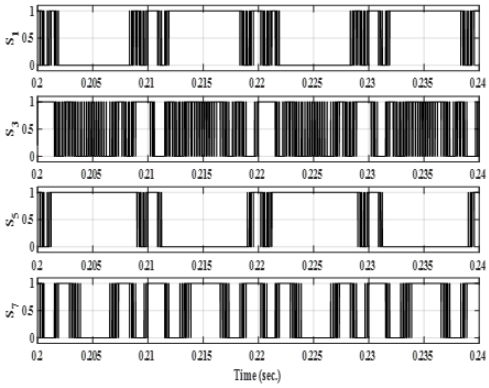


***Fig. 9**: 13-level MLI. Control signals of odd-numbered switches S_1 , S_3, S_5 and S_7 at MI=0.9.*

0.6 in addition to spectrum analysis of v_o at MI = 0.9. The control signals of the odd-numbered switches S_1 , S_3, S_5 and S_7 are given in Fig. 9 at a modulation index of 0.9.

Fig. 10 gives the inverter output voltage and load current at modulation indexes of 0.9 and 0.6 in addition to spectrum analysis of v_o at MI = 0.9. To emphasize the efficient performance of the proposed algorithm, the values of total harmonic distortion THD for the inverter output voltage v_o and inverter output current i_o are calculated along variation of modulation index from 0.1 to 1. Table 4 and Figs. 11 and 12 present the results of THD of v_o and i_o. In addition, the THD_V for the MC-SPWM based MLI given in references [21-23] are presented in Table 4 for the aim of comparison. It can be investigated that the values of THD in the proposed technique are very close to the corresponding values in the literature.

From the results of Figs. 5 to 10 in addition to THD results, it can be proved that the proposed algorithm behaves very excellent, and the results are exactly the same as if MC-SPWM technique is applied for any of the considered MLIs. Therefore, it can be said that the proposed algorithm is a general simple effective algorithm, and it is an effective alternative solution for any other multi-level inverters that operate on the basis of multi carrier sinusoidal pulse width modulation technique.

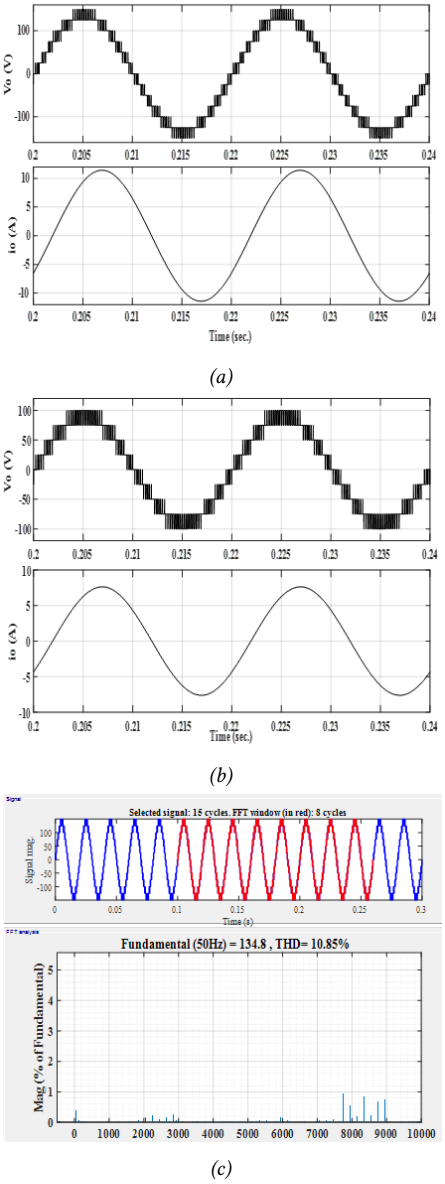


***Fig. 10**: 13-level MLI. Inverter output voltage (V) and load current (A) (a) MI=0.9 (b) MI=0.6, (c) spectrum analysis of v_o at MI = 0.9.*

6. EXPERIMENTAL RESULTS

A small-scale single-phase inverter is built for the 15-level and 7-level MLIs to verify the effectiveness of the proposed algorithm. The prototype setup of the system is presented in Fig. 13. It includes the following main parts: (1) low cost PIC18F2431 microcontroller, (2) 16 MHz crystal oscillator, (3) PIC-kit 3 programmer, (4) N-channel power MOSFET switches IRF740, (5) optocoupler 6n137, (6) Four power supplies for inverter power circuit 4V, 8V, 16V and 28V (7) R-L load with L=230mH and R=100Ω and (8) 4-channel measuring oscilloscope. The microcontroller PIC18F2431 is utilized to apply the proposed algorithm and generate the required gating signals of power switches where its internal PWM module is employed to generate the control signal Q and $\overline{Q}$ that are given in Fig. 3. Fortunately, operating microcontroller PWM module in the center-alignment mode mimics exactly the comparison between carrier signal with constant value. The carrier frequency is set to 2700 Hz as in simulation procedure. After initializing the hardware modules of the microcontroller, the same steps (described in section 4) are executed. Modulation index is adjusted at 0.9 The control signals of switches Q_1, Q_3, Q_5 and Q_7 are given in Fig. 14 at MI=0.9. Q_1 and Q_3 operate nearly at low switching frequency while Q_5 and Q_7 operate at high switching frequency. Complement signals are delivered to switches Q_2, Q_4, Q_6 and Q_8. The output voltage of the inverter

***Table 4**: Total harmonic distortion of inverter output voltage v_o and inverter output current i_o*

Modulation Index (MI)		0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
7-Level MLI	v_o	180	106.4	64.4	45.13	39.24	33.46	25.22	24.13	22.61	18.54
		[Ref. 21]: THD = 19.48 at MI = 1									
		[Ref. 23]: THD = 17.84 at MI = 1									
	i_o	6.1	3.56	2.54	2.87	2.2	1.43	1.34	1.27	1.24	1.02
13-Level MLI	v_o	106	44.53	33.33	24.29	18.03	16.8	13.2	12.37	10.85	9.27
		[Ref. 21]: THD = 9.21 at MI = 1									
		[Ref. 22]: THD = 16 at MI = 0.5, THD = 11.24 at MI = 0.8, THD = 8.33 at MI = 1									
	i_o	1.92	0.733	0.6	0.49	0.42	0.37	0.33	0.28	0.25	0.23
15-Level MLI	v_o	90.6	41.85	25.3	21.4	17.1	13.33	11.96	10.78	9.08	8.12
		[Ref. 21]: THD = 7.98 at MI = 1									
	i_o	1.65	0.73	0.49	0.46	0.37	0.35	0.29	0.26	0.23	0.22

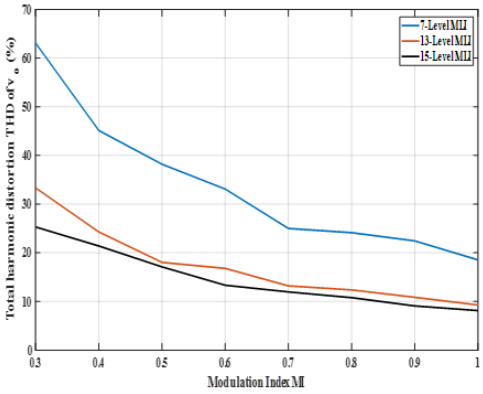


***Fig. 11**: THD of inverter output voltage v_o versus modulation index.*

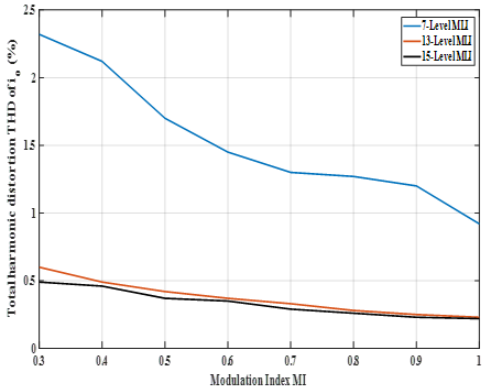


***Fig. 12**: THD of inverter output current i_o versus modulation index.*

***Fig. 13**: Experimental setup of the single phase 15 levels MLI.*

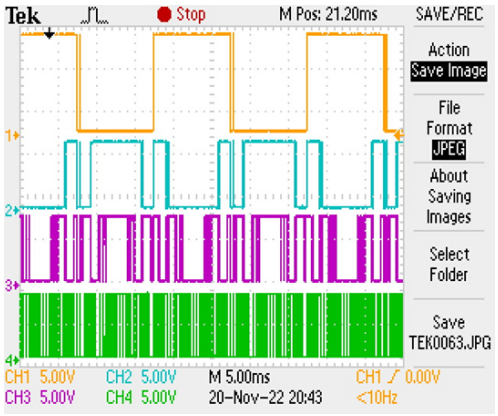
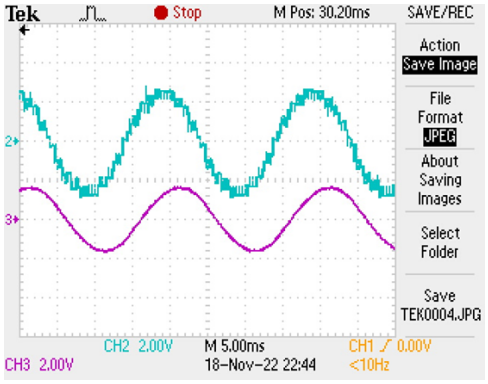


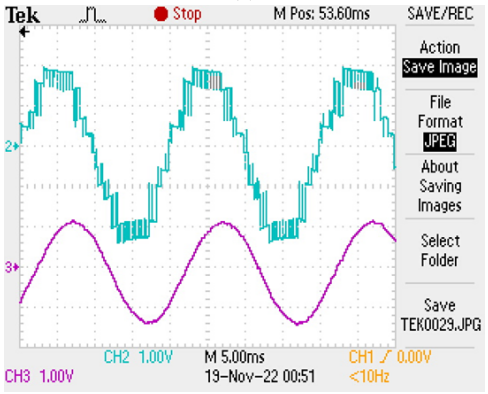
***Fig. 14**: 15-level MLI Experimental results) control signals of switches Q_1, Q_3, Q_5 and Q_7 at MI=0.9 .*

and load current are shown in Fig. 15 at MI=0.9 and MI=0.6. The load current in both values of MI is very close to sinusoidal shape. A comparison between the control signals, output voltage and load current in simulation results and the counterpart experimental results verifies the successful application of the proposed algorithm. Experimental results for 7-Level MLI are carried out for the same load parameters of 15-Level MLI (L=230mH and R=100Ω). The cells supply voltages are set to 4V, 8V and 12V. Fig. 16 shows the control signals of switches T_1, T_3 and T_5. Fig. 17 presents the load voltage and currents at MI=0.9 and MI=0.6. The results are very close to simulation results in Fig. 8. Spectrum analysis of inverter output voltage and load current at MI=0.9 is shown in Fig. 18.

To calculate the total harmonic distortion in this case using the available oscilloscope (TDS 2014C), either one



(a)



(b)

***Fig. 15**: 15-level MLI Experimental results (a) output voltage of the inverter (20V/div) and load current (0.2A/div.) MI=0.9 (b) output voltage of the inverter (20V/div) and load current (0.1A/div.), MI=0.6.*

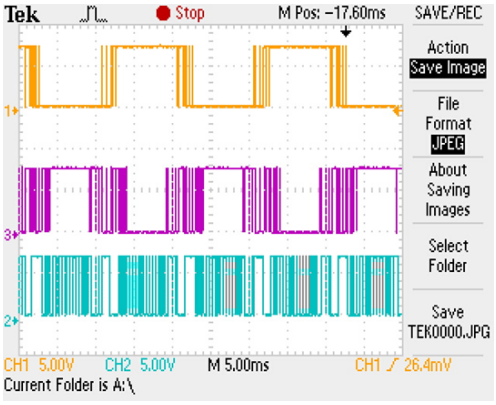
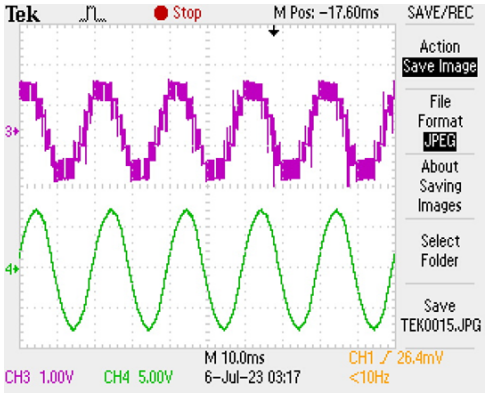


***Fig. 16**: 7-level MLI Experimental results) control signals of switches T_1, T_3 and T_5 at MI=0.9.*

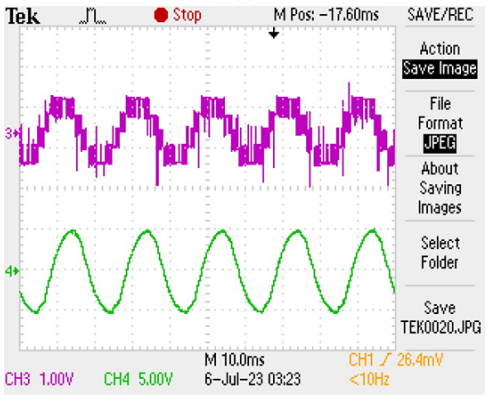
of the following THD formula can be applied. Obviously the second formula is the easier one.

$$THD = \frac{1}{V_1}\left(\sum_{n=2,3,4,\ldots}^{\infty} V_n^2\right)^{0.5} = \frac{1}{V_1}\left(V_{rms}^2 - V_1^2\right)^{0.5}$$

Applying the second formula and taking into account that the Y-axis in the spectrum analysis is in (dB) not in voltage. The experimental THD_V and THD_I are calculated as 28% and 1.8% respectively which are close



(a)



(b)

***Fig. 17**: 7-level MLI Experimental results output voltage of the inverter (10V/div) and load current (50mA/div.) (a) MI=0.9 and (b) MI=0.6.*

to the corresponding values in Table 4.

As the 15-level and 7-level MLIs are chosen for experimental verification, similar results can be obtained for 13-level MLI.

7. CONCLUSION

A simple low cost and effective algorithm is proposed for multilevel inverters that operate at sinusoidal pulse width modulation. The proposed algorithm is based on utilizing single carrier signal instead of multicarrier based PWM. Hence, the several difficulties of MC-SPWM are avoided with single carrier signal. The algorithm utilizes the symmetry of the shifted carrier waveforms when comparing these waveforms with discrete sine-wave signal in the conventional MC-SPWM. The proposed algorithm is applied to three different topologies of MLIs through simulation. The considered MLIs 15-level, 7-level and 13-level MLIs. Simulation results are exactly the same if MC-SPWM is applied to each topology. Total harmonic distortion of inverter output voltage and current is calculated for the considered MLIs. The results of THD are very close to that in the literature. The proposed algorithm is simply implemented using single chip PIC18F2431 microcontroller to generate the gating signals to power switches of the MLI. The proposed algo-

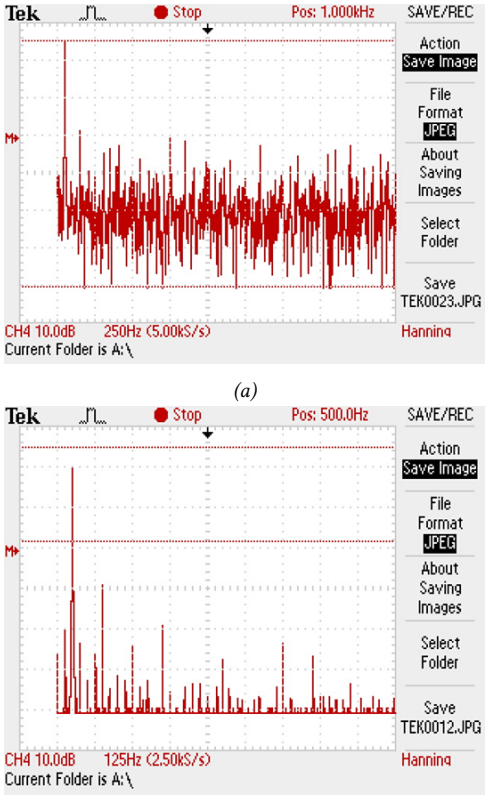


***Fig. 18**: 7-level MLI Experimental results Spectrum analysis of inverter output voltage (a) and load current (b) at MI=0.9.*

rithm is tested using single phase 15-level MLI through experimental verification. Simulation and experimental results verify that the proposed algorithm can be applied successfully and therefore multicarrier based SPWM can be replaced by the proposed algorithm and consequently the great difficulties of MC-SPWM can be avoided. The proposed algorithm can be considered as a general alternative solution technique for any multicarrier based MLI that operates with SPWM.

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