The Performance of Organic Field Effect Transistor Affected by Different Thickness of Active Semiconductor Layer and Thickness of Gate Insulator

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ABSTRACT

The purpose of this paper is to fabricate organic field effect transistor and to investigate the effect of the thickness of the pentacene active layer and the thickness of gate insulator layer on MOSFET performance. The fabricated structure is top-contact. When the thickness of the insulator gate layer increases from 10 nm to 30 nm, the magnitude of the drain source current, when V_{GS} = V_{DS} = -4 V, decreases from 1813 nA to 214 nA and then the threshold voltage shifts from -1.4 V to -2.4 V. When the thickness of pentacene increases from 9 nm to 40 nm, the threshold voltage shifts slightly in the negative direction from -1.4 V to -1.6 V in case of SiO_2 thickness of 10 nm. In case of SiO_2 thickness of 20 nm, the threshold voltage shifts from -1.9 V to -2.2 V. In case of SiO_2 thickness of 30 nm, the threshold voltage shifts from -2.4 V to -2.9 V. Besides that, the mobility decreases from around 0.31 cm^2/(Vs) to 0.15 cm^2/(Vs) when the pentacene thickness increases from 9 nm to 40 nm.

Keywords: Transistor, MOSFET, Pentacene, Organic

1. INTRODUCTION

Organic electronics has gone far beyond being a specific research term [1]. Organic MOSFETs have lower charge carrier mobility and a larger subthreshold slope than conventional MOSFETs. However, organic MOSFETs can be applied to flexible devices [2]. Flexible devices are difficult to fabricate on inorganic substrates like silicon. Thickness is one of the fundamental physical parameters affecting transistor devices. Semiconductor layer thickness is related to transistor performances as observed in several studies. However most of studies are based on bottom contact configuration and very few investigations were performed in the top contact transistors. Therefore, the purpose of this paper is to fabricate top-contacct organic field effect transistor and to see the effect of the thickness of the pentacene active layer and the thickness of gate insulator layer on MOSFET performance. This research is important since the thickness of semiconductor layer is related to resitance of the devices.

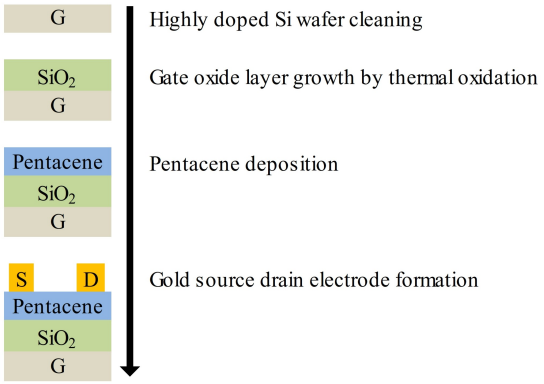

***Fig. 1**: Fabrication process.*

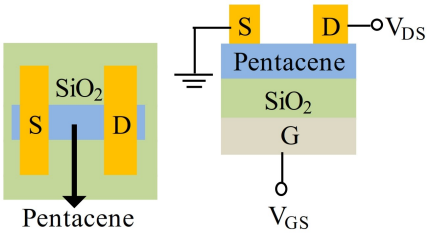

***Fig. 2**: The top view and measurement schematic.*

2. METHOD

Figure 1 shows the fabrication sequence. First highly dopes silicon wafer was cleaned using sulphuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) mixture (SPM). Then, SiO_2 gate insulator with thicknesses of 10 nm, 20 nm and 30 nm were grown using the thermal wet oxidation method on heavily doped silicon wafers for 10, 20 and 30 minutes respectively. SiO_2 is an insulator layer [3]. These heavily doped silicon wafers have very low specific resistance, resulting in very high conductivity. This silicon wafer works as a gate electrode. After that, pentacene organic semiconductors with thicknesses of 9 nm, 21 nm and 40 nm were deposited using the thermal evaporation method. Pentacene is well-known

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for its high mobility and conductivity [4]. The advantage of thermal evaporation method is it is a solvent free technique [5]. The high deposition rate is another advantage of thermal evaporation [6]. Finally, source and drain electrodes were formed from Au (gold) by thermal evaporation method. The work function of gold is 5.1 eV [7]. Gold and pentacene interface have good ohmic characteristic as the HOMO level of pentacene is ∼5.2 eV and the work function of Au is ∼5.1 eV [8]. After fabrication is complete, the electrical characteristics of the I_D-V_D and I_D-V_G are measured. Figure 2 shows the schematic top view of the device and a schematic of measuring the electrical characteristics of a pentacene MOSFET.

3. RESULTS AND DISCUSSION

Figure 3 shows the I_D-V_D and I_D-V_G characteristics when the thickness of pentacene is 9 nm. Figure 3(a), (b) and (c) show the I_D-V_D characteristics when the thickness of SiO_2 is 10 nm, 20 and 30 nm, respectively. The horizontal axis represents drain source voltage and the vertical axis shows drain source current. When the thickness of SiO_2 is 10 nm, the drain source current magnitude when the gate source voltage = drain source voltage = -4 V is about 1813 nA. When the thickness of SiO_2 is 20 nm, the drain source current magnitude decreases to about 572 nA. When the thickness of SiO_2 is 30 nm, the drain source current magnitude decreases to about 214 nA Figure 3(d) show the I_D-V_G characteristics. The horizontal axis represents gate source voltage and the vertical axis shows drain source current magnitude. When the thickness of SiO_2 is 10 nm, the threshold voltage is about -1.4 V. When the thickness of SiO_2 is 20 nm, the threshold voltage is about -1.9 V. When the thickness of SiO_2 is 30 nm, the threshold voltage is about -2.4 V. Threshold voltage V_T is required to detect a digital signal as an H (or 1) / L (or 0) signal. It is the potential that becomes the threshold value. It is the voltage applied to the gate-source voltage applied to form a source-drain conduction path. In this way, it is used in various places such as the minimum potential between signal grounds required for an IC with a built-in transistor to recognize it as a signal. Threshold voltage is important parameter [9]. This voltage is the most important number for maintaining power efficiency and signals. It is the voltage required to switch the transistors

In general, when the magnitude of drain source voltage is increased, the magnitude of drain source current will increase to certain point and become saturated. In general, when the magnitude of gate source voltage is increased, the magnitude of drain source current will increase. The increase in drain source current as the gate source voltage changes in the negative direction is caused by an increase in the positive hole carrier charge induced by the negative gate voltage. Meanwhile, when the drain voltage becomes negative, the drain source current increases, but at a certain voltage the current becomes saturated and does not increase anymore.

Figure 4 shows the I_D-V_D and I_D-V_G characteristics when the thickness of pentacene is 21 nm. Figures 4(a), (b) and (c) show the I_D-V_D characteristics when the thickness of SiO_2 is 10 nm, 20 and 30 nm, respectively. The horizontal axis represents drain source voltage and the vertical axis shows drain source current. When the thickness of SiO_2 is 10 nm, the drain source current magnitude when the gate source voltage = drain source voltage = -4 V is about 973 nA. When the thickness of SiO_2 is 20 nm, the drain source current magnitude decreases to about 293 nA. When the thickness of SiO_2 is 30 nm, the drain source current magnitude decreases to about 90 nA. Figure 4(d) show the I_D-V_G characteristics. The horizontal axis represents gate source voltage and the vertical axis shows drain source current magnitude. When the thickness of SiO_2 is 10 nm, the threshold voltage is about -1.5 V. When the thickness of SiO_2 is 20 nm, the threshold voltage is about -2.0 V. When the thickness of SiO_2 is 30 nm, the threshold voltage is about -2.6 V.

Figure 5 shows the I_D-V_D and I_D-V_G characteristics when the thickness of pentacene is 40 nm. Figure 5(a), (b) and (c) show the I_D-V_D characteristics when the thickness of SiO_2 is 10 nm, 20 and 30 nm, respectively. The horizontal axis represents drain source voltage and the vertical axis shows drain source current. When the thickness of SiO_2 is 10 nm, the drain source current magnitude V_{GS} = V_{DS} = -4 V is about 752 nA. When the thickness of SiO_2 is 20 nm, the drain source current magnitude decreases to about 196 nA. When the thickness of SiO_2 is 30 nm, the drain source current magnitude decreases to about 45 nA. Figure 5(d) show the I_D-V_G characteristics. The horizontal axis represents gate source voltage and the vertical axis shows drain source current magnitude. When the thickness of SiO_2 is 10 nm, the threshold voltage is about -1.6 V. When the thickness of SiO_2 is 20 nm, the threshold voltage is about -2.2 V. When the thickness of SiO_2 is 30 nm, the threshold voltage is about -2.9 V.

Figure 6(a) shows the dependence of threshold voltage on SiO_2 thickness. The horizontal axis represents the thickness of SiO_2 in nm and the vertical axis represents the threshold voltage in V. Based on the graph, when the SiO_2 increases from 10 nm to 30 nm, the threshold voltage shifts in negative direction from -1.4 V to -2.4 V. The gate capacitance increases when the gate oxide thickness is decreased. It allows a smaller voltage to induce the same channel charge and drive current.

Figure 6(b) shows the dependence of threshold voltage on pentacene thickness. The horizontal axis represents the thickness of pentacene in nm and the vertical axis represents the threshold voltage in V. Based on the graph, when the pentacene thickness increases from 9 nm to 40 nm, the threshold voltage shifts slightly in negative direction from -1.4 V to -1.6 V for SiO_2 thickness of 10 nm. The increase in the magnitude of threshold voltage probably results from an injection barrier at the gold–pentacene interface. The threshold voltage shift is also

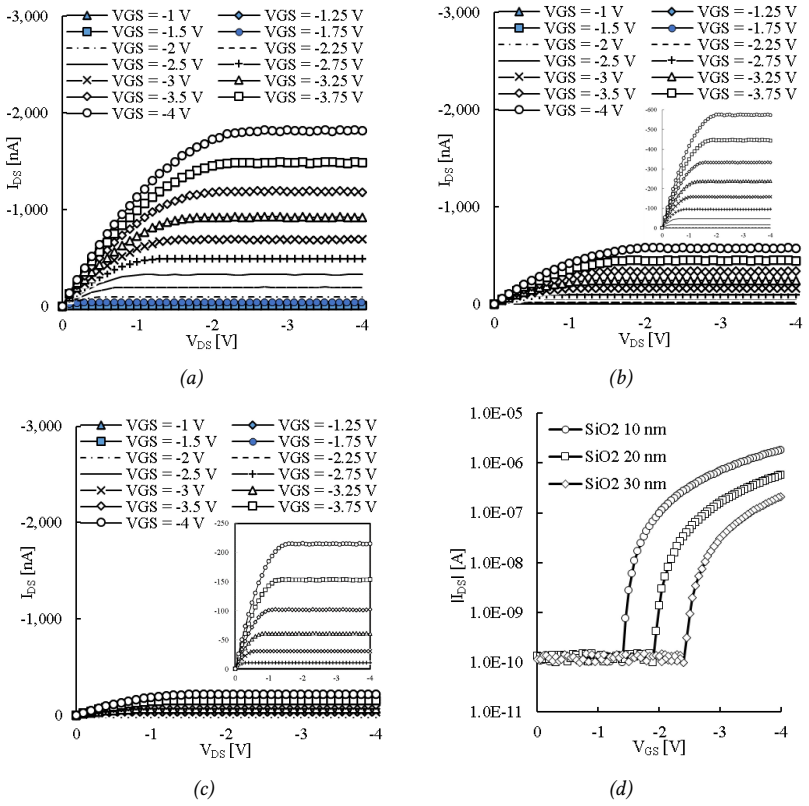

***Fig. 3**: (a) I_D-V_D characteristic when pentacene 9 nm and SiO_2 10 nm (b) I_D-V_D characteristic when pentacene 9 nm and SiO_2 20 nm (c) I_D-V_D characteristic when pentacene 9 nm and SiO_2 30 nm (d) I_D-V_G characteristic when pentacene 9 nm.*

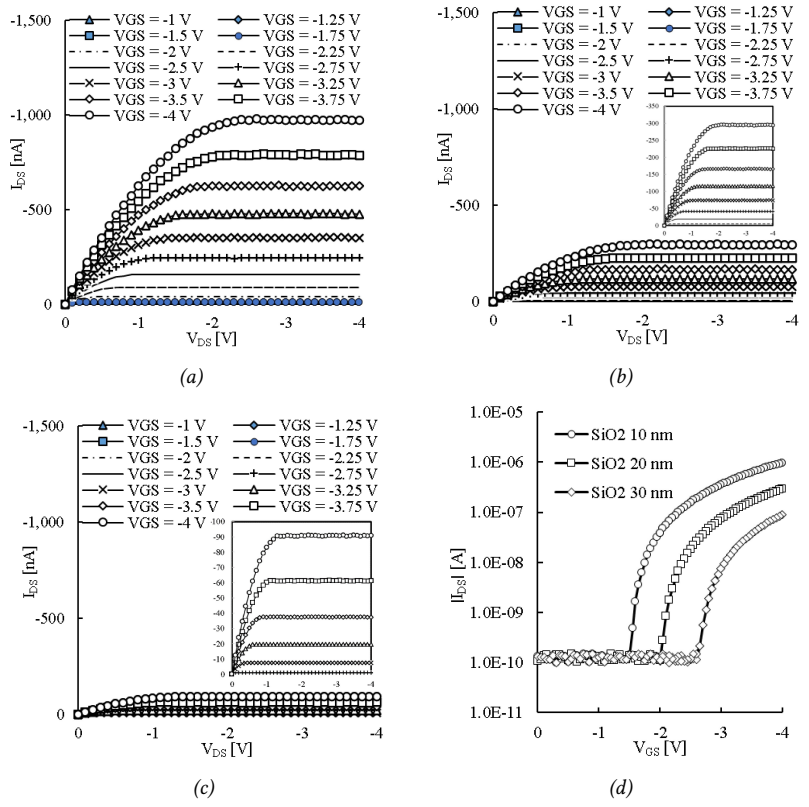

***Fig. 4**: (a) I_D-V_D characteristic when pentacene 21 nm and SiO_2 10 nm (b) I_D-V_D characteristic when pentacene 21 nm and SiO_2 20 nm (c) I_D-V_D characteristic when pentacene 21 nm and SiO_2 30 nm (d) I_D-V_G characteristic.*

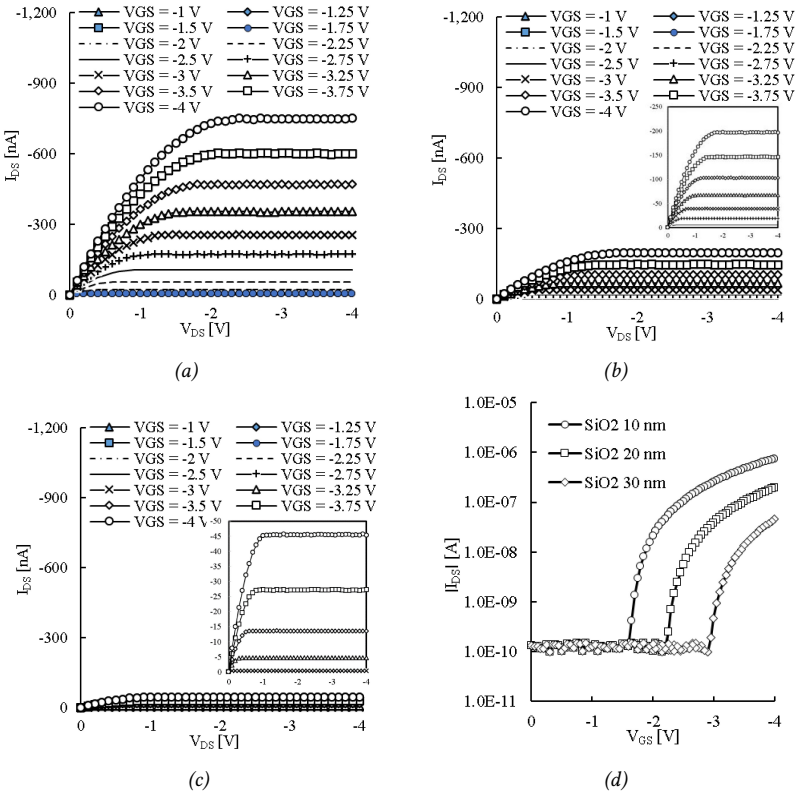

***Fig. 5**: (a) I_D-V_D characteristic when pentacene 40 nm and SiO_2 10 nm (b) I_D-V_D characteristic when pentacene 40 nm and SiO_2 20 nm (c) I_D-V_D characteristic when pentacene 40 nm and SiO_2 30 nm (d) I_D-V_G characteristic.*

***Table 1**: Comparison with other works.*

	This work	Ref. [11]	Ref. [12]	Ref. [13]	Ref. [14]	Ref. [15]
Mobility [cm^2/Vs]	0.31	0.12	0.048	0.09	0.04	0.035
Threshold voltage [V]	-2.9	-12.9	-3.1	-	-15	-8.5
$\|I_{DS}\|_{max}$ [nA]	1813	~45	~1001	-	~900	-
Subthreshold Swing [V/dec]	2.9	9.3	-	-	-	-
On/Off ratio	~10^3	~10^3	98.3	-	10^3	-

caused by that the presence of dipole monolayer.

Figure 7 shows the dependence of mobility on pentacene thickness. Mobility is a parameter related to the efficiency of carrier transport [10]. The horizontal axis represents the thickness of pentacene in nm and the vertical axis represents the mobility in cm^2/(Vs). Generally, based on the graph, when the pentacene thickness is increased, the mobility decreases and saturates. When the SiO_2 thickness is 10 nm, the mobility is 0.31 cm^2/(Vs), 0.18 cm^2/(Vs)and 0.15 cm^2/(Vs) when the pentacene thickness is 9 nm, 21 nm and 40 nm, respectively. The mobility decreases with the presence of traps and grain boundaries. Small grain sizes decrease the number of grain boundaries acting as charge traps during the transport. Table 1 shows the comparison with other works. The mobility obtained in this work is higher than those obtained in reference [11], [12], [13], [14] and [15]. The magnitude of threshold voltage obtained in this work is lower than those obtained in reference [11], [12], [14] and [15]. This work has larger drain source current compared to reference [11], [12] and [14]. The sub-threshold swing obtained in this work is lower than those obtained in reference [11]. The on off ratio obtained in this work is higher than that obtained in reference [12] and similar with those obtained in reference [11] and [14].

One of the intrinsic properties of a semiconductor material is the mobility of electrons and holes [16]. Factors such as electric field, geometry, impurities trapped, the presence of oxygen and grain size can affect electron mobility [17]. Electron mobility very important to determine the speed of the device and is required for high speed transistors and photovoltaic with good performance [18]. On transistor, the off current can be affected by doping, interface properties, tunnelling, crystal structure and time living carriers [19]. Temporary Therefore, the threshold voltage can be affected by saturation velocity, contact material, moving charge, work function of the gate electrode, gate dielectric,

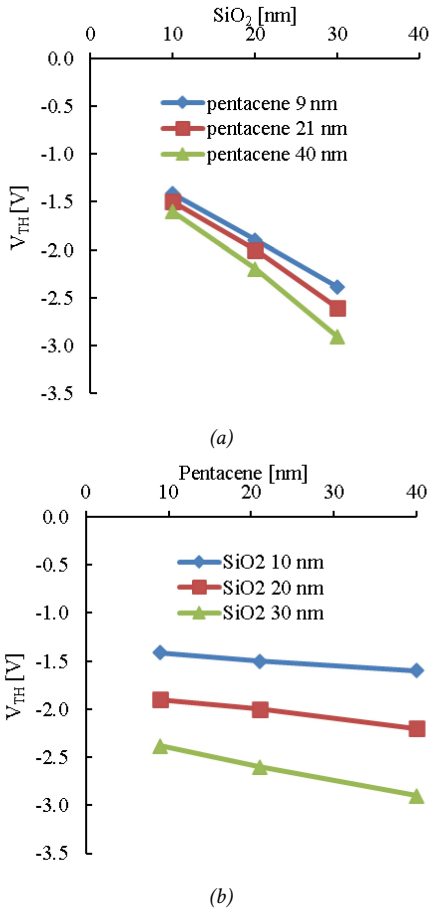

***Fig. 6**: The dependence of threshold voltage on (a) SiO_2 thickness (b) pentacene thickness.*

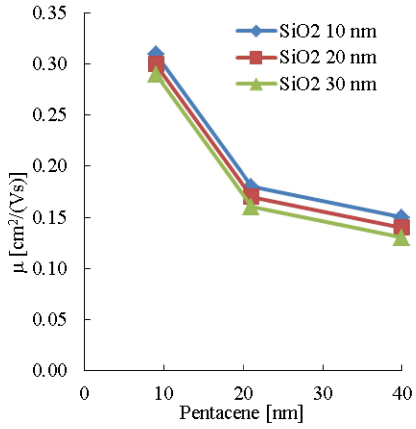

***Fig. 7**: The dependence of mobility on the pentacene thickness.*

dielectric layer capacitance and channel modulation [20].

4. CONCLUSION

The purpose of this research has been achieved. Organic field effect transistor with structure of top contact is fabricated. The active semiconductor layer is pentacene and the gate insulator layer is SiO_2. The effect of increasing thickness of SiO_2 and pentacene is investigated. The magnitude of the drain source current, when V_{GS} = V_{DS} = -4 V, decreases from 1813 nA to 214 nA and then the threshold voltage shifts from -1.4 V to -2.4 V as the thickness of the insulator gate layer is increased from 10 nm to 30 nm. The threshold voltage shifts slightly in the negative direction from -1.4 V to -1.6 V for SiO_2 thickness of 10 nm as the thickness of the pentacene is increased from 9 nm to 40 nm. In case of SiO_2 thickness of 20 nm, the threshold voltage shifts from -1.9 V to -2.2 V. In case of SiO_2 thickness of 30 nm, the threshold voltage shifts from -2.4 V to -2.9 V. Besides that, the mobility decreases from around 0.31 $cm^2/(Vs)$ to 0.15 $cm^2/(Vs)$ when the pentacene thickness increases from 9 nm to 40 nm. Based on the conclusion above, the suggestion related to this research is offered for the other researchers. The researcher hopes that the result of this study can be used as reference to improve the performance of the organic transistor devices.

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