Various Methods of Realization for Fractional-Order Elements

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ABSTRACT

Fractional-order circuits are finding applications in control systems, signal processing, and other allied fields. As a result, realizing fractional-order elements or fractance devices is an essential research topic. A unique fractance device is realized in this study using continued fraction expansion (CFE) and partial fraction expansion (PFE) formulas. Continued fraction expansion is used to calculate the rational approximation. For simulation, the fourth order rational approximation for fractional order, $\alpha = -1/2, -1/3, -1/4$ is used. All simulations are carried out with the help of the MATLAB and TINA software packages. The theoretical and simulation results are in agreement.

Keywords: Fractional Order, Continued Fraction Expansion, Rational Approximation, Fractance Device, Magnitude Response, Phase Response, Simulation

1. INTRODUCTION

Fractional calculus has been studied for over 300 years [1]. It refers to α, or the extension of integration and differentiation to any order. The processes of integration and differentiation are generalized in fractional calculus. This mathematical idea is used in control systems, instrumentation, physics, signal processing, image processing, electrical circuits, and other fields [2, 3].

A fractional-order system is defined by a fractional-order differential equation. In the literature, it has been proven that fractional-order systems have an inherent property of limitless memory. Memory is constrained in integer-order systems. Heat diffusion through solids, transmission lines, fractional-order differentiators and integrators, and the nature of hills are all fractional-order systems.

In general, the operator ${}_aD_t^{\alpha}$ can be used to express differentiation and integration in the non-integer order, where α is the fractional order and t are the operation's bounds. The frequency-domain representation of an ideal fractional-order differ-integrator is $H(s) = (s)^{\pm\alpha}$, where α denotes the order and its value ranges from 0 to 1. $j\omega$ is the variable s, where $\omega = 2\pi f$ rad/s. A fractional-order system refers to any system that can be represented by a fractional-order differential equation. A system with input $x(t)$ and $y(t)$ is related to the following equation [2],

$$a_n D^{\alpha_n} y(t) + a_{n-1} D^{\alpha_{n-1}} y(t) + \ldots + a_0 D^{\alpha_0} y(t) = b_n D^{\beta_n} y(t) + b_{n-1} D^{\beta_{n-1}} y(t) + \ldots + b_0 D^{\beta_0} y(t) \quad (1)$$

where a_n, a_{n-1}, …, a_0 and b_n, b_{n-1}, …, b_0 are system coefficients and the differentiation orders are integer multiples of based orders, i.e., $\alpha_k = \beta_k = k\alpha$. Applying the Laplace transform to Eq. (1) with zero initial conditions, the transfer function can be expressed as

$$H(s) = \frac{Y(s)}{X(s)} = \frac{b_m s^{\beta_m} + b_{m-1} s^{\beta_{m-1}} + \ldots + b_0 s^{\beta_0}}{a_n s^{\alpha_n} + a_{n-1} s^{\alpha_{n-1}} + \ldots + a_0 s^{\alpha_0}} \quad (2)$$

Fractional-order systems offer a substantial benefit over integer-order systems since they are dictated by memory. Integer-order systems have finite memory, but fractional-order systems have unbounded memory. Fractional-order differentiators (FODs) and integrators (FOIs) are part of fractional-order systems. For any arbitrary order, the time integral and derivative of a signal are determined using generalized fractional differentiation and integration. In the literature, there are numerous definitions for fractional-order calculus. Fractional-order differ-integrators are often defined using the Grünwald-Letnikov (G-L) and Riemann-Liouville (R-L) derivatives. The following is the Grünwald-Letnikov (G-L) definition:

$$D_t^{\alpha} f(t) = \lim_{h \to 0} \frac{1}{h^{\alpha}} \sum_{i=0}^{\infty} (-1)^i \binom{\alpha}{i} f(t - ih) \quad (3)$$

where

$$\binom{\alpha}{i} = \frac{\Gamma(\alpha + 1)}{\Gamma(i + 1)\Gamma(\alpha - i + 1)}$$

and $\Gamma(\cdot)$ is Euler's gamma function.

The Riemann-Liouville (R-L) definition is

$${}_aD_t^{\alpha} = \frac{1}{\Gamma(n - \alpha)} \frac{d^n}{dt^n} \int_a^t \frac{f(\tau)}{(t - \tau)^{\alpha - n + 1}} d\tau \quad (4)$$

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for $(n-1<\alpha<n)$, where a and t are the limits of the operation ${}_aD_t^{\alpha} f(t)$. Many definitions exist for fractional-order differentiation and integration. However, the commonality is that the Laplace transform can be expressed as s^{α} independent of the way it is defined.

A fractional-order system includes a fractional-order device. An electrical element with fractional-order impedance qualities is known as a fractance device. This device is also called a constant phase element or fractor. Robotics, hard disc drives, signal processing circuits, fractional-order control, and other fields use the fractance device. A fractance device can be used to produce moderate characteristics between an inductor, resistor, and capacitor. Fractional-order differentiation and integration can be simply achieved with the help of an operational amplifier and a fractance device.

The structure of the paper is broken down as follows. Section 2 discusses the performance of the fractance device. Section 3 explains the basic elements, while a literature review is presented in Section 4. The proposed methodology is detailed in Section 5. The findings and discussion are included in Section 6, along with the conclusions in Section 7.

2. FRACTANCE DEVICE

The fractance device is an emerging element in electrical engineering which is an attractive field of research for many people across the world. The mathematical equation defines it as,

$$Z(s)=\frac{k_0}{s^{\alpha}} \tag{5}$$

where k_0 is a constant, α is the fractional order, and s is the Laplace transform operator. The absolute value is given by,

$$|z(j\omega)|=\frac{k_0}{\omega^{\alpha}} \tag{6}$$

and the phase angle is expressed as,

$$\angle z(j\omega)=\pm\frac{\alpha\pi}{2} \tag{7}$$

+ sign for a differentiator and − sign for an integrator.

The phase angle is proportional to the frequency but solely depends on the fractional-order value. As a result, this device is also known as a *fractor* or *constant phase angle device*. The variations in magnitude and phase response of the device are shown in Figs. 1 and 2, respectively. The magnitude reveals the value of linear changes in either an increasing or decreasing manner. However, the phase angle remains constant irrespective of the value of α. The response of the half and one-quarter fractional-order differentiator and integrator responses are shown in Figs. 1 and 2. From the responses, it is clear that the magnitude in dB decreases along with the fractional order. The fractional order of the differentiator is directly proportional to the gain in dB. The phases of the half and one-quarter order differentiators are 45° and

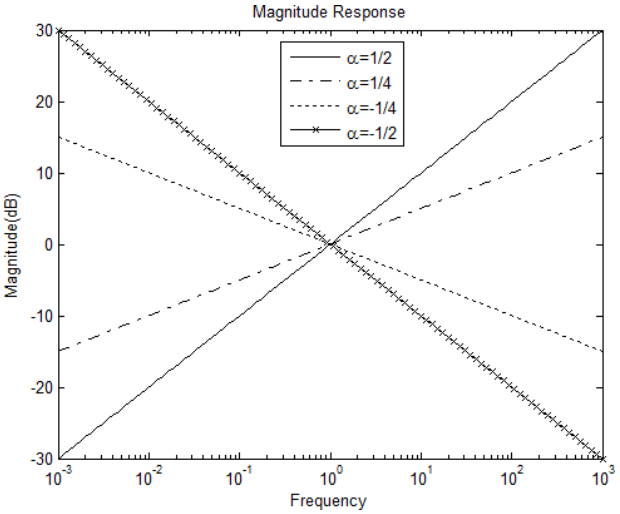

***Fig. 1**: Magnitude response of the fractance device.*

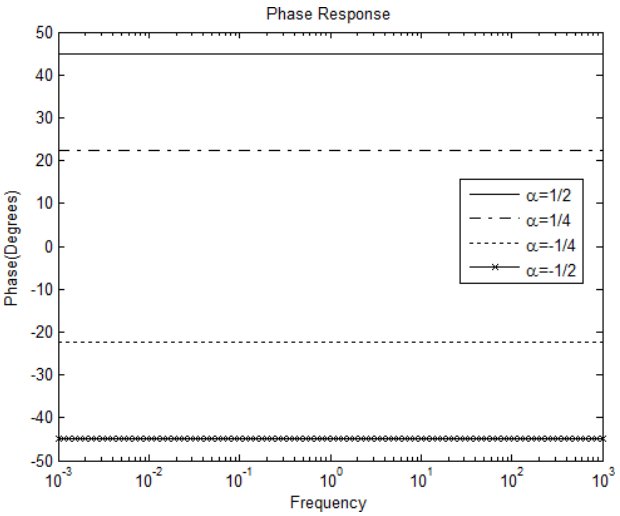

***Fig. 2**: Phase response of the fractance device.*

22.5°, respectively, and −45° and −22.5° for the half and one-quarter order integrators, respectively.

As the fractional order α is changed, the behavior of the fractance device varies. It acts as a resistor when $\alpha=0$. As the value of α varies from −1 to +1, it functions as an inductor and capacitor. Whereas it functions as a frequency dependent negative resistor (FDNR) when $\alpha=2$. As a result, researchers are becoming increasingly interested in its development.

Many different realization approaches are discussed in the literature. The goal of this study is to use the CTE approach to create a fractance device. The circuit is constructed entirely of passive components, while TINA software is used to test and plot the magnitude and phase responses of the proposed circuits.

3. BASIC SYNTHESIS ELEMENTS

3.1 Inverting Amplifier

The gain of the inverting amplifier in Fig. 3 is given as,

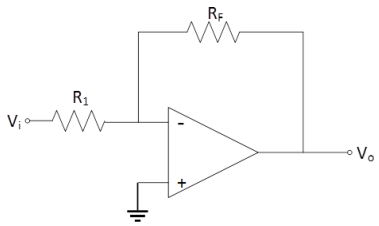

***Fig. 3**: Inverting amplifier.*

$$\frac{V_o}{V_i} = -\frac{R_F}{R_1} \tag{8}$$

3.2 Low-Pass Filter

For the low-pass filter in Fig. 4 the gain is shown to be,

$$\frac{V_o}{V_i} = -\frac{1/R_1C}{s + \left(1/R_FC\right)} \tag{9}$$

3.3 Summing Amplifier

The overall output of the summing amplifier in Fig. 5 is given by,

$$V_o = -\frac{R_{F2}}{R_a}\left(-\frac{R_{F1}}{R_1}V_1 - \frac{R_{F1}}{R_2}V_2 - \ldots - \frac{R_{F1}}{R_n}V_n\right) \tag{10}$$

If $R_{F2} = R_{F1} = R_a = R_1 = R_2 = \ldots = R_n = R$, then the expression simplifies to

$$V_0 = V_1 + V_2 + V_3 + \ldots + V_n \tag{11}$$

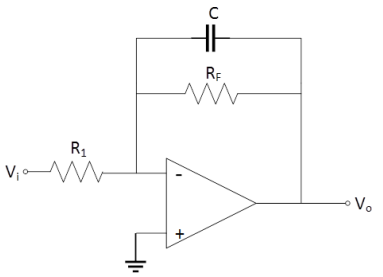

***Fig. 4**: Low-pass filter.*

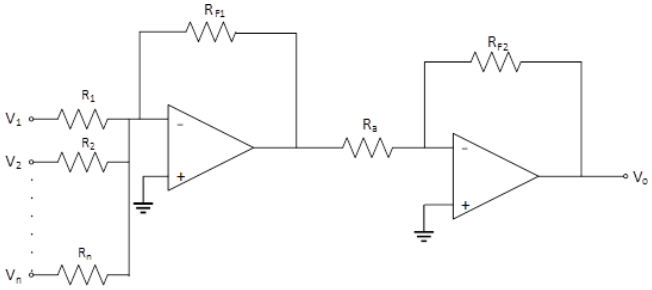

***Fig. 5**: Summing amplifier.*

4. LITERATURE REVIEW

The creation of a fractance device is a fascinating, long-standing topic. For example, $\alpha = 0.507$ is used to model tissue types in the skull, teeth, fruits, and vegetables. The fractional order $\alpha = 0.766$ is used to model sheep intestines, wood, tumor xenografts, and stems. There are numerous approaches to realization, such as finding the rational approximation and realizing the calculated approximation, using either passive or active aspects. Another method of realization involves the capacitor function principle. Nakagawa and Sorimachi investigated the basic properties of the fractance device in [4].

Analog realization of fractional-order controllers was discussed in [5] by Podlubny *et al.* In [5], different methods are discussed for the calculation of rational approximations. The procedure for the realization of negative impedance is also presented. Two types of nested multiple-loop systems can be used for the realization of fractional-order systems and controllers.

Nakagawa and Sorimachi proposed a self-similar tree-type circuit with resistors and capacitors [4]. Fractance devices can take the form of tree, chain, or net-grid networks. In the literature, various recursive structural realizations have been presented, although hardware complexity is a drawback [6]. The cost of realization rises along with the circuit complexity. In [6], a tree-type analog fractance circuit for order $\alpha = 1/2$ is proposed. Three novel analog fractional-order circuits are proposed and compared with each other in this study. It is observed that the half-order net-grid type analog fractance circuit is the best option. These circuits find applications in electronic communication and information processing [6].

The calculation of rational approximation has been discussed by many researchers. To obtain the approximated rational fractional transfer function with integer order, several methods have been attempted. This category includes the CRONE approximation, Oustaloup's approximation, Matsuda's approximation, and many others.

The recursive distribution of zeros and poles is used in Oustaloup approximation [7]. This method is used to produce the approximation in a given frequency range. However, the disadvantage of this method is its poor response at the edges.

The calculation of rational approximation based on the regular Newton process is presented in [8]. The positive realness of the proposed approximations is tested. This paper proposes the realizations of one-third and one-quarter order fractional capacitors. As the order size grows, so does the expense and complexity of this method.

By identifying a model from its gain, the Matsuda methodology provides continuous approximations of fractional plants. Assuming that $F(s)$ [9] is used to approximate a fractional-order operator. The gain must be determined at various frequencies, the level of which defines the number of zeros and poles present in the

approximation; $2M + 1$ frequencies must be utilized for M zeros and M poles. It is advisable to always use an odd number of frequencies; if an even number is used, the number of zeros will equate to the number of poles plus one, and thus the model is not suitable [9].

For the proposed fifth order approximation, the realized circuit is simulated using PSpice in [10, 11], where the rational approximation is calculated using the continued fraction expansion technique. TINA software base simulations are performed in [3], while the time domain magnitude and phase responses of fractional-order integrator circuits are calculated using Multisim software in [2].

The phenomenon occurring in nature can be more accurately modeled using fractional-order calculus. The calculation of the integer-order approximation to a fractional-order operator is a vital step. In [7] four different approximation methods are studied and compared using two different cases, with the results compared in the time and frequency domains. On a fractional-order plant model, the CFE method is applied, and the approximated model converted to its equivalent delta domain model. The step responses are then demonstrated using delta domain and continuous domain models. A complete analysis of four alternative fractional-order operator approximation approaches is offered in this research, along with two separate illustrative cases. The simulation data are also provided so that the quality of various approximation methods may be easily studied. The approximated model will converge to the original model as the order of approximation is increased, resulting in a more accurate fit. The analogous delta domain model is also provided, as well as the simulation results. Based on the findings, it is difficult to identify which of the approximation methods is the best. The relative merits of various approximation methods vary depending on whether exact frequency behavior or accurate time responses are more important.

The goal of the research in [12] was to demonstrate the stability of a regulatory system utilizing a non-conventional corrector, such as the one used in this current study, rather than a traditional corrector system. In a frequency region known as the fractal area, the input impedance of the realized electronic component has a fractional order. This feature suggests that they could be used in the practical implementation of non-integer analogical controllers. In this paper, an electronic component based on Hilbert's fractal structure is used to create a fractional controller with an order of 1/2. The proposed component has been shown to be useful for the realization of 1/2-order fractance in simulations and experiments.

Based on the mixed integer-order genetic algorithm (GA), work carried out in [13] takes a new approach to optimizing the phase and magnitude responses of fractional-order capacitive and inductive elements over a four-decade bandwidth and functioning up to 1 GHz with a low phase error of about 1 GHz. It performs phase optimization in the specified bandwidth with the smallest branch number possible, without the use of negative component values or complicated mathematical analysis. Since commercially available passive component values are standardized and IEC 60063 compliant, no passive element adjustment is necessary [13].

The goal of the study in [14] was to achieve a fractional-order derivative (FD) with an electrical circuit using fractance circuit synthesis. The synthesis of two types of fractance as passive *RC* circuits coupled in an operational amplifier was used to achieve the goal. The FD transfer function was approximated to the integer-order rational transfer function using the Carlson, Cauer, and Foster technique with custom MATLAB instructions using continuous fraction expansion (CFE) and partial fractional expansion (PE). The FD was increased to order 0.9 with electronic realization as a case study and simulation of the analog electronic circuit completed.

In [15] presents a straightforward method for creating fractional-order filters with transfer functions that incorporate Laplace operators of various fractional orders. Based on a fractional-order transfer function that defines low-pass, high-pass, and band-pass filters, the concept relates to the examination of band-pass, band-stop, and all-pass filter functions as a whole, with a curve-fitting-based approach used for approximation. In contrast to the traditional technique, where each fractional-order Laplace operator of the transfer is calculated separately when a function is individually approximated, the key benefit presented is a large reduction in the amount of time it takes to perform [15].

A new implementation of the fractional capacitor (FC) employing passive symmetric networks is proposed in [16]. The symmetric network is subjected to a general analysis independent of the internal impedance composition. The network employs three different internal impedances to provide the FCs needed for responsiveness. These three examples use a series *RC* circuit, an integer Cole-impedance circuit, or a combination of the two. Minimax and least the optimization approaches are used to optimize the network size and values of the passive elements. The proposed realizations are compared to well-known realizations, providing a respectable performance with an approximate phase inaccuracy.

A detailed approach for the analog modeling of fractional-order elements (FOEs) is described in [17]. Unlike most other techniques, this one uses a standard methodology from classical circuit theory. It comprises the synthesis technique for realizing fundamental fractional-order (FO) one-port models as passive *RC* Cauer and Foster form canonical circuits, as well as the realization of a system function by the mathematical approximation of the necessary phase response. Simple realizations of two-port differentiator and integrator models are developed from the described one-ports. Aside from the design technique, examples are presented of circuit schematics and simulation results.

***Table 1**: Rational approximations for fractional order α.*

Terms	$\alpha = 1/2$	$\alpha = 1/3$	$\alpha = 1/4$
2	$\frac{3s+1}{s+3}$	$\frac{2s+1}{s+2}$	$\frac{5s+3}{3s+5}$
4	$\frac{5s^2+10s+1}{s^2+10s+5}$	$\frac{14s^2+35s+5}{5s^2+35s+14}$	$\frac{15s^2+42s+7}{7s^2+42s+15}$
6	$\frac{7s^3+35s^2+21s+1}{s^3+21s^2+35s+7}$	$\frac{7s^3+42s^2+30s+2}{2s^3+30s^2+42s+7}$	$\frac{195s^3+1287s^2+1001s+77}{77s^3+1001s^2+1287s+195}$
8	$\frac{9s^4+84s^3+126s^2+36s+1}{s^4+36s^3+126s^2+84s+9}$	$\frac{91s^4+1001s^3+1716s^2+572s+22}{22s^4+572s^3+1716s^2+1001s+91}$	$\frac{663s^4+7956s^3+14586s^2+5236s+231}{231s^4+5236s^3+14586s^2+7956s+663}$
10	$\frac{11s^5+165s^4+462s^3+330s^2+55s+1}{s^5+55s^4+330s^3+462s^2+165s+1}$	$\frac{52s^5+910s^4+2860s^3+2288s^2+440s+11}{11s^5+440s^4+2288s^3+2860s^2+910s+52}$	$\frac{663s^5+12597s^4+41990s^3+35530s^2+7315s+209}{209s^5+7315s^4+35530s^3+41990s^2+12597s+663}$

The study conducted in [18] shows how an approximation function can be used to create a fractance device. The characteristics of a fractional passive element with a constant phase at a given bandwidth may be obtained from this function, while the *RC* network can be used to realize the approximation functions. Unfortunately, due to its lack of intriguing features and frequency adjustment, the *RC* passive network is not suitable for integration. Consequently, this current work offers the implementation of a fractional device using OTA-C without the use of a resistor. The rational functions are reduced to a series expansion, potentially realized with the OTA-C. The device orders of 0.507 and 0.766 are offered in this article due to their biomedical applications. The magnitudes, phases, and approximation functions are in conformity with the theory. PSpice simulation verifies the accuracy of the results.

The authors in [19] use CFE and rational function approximation approaches to realize fractional-order devices or constant phase elements (CPE). The Cauer network principle was used to create an *RC* ladder network prototype utilizing CFE. The proposed CPE was realized using an *RC* ladder network and signal flow graph (SFG). Operational transconductance amplifiers (OTA) and grounded capacitors were used to create voltage gain circuits and voltage-mode integrators. The proposed CPE was subsequently created using voltage gain circuits and voltage-mode integrators based on SFG. The proposed CPE could be used as both a fractional-order capacitor and inductor. Furthermore, the CPE could be built in any fractional order. By adjusting the OTA bias current, the impedance and operation frequency can be adjusted independently. The proposed fractional-order gadget was used for validation.

In this paper, rational approximation based on the continued fraction expansion method is proposed for the realization of a fractance device. The realization of one-third order rational approximation is also discussed.

5. PROPOSED METHOD

Khovanskiĭ [20] proposed CFE as follows

$$(1+x)^{\alpha} = \cfrac{1}{1-\cfrac{\alpha x}{1+\cfrac{(\alpha+1)\,x}{2+\cfrac{(1-\alpha)\,x}{3+\cfrac{(2+\alpha)x}{2+\cfrac{(2-\alpha)x}{5+\ldots}}}}}} \tag{12}$$

The expansion of s^{α} is obtained by substituting x by $(s-1)$ in the finite complex s-plane from $x=-\infty$ to $x=-1$. FODs and FOIs are obtained for the various fractional orders $\alpha = 1/2$, $1/3$, and $1/4$, etc., by truncating to a finite number of terms. The degree of denominator and numerator polynomials in the generated rational transfer function have been adjusted depending on the truncation order of CFE.

Table 1 lists the analog rational approximations for fractional orders $\alpha = 1/2$, $1/3$, and $1/4$ along with truncation of CFE to finite number terms. The transfer functions for various iterations for half order differentiators and integrators are also listed. The integrator transfer function is obtained simply by interchanging the numerator and denominator terms in the differentiator transfer function. The rational approximations using CFE for one-third and one-quarter differentiators and integrators are listed in Table 1. The magnitude and phase response for the half-order analog differentiator and integrator are shown in Figs. 6 and 7, respectively. From the responses, it is clear that the fifth order rational transfer function matches with the ideal response. As the order of rational transfer function increases, the ideal response is achieved. However, the number of terms, hardware complexity, and cost also increase. Therefore, the optimum value of the order is chosen to compromise both the system performance and hardware requirements.

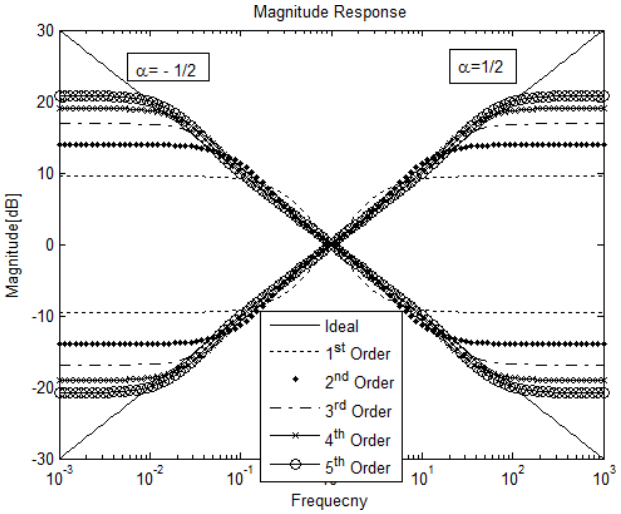

***Fig. 6**: Comparison of the magnitude response for rational approximation of the fractance device.*

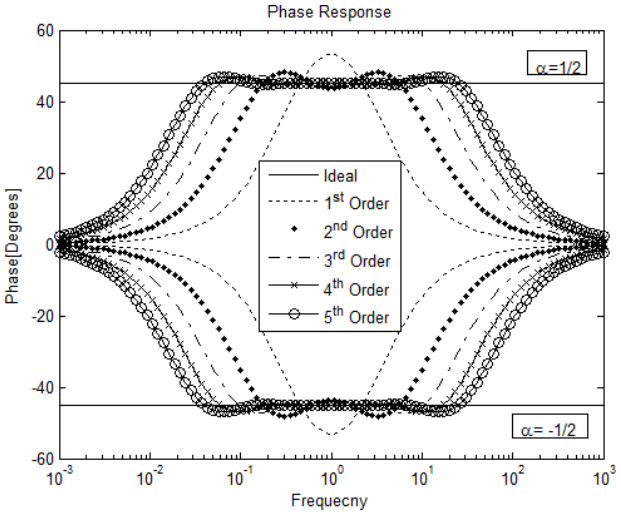

***Fig. 7**: Comparison of the phase response for rational approximation of the fractance device.*

6. REALIZATION OF THE FRACTANCE DEVICE

The fourth order approximation ($\alpha = 1/3$) is given as,

$$H(s) = \frac{91s^4 + 1001s^3 + 1716s^2 + 572s + 22}{22s^4 + 572s^3 + 1716s^2 + 1001s + 91} \quad (13)$$

The pole-zero plot of the above transfer function is shown in Fig. 8.

The following observations are presented:

- The poles and zeros lie on the non-positive real axis.
- They are simple poles and zeros.
- Poles and zeros alternate on the negative real axis.
- The slopes of impedance functions are negative, while those of admittance functions are positive.

The transfer function can be synthesized using *RC* elements. The proposed device can be synthesized using CFE and PFE. The structures derived are Cauer forms and Foster forms, respectively. In this paper,

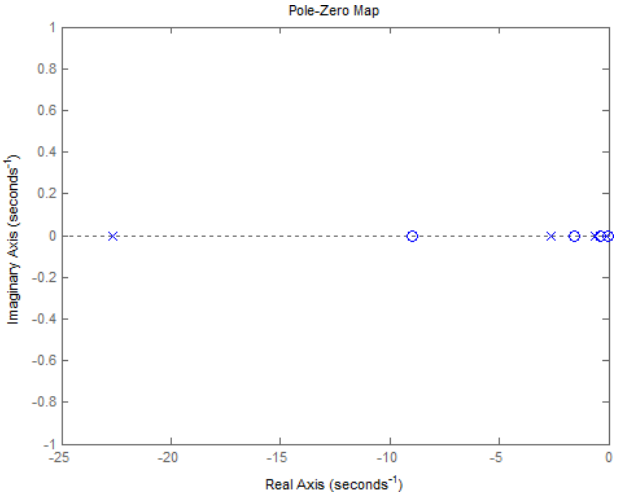

***Fig. 8**: Pole-zero plot of $H(s)$.*

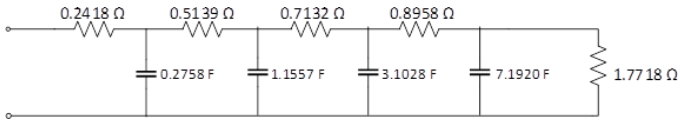

***Fig. 9**: Cauer form I.*

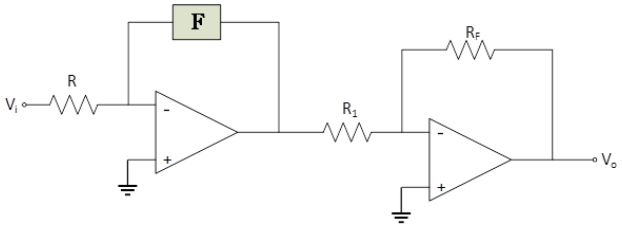

***Fig. 10**: Active realization of Cauer form I.*

active realization is chosen for the realization of Cauer and Foster forms. The following sections explain the synthesis of the fractance device.

6.1 Cauer Form I

On performing the CFE at the point of infinity,

$$H(s) = R_1 + \cfrac{1}{C_2 s + \cfrac{1}{R_3 + \cfrac{1}{C_4 s + \cfrac{1}{R_5 + \cfrac{1}{C_6 s + \ldots}}}}} \quad (14)$$

Eq. (14) shows the CFE of Eq. (13). The passive and active realizations are shown in Figs. 9 and 10, respectively. The response of the sinusoidal signal, square wave signal, and Bode plot are shown in Figs. 11, 12, and 13, respectively. The variation of the output amplitude for different values of R in Fig. 10 is shown in Fig. 14. It can be observed that as the value of the series resistor increases the value of the output amplitude decreases. As a compromise, the value of R in the simulation is chosen to be $10\,\Omega$.

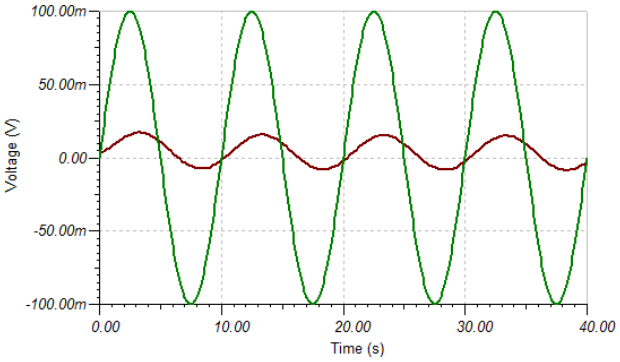

***Fig. 11**: Sinusoidal response of Cauer form I.*

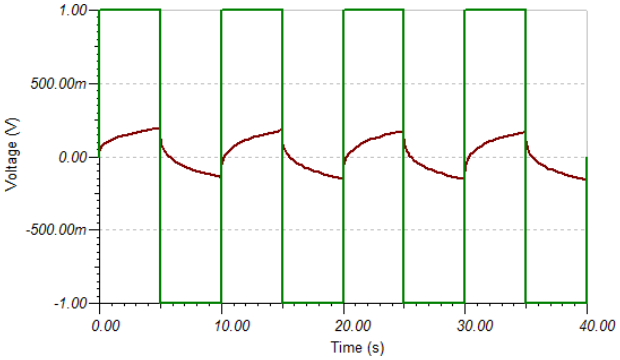

***Fig. 12**: Square wave response of Cauer form I.*

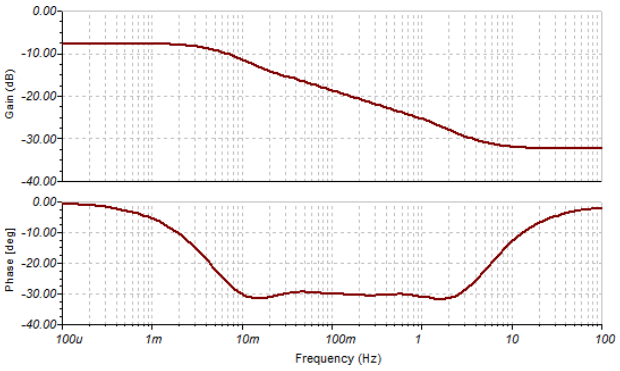

***Fig. 13**: Bode plot of the realized Cauer form I.*

6.2 Cauer Form II

Continued fraction expansion on the origin is performed to achieve the Cauer form II. It can be represented as,

$$H(s) = \frac{1}{C_1 s} + \cfrac{1}{R_2 + \cfrac{1}{C_3 s + \cfrac{1}{R_4 + \cfrac{1}{C_5 s + \cfrac{1}{R_6 + \ldots}}}}} \tag{15}$$

The Cauer form II for the above equation can be represented in circuit form as in Fig. 15.

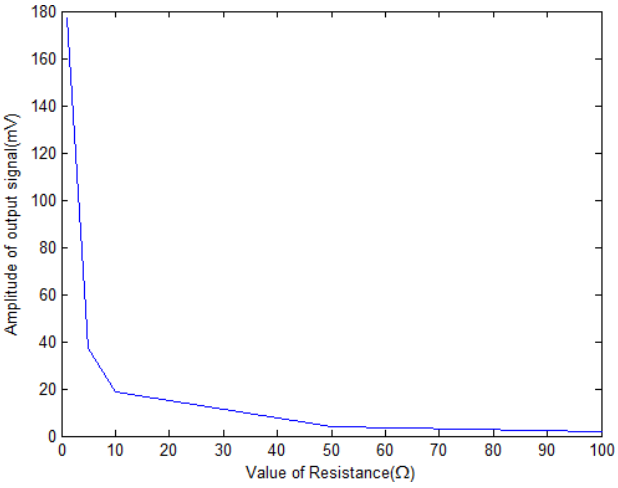

***Fig. 14**: Variation of output with resistance R (V_i = 100 mV).*

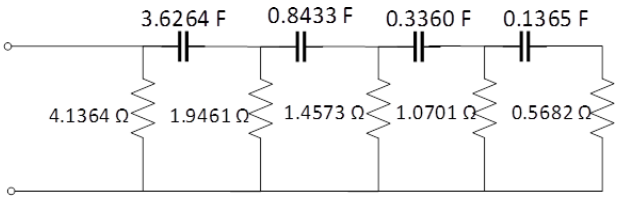

***Fig. 15**: Cauer form II.*

6.3 Foster Form I

The Foster form I is obtained by preforming the PFE of the impedance function. The rational approximation of a fractance device can be expressed as a ratio of two polynomials in s as,

$$H(s) = \frac{a_n s^n + a_{n-1} s^{n-1} + \ldots + a_1 s + a_0}{b_n s^n + b_{n-1} s^{n-1} + \ldots + b_1 s + b_0} \tag{16}$$

where $[a_n, a_{n-1}, \ldots, a_1, a_0]$ and $[b_n, b_{n-1}, \ldots, b_1, b_0]$ are numerator and denominator coeffcients. The above expansion is split into the sum of several first order transfer functions by making use of the PFE, as given below,

$$H(s) = k_0 + \frac{k_1}{s - p_1} + \frac{k_2}{s - p_2} + \ldots + \frac{k_n}{s - p_n} \tag{17}$$

The symbols $k_1, k_2, \ldots, k_n$ are the residues. $p_1, p_2, \ldots, p_n$ are the poles of the function. The above expansion can be put into a compact form as,

$$H(s) = k_0 + \sum_{i=1}^{n} \frac{k_i}{s - p_i} \tag{18}$$

The diagrammatic representation of the compact form is shown in Fig. 16. It is evident that the inverting amplifier, low-pass filter, and summer are necessary for implementing the given function.

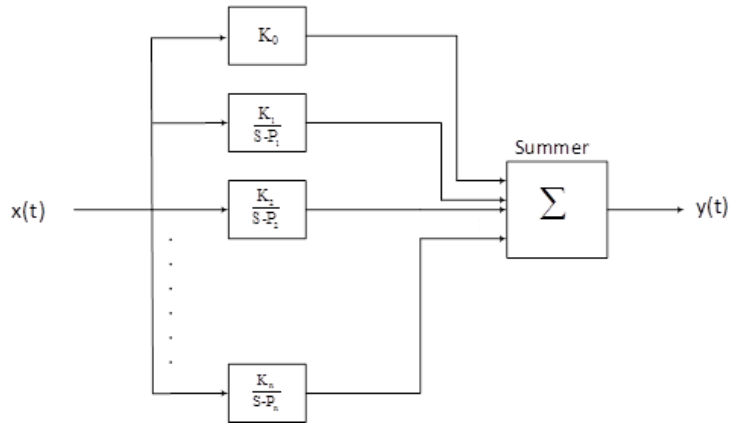

***Fig. 16**: Transfer function representation of Foster form I.*

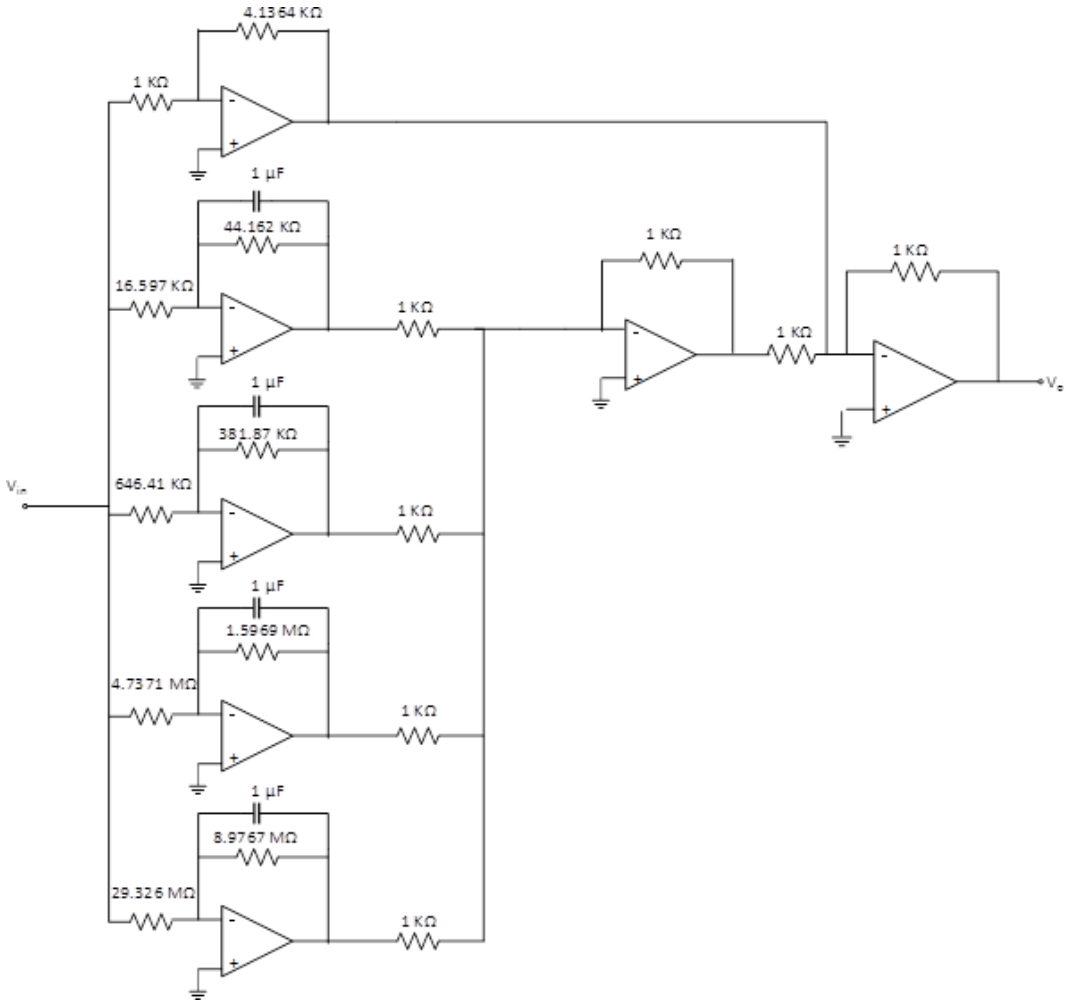

***Fig. 17**: Circuit for Foster form I.*

The transfer function under consideration can be expressed in terms of partial fractions as,

$$H(s) = 4.3164 + \frac{-60.2533}{s + 22.6437} + \frac{-1.5470}{s + 2.6187} + \frac{-0.2111}{s + 0.6262} + \frac{-0.0341}{s + 0.1114} \quad (19)$$

The calculated values of the components are shown in Table. 2. The practical circuit diagram used for simulation purposes is shown in Fig. 17. The output signals for the sinusoidal, square wave excitations are shown in Figs. 18 and 19, respectively. Fig. 20 shows the magnitude and phase responses of the practical circuit under consideration.

***Table 2**: Element values of the 4^{th} order approximation.*

No.	PFE Term	Component Values
1	4.1364	$R_1 = 1\,\text{k}\Omega$ $R_F = 4.1364\,\text{k}\Omega$
2	$\frac{-60.2533}{s+22.6437}$	$C = 1\,\mu\text{F}$ $R_1 = 16.597\,\text{k}\Omega$ $R_F = 44.162\,\text{k}\Omega$
3	$\frac{-1.5470}{s+2.6187}$	$C = 1\,\mu\text{F}$ $R_1 = 646.41\,\text{k}\Omega$ $R_F = 381.87\,\text{k}\Omega$
4	$\frac{-0.2111}{s+0.6262}$	$C = 1\,\mu\text{F}$ $R_1 = 4.7371\,\text{M}\Omega$ $R_F = 1.5969\,\text{M}\Omega$
5	$\frac{-0.0341}{s+0.1114}$	$C = 1\,\mu\text{F}$ $R_1 = 29.326\,\text{M}\Omega$ $R_F = 8.9767\,\text{M}\Omega$

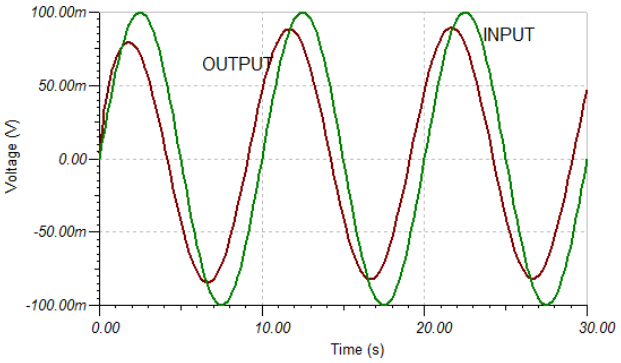

***Fig. 18**: Sinusoidal response of Foster form I (V_i = 100 mV, 100 mHz).*

6.4 Foster Form II

Partial fraction expansion of the admittance function provides the Foster form II. The PFE of $H(s)$, when arranged in the ascending power of s is,

$$H(s) = 0.2418 + \frac{2.7448}{s+8.9771} + \frac{0.5384}{s+1.5969} + \frac{0.2256}{s+0.3819} + \frac{0.1175}{s+0.0442} \tag{20}$$

The realized passive circuit is shown in Fig. 21.

7. CONCLUSION

This paper describes the creation of a fractance device in the order of one-third. The rational approximation is obtained using the CFE approach. The order of the approximation is limited to fourth order due to the hardware complexity. Passive and active circuits are realized. Using an operational amplifier, active realization is achievable. The circuit simulations are carried out utilizing TINA software. The acquired results

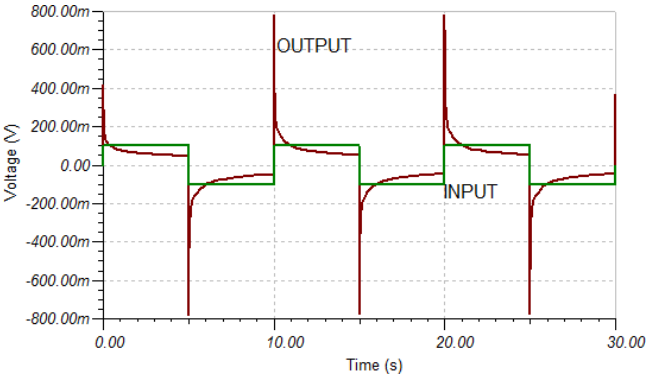

***Fig. 19**: Square wave response of Foster form I (V_i = 100 mV, 100 mHz).*

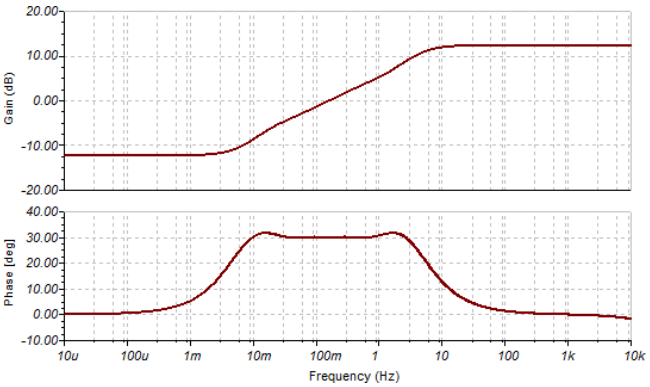

***Fig. 20**: Magnitude and phase response characteristics of Foster form I.*

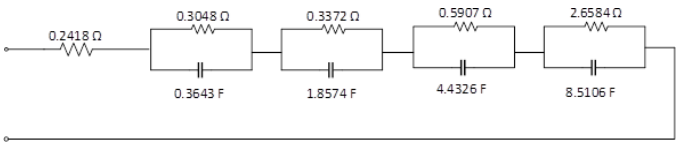

***Fig. 21**: Foster form II.*

are closer to those predicted in theory. The frequency of the input signal is set to 100 mHz. Both square and sine waves are used as inputs, and the responses recorded for the various realized circuits. Both differentiation and integration operations are realized using an operational amplifier.

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