Field Programmable Gate Array-Based Execution on a Distributed Energy Resource Supported Electrical Distribution System for Enhanced Power Quality with Optimal Active Power Flow Control

Jogeswara Sabat[†] and **Mrutyunjaya Mangaraj**, Non-members

ABSTRACT

This paper explains the experimental study of a distributed energy resource (DER) integrated three-phase, three-wire electrical distribution system (EDS) under power quality (PQ) and optimal active power flow control (OAPFC). In this research, a back-to-back connected two-level VSI (BTB-TVSI) based distribution static compensator (DSTATCOM) for unbalanced non-linear load is designed. The aim is to provide better OAPFC in EDS with shunt compensation to maintain a round-the-clock quality power supply for end users. The improved neural network-based adaptive least mean square (ALMS) control algorithms are employed for DSTATCOM. The ALMS control strategy is realized using the SPARTAN-6 field programmable gate array (FPGA) evaluation kit. This research involves the comparative study of a two-level voltage source inverter (VSI) and a BTB-TVSI in terms of their OAPFC capability and robustness in mitigating power quality (PQ) against source current disturbances, low power factor (PF), poor voltage regulation, unbalanced voltage at the point of common coupling (PCC), high switching stress, and issues in the EDS operation. The experimental results demonstrate that the BTB-TVSI using an ALMS controller is able to achieve better dynamic performance and lower total harmonic distortion (THD) under selected/permissible limits in comparison to a conventional VSI.

Keywords: Distributed Energy Resource, DER, Power Quality, PQ, Optimal Active Power Flow Control, OAPFC, Back-to-Back Connected Two-Level Voltage Source Inverter, BTB-TVSI, Distribution Static Compensator, DSTATCOM, Adaptive Least Mean Square, ALMS, Field Programmable Gate Array, FPGA, Power Factor, PF, Total Harmonic Distortion, THD

1. INTRODUCTION

Pollution-free environmental and economic support of modern EDS is credited with the introduction of DER. It addresses the shortage of electrical energy conspicuously generated from a larger share of non-conventional energy resources and avoids losses over long-distance distribution lines. However, this support solves the power quantity issues rather than PQ because almost all connected loads in an EDS are based on solid-state power electronics [1]. They inject current harmonics into the EDS and cause PQ issues at different sections of the system, such as excessive heating in coils, increased copper loss, and electrical magnetic torque in the machine producing mechanical jerk, phase cable damage, unwanted excessive current flow, distribution losses increases and difficulty in running sophisticated medical and industrial equipment [2]. To a certain extent, pollution in the environment by utilizing non-conventional sources is reduced, but, until now, PQ has been lacking [1–3]. In this paper, the importance of power quantity and quality is explained, along with the necessity for the smooth running of a modern EDS.

An intelligent harmonic control device, another name for an active power filter (APF), senses the distortion and supplies compensating current into the EDS to enhance the PQ as a regular component[4]. The VSI is a critical component of an APF, facilitating shunt compensation and acting as a flexible and agile interface between the DER and EDS [2, 4]. The system stability and PQ supply depend upon proper topology configuration and controller design [5, 6]. Generally, in VSI topology, power flow control tends to be reactive for a shunt compensator [6] or OAPFC for a DER integrated VSI [7]. However, in more complex VSI topologies, both active and reactive power controls are achieved. Furthermore, it is necessary to compromise either in shunt compensation or OAPFC. The superior performance of both power flows cannot be achieved simultaneously. Also, this topology has some other disadvantages, such as extra conversion requirements, given that the VSI is a buck converter, unable to arrest circulating current, higher voltage, and current total harmonic distortion (THD) [8, 9]. Higher THDs lead to an increase in PQ issues.

In recent years, bidirectional inverters and the BTB-TVSI configuration of conventional VSIs for wind power systems, microgrids, hybrid electric vehicles, and electric

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The authors are with the Lendi Institute of Engineering & Technology, Vizianagaram, India.

[†]Corresponding author: jogesh.electrical@gmail.com

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drives have become more popular [10–16]. Among these applications, the microgrid integrated BTB-TVSI is more commonly applied because of its simple isolation properties and flexibility [12–15]. The inherent properties of BTB-TVSI configuration are power controllability at both the source and load sides [16]. This research work is thereby motivated to utilize a technique which provides superior OAPFC, including shunt compensation.

Currently, various techniques are available such as the new feedback recurrent neural network [17], Kernel Hebbian Least Mean Square [18], Gradient Descent Back Propagation [19], least mean LMS-based neural network [20], ADALINE Least Mean Square Algorithm [21], and Gradient adaptive variable step least mean square control algorithm [22], etc., to deal with different kinds of power quality issues. From these, adaptive control techniques are conferred in the DSTATCOM to adjust the internal parameter, subject to any disturbances that may occur in the system [23]. The problem with the application of neural networks is the selection of their proper size and topology. These problems become more complex when training a very small error signal. These complexities can be mitigated by implementing an improved neural network with a PI controller [24]. Mathematical modeling is proposed for a single step size, thereby fulfilling weight updating and normalization attributes. It aims to achieve improved performance between the input and output neurons in order to adopt its own learning rule, subject to different parameter variations, irrespective of time. This ALMS algorithm is sufficiently capable of detecting, measuring, and monitoring signal attributes such as amplitude, power factor, and frequency. It also facilitates simultaneous smooth operation between analog components and the digital signal processor in real-time applications [23, 24].

In view of previous research works and their merits based on the BTB-TVSI, in this paper, a DER integrated BTB-TVSI with a self-supported capacitor is proposed. Theoretical and experimental studies have revealed useful applications for the proposed topology in three-phase EDS with some important benefits such as reduced harmonic distortion, facilitating sinusoidal source currents, active power supplies to the EDS when the main source fails, shunt compensation by both inverters, flexibility, and simple isolation properties. The principal feature of the BTB-TVSI model is its ability to enhance the capabilities of OAPFC, fault ride-through, and robustness against grid anomalies while maintaining a power quality that complies with international grid codes.

The above benefits of a BTB-TVSI enable it to serve as a multi-functional inverter. A BTB-TVSI with a DC link can supply the full output power to its linear or non-linear load while controlling the real and reactive power drawn from the DER. Their high overall efficiency identifies these topologies as promising solutions in the future use of three-phase three-wire low and medium voltage EDS. The objective of the BTB-TVSI topology is as follows:

(i) The proposed configuration is very useful for weak EDS end users, where the EDS suffers from both power quantity and quality issues.
(ii) It reduces the switching stress and is less dependent on fossil fuel usage, balance voltage at PCC, PF correction and source current shaping.
(iii) An ALMS control technique has adaptive abilities that are attained under any loading scenarios.
(iv) This topology allows for the preservation of the system dynamics at low frequency and noise rejection. Consequently, the corresponding apparel advantages are obtained, such as greater accuracy in the sensing of reference signals and one cycle control to update the weighted values closer to the target value at a faster rate.
(v) Reliability of the EDS operation is increased due to continuous PQ supply.

This paper proposes BTB-TVSI using an ALMS control algorithm to ensure stability, robustness, and increased system performance. In Section 1, the BTB-TVSI, which is connected between the DER and EDS circuit, is presented and its operation explained in detail. Section 2 shows the power circuit design of the BTB-TVSI. The proposed ALMS control scheme and its design are shown in Section 3, while Section 4 presents the experimental results, and finally, the conclusion is provided in Section 5.

2. MODELING OF THE BTB-TVSI-BASED DSTATCOM SYSTEM

2.1 Circuit Description

The structure of a three-phase BTB-TVSI system, based on DSTATCOM architecture and encompassing all the aforementioned capabilities, is illustrated in Fig. 1. This configuration is chosen to prove the power flow control capability. The variable non-linear load (uncontrolled bridge rectifier with R-L) drawing the load currents (i_{la}, i_{lb}, i_{lc}) is connected to the three-phase balanced source which injects (i_{sa}, i_{sb} and i_{sc}) source currents through the distribution line impedance Z_s. The self-supported capacitor connected to the BTB-TVSI is coupled with the PCC via the interface compensating impedance Z_c. In the laboratory, the DER is a three-phase AC source connected to the BTB-TVSI through a rectifier across the common DC voltage V_{dc} of both VSIs. The compensating currents (i_{ca}, i_{cb}, i_{cc} for VSI-1 and i'_{ca}, i'_{cb}, i'_{cc} for VSI-2) are controlled by DSTATCOM to compensate the reactive power. Generation of the schematic switching signal using the ALMS control algorithm is described in Section 3. The proposed topology configuration underlines the effectiveness of the proposed scheme.

2.2 Power Flow Control

The two VSIs are connected back-to-back in between the DER and EDS. As soon as the PQ issues of the EDS are detected, the BTB-TVSI provides shunt compensation to improve the quality. The DER is connected to

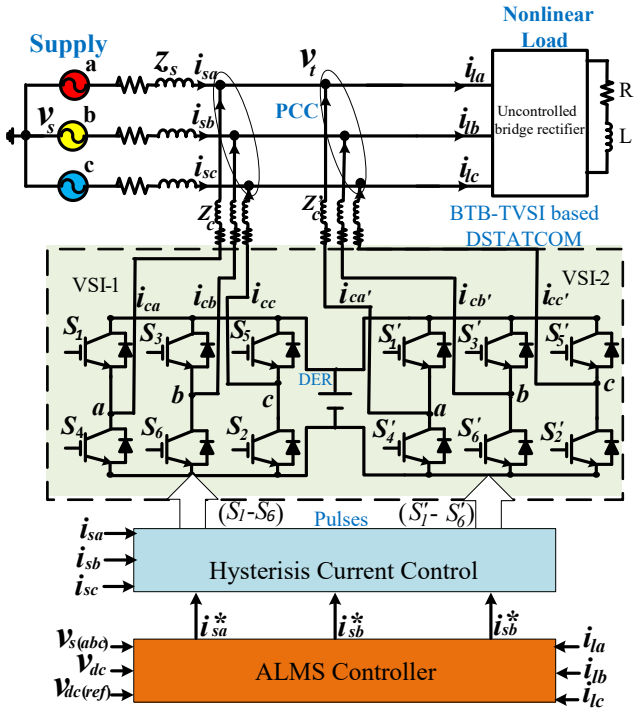

Fig. 1: Circuit diagram of the BTB-TVSI-based DSTATCOM using the proposed ALMS control method.

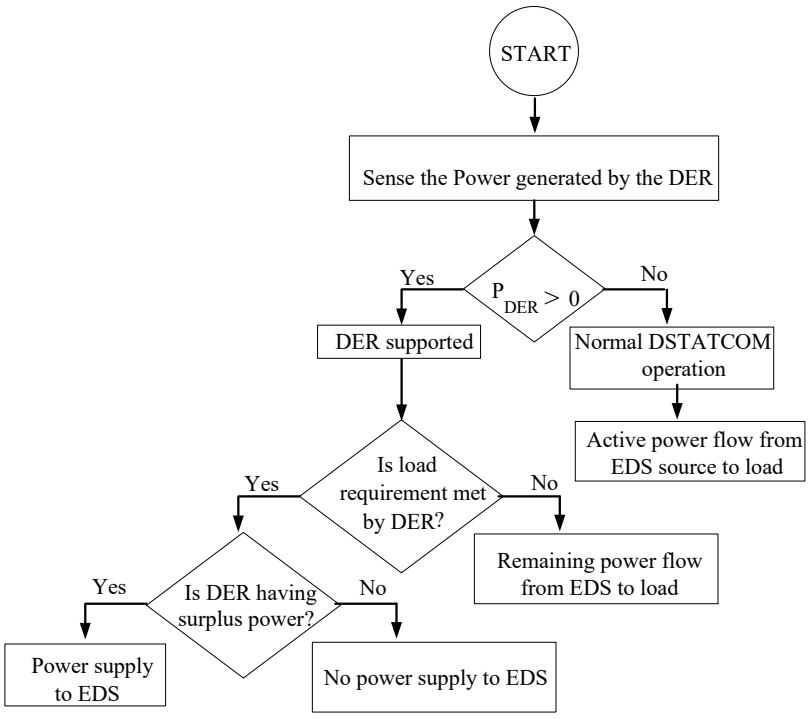

Fig. 2: Flow chart representing the power flow control of the proposed topology.

the rectifier through an isolation transformer and the output of the rectifier coupled with the DC link of the BTB-TVSI. As the EDS is connected to the DER, the power generated by the DER feeds into the EDS in the sequence shown in the flow chart (Fig. 2). On the other hand, the BTB-TVSI connected to the normal EDS will act as a shunt compensator to minimize the harmonic distortion, balance the unbalanced components in the source current, shunt compensation, improve the voltage regulation, and perform voltage balancing at the PCC.

2.3 Parameter Design

2.3.1 Design of L_f

The filter inductance L_f, is designed using the formula presented in Eq. (1). Its role is to remove the switching frequency component from both the VSI-1 and VSI-2 currents.

$$L_f = \frac{V_{DC}}{4hf_{\max}} \tag{1}$$

where h is the hysteresis band, taken as 5% of the compensation current and $f_{\max}$ is the maximum switching frequency.

2.3.2 Design of C_{DC}

The rating of the DC link capacitors C_{DC} is designed using Eq. (2). During the transient period, it stores energy and the DC ripple.

$$C_{DC} \geq \frac{S}{2\omega V_{DC}\Delta V_{DC}} \tag{2}$$

where S is the rating of an individual inverter, V_{DC} is the DC link voltage, ω is the system frequency and ΔV_{DC} is the peak-to-peak DC link voltage ripple.

2.3.3 Design of V_{DC}

Using Eq. (3), the minimum value of the DC link voltage $V_{DCminimum}$ can be calculated [25].

$$V_{DCminimum} = \sqrt{2} \times V_s \tag{3}$$

where V_s is the peak value of the phase voltage.

Using Eq. (4), the maximum value of the DC link voltage $V_{DCmaximum}$ can be calculated.

$$V_{DCmaximum} = 1.5 \times \sqrt{2}V_s \tag{4}$$

The rating of the DC link voltage is selected using the average minimum and maximum values.

2.4 Novelties of the Proposed System

The novelties of this paper, as compared with VSI based on theoretical and experimental results, are summarized as follows:

(i) The filtering capability of the proposed BTB-TVSI is superior to VSI by maintaining the source current shape as suggested by the standard international grid code (IEEE Std 1159-2009) [26–28].
(ii) It provides real power round the clock to the clients of EDS with a smooth operation.
(iii) The maximum capacity of the BTB-TVSI is utilized, which, in turn, increases the efficiency of the inverter and system.
(iv) The key highlight of this work is that both inverters have the power control capability to increase the reliability of the EDS.
(v) In this system, if any fault arises in one inverter, it can be easily isolated, and the operation of the system will continue without complete shutdown by providing a two-way current path.
(vi) Single topology with dual operation: The proposed topology has dual operation (real power injection and PQ enhancement), which increases the utilization factor corresponding to the DER supported BTB-TVSI based DSTATCOM in the three-phase EDS.

3. PROPOSED METHOD FOR PQ IMPROVEMENT WITH OAPFC

3.1 ALMS Control Algorithm

The structural diagram of the ALMS control algorithm is displayed in Fig. 3. Here, the ALMS algorithm is discussed briefly by considering the different weighting parameters such as learning rate, step size, unit input weights, bias, etc. The main purpose is to provide an individual phase tuned weight corresponding to the real fundamental frequency component of the load current [21].

The learning mechanism of the ALMS algorithm is expressed in the following iteration:

1. The updating weights (w_{pa}, w_{pb}, w_{pc}) of the active part of the load current are calculated as:

$$w_{pa}(n) = \alpha\gamma\left\{i_{la}(n) - w_{pa}(n-1)\,u_{pa}(n)\right\}u_{pa}(n) + w_{pa}(n-1) \tag{5}$$

$$w_{pb}(n) = \alpha\gamma\left\{i_{lb}(n) - w_{pb}(n-1)\,u_{pb}(n)\right\}u_{pb}(n) + w_{pb}(n-1) \tag{6}$$

$$w_{pc}(n) = \alpha\gamma\left\{i_{lc}(n) - w_{pc}(n-1)\,u_{pc}(n)\right\}u_{pc}(n) + w_{pc}(n-1) \tag{7}$$

2. The updating weights (w_{qa}, w_{qb}, w_{qc}) of the reactive part of the load current are calculated as:

$$w_{qa}(n) = \alpha\gamma\left\{i_{la}(n) - w_{qa}(n-1)\,u_{qa}(n)\right\}u_{qa}(n) + w_{qa}(n-1) \tag{8}$$

$$w_{qb}(n) = \alpha\gamma\left\{i_{lb}(n) - w_{qb}(n-1)\,u_{qb}(n)\right\}u_{qb}(n) + w_{qb}(n-1) \tag{9}$$

$$w_{qc}(n) = \alpha\gamma\left\{i_{lc}(n) - w_{qc}(n-1)\,u_{qc}(n)\right\}u_{qc}(n) + w_{qc}(n-1) \tag{10}$$

3. The average weight (w_a) of the active component is calculated as:

$$w_a = \frac{w_{pa} + w_{pb} + w_{pc}}{3} \tag{11}$$

4. Similarly, the average weight (w_a) of the reactive component is calculated as:

$$w_r = \frac{w_{qa} + w_{qb} + w_{qc}}{3} \tag{12}$$

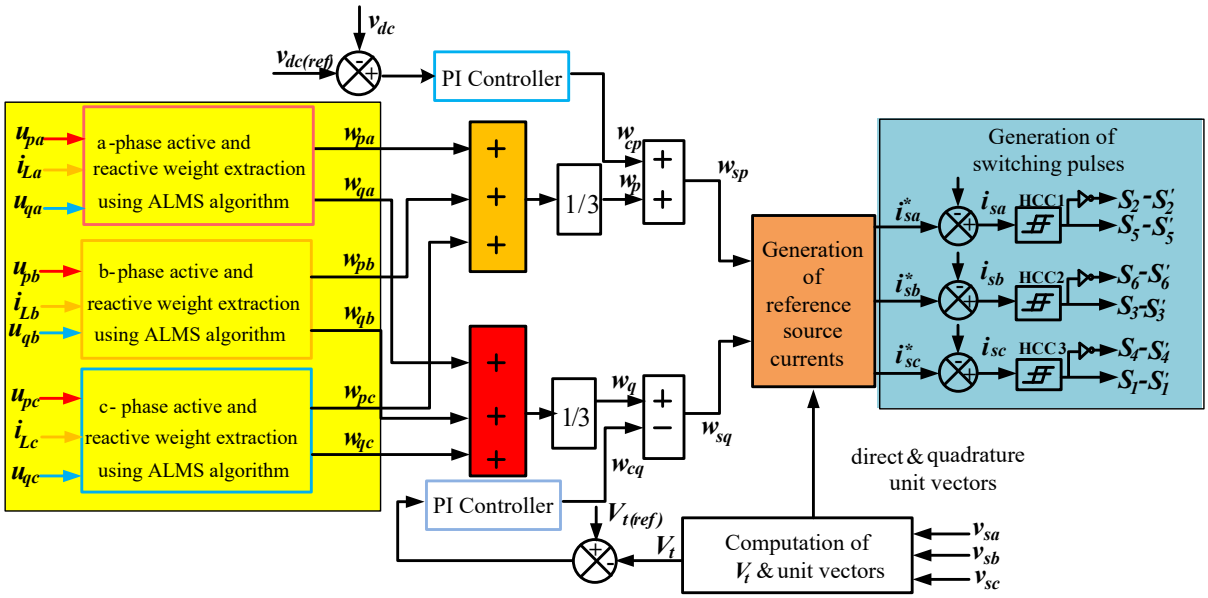

Fig. 3: *Generation of reference source current using the ALMS technique.*

3.2 Computation of In-Phase and Quadrature Unit Voltage Template

Active unit voltage templates (u_{pa}, u_{pb}, u_{pc}) are estimated as:

$$\begin{aligned} u_{pa} &= \frac{v_{sa}}{v_t} \\ u_{pb} &= \frac{v_{sb}}{v_t} \\ u_{pc} &= \frac{v_{sc}}{v_t} \end{aligned} \tag{13}$$

Similarly, the reactive unit voltage templates (u_{qa}, u_{qb}, u_{qc}) are estimated as:

$$\begin{aligned} u_{qa} &= \frac{u_{pb} + u_{pc}}{\sqrt{3}} \\ u_{qb} &= \frac{3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}} \\ u_{qc} &= \frac{-3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}} \end{aligned} \tag{14}$$

where v_t can be expressed as:

$$v_t = \sqrt{\frac{2\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2\right)}{3}} \tag{15}$$

3.3 Estimation of the Active Component of the Reference Source Currents

The difference between the referenced and sensed DC voltage is the error in DC voltage (v_{de}), which can be expressed as

$$v_{de} = v_{dc(ref)} - v_{dc} \tag{16}$$

This difference is processed through the proportional-integral (PI) controller to control the constant DC bus voltage [21, 24]. The output of the PI controller can be expressed as:

$$w_{cp} = k_{pa} v_{de} + k_{ia} \int v_{de} dt \tag{17}$$

The active component of the reference source current is determined as:

$$w_{sp} = w_a + w_{cp} \tag{18}$$

3.4 Estimation of the Reactive Component of the Reference Source Currents

The ac voltage error (v_{te}) is determined by subtracting the sensed amplitude of the PCC from the reference ac voltage, calculated as:

$$v_{te} = v_{t(ref)} - v_t \tag{19}$$

The output of the PI controller can be expressed as [21]

$$w_{cp} = k_{pr} v_{te} + k_{ir} \int v_{te} dt \tag{20}$$

The reference source current is obtained by subtracting the average magnitude of the reactive component of the load current from the output of the AC side PI controller, thus;

$$w_{sq} = w_r + w_{cq} \tag{21}$$

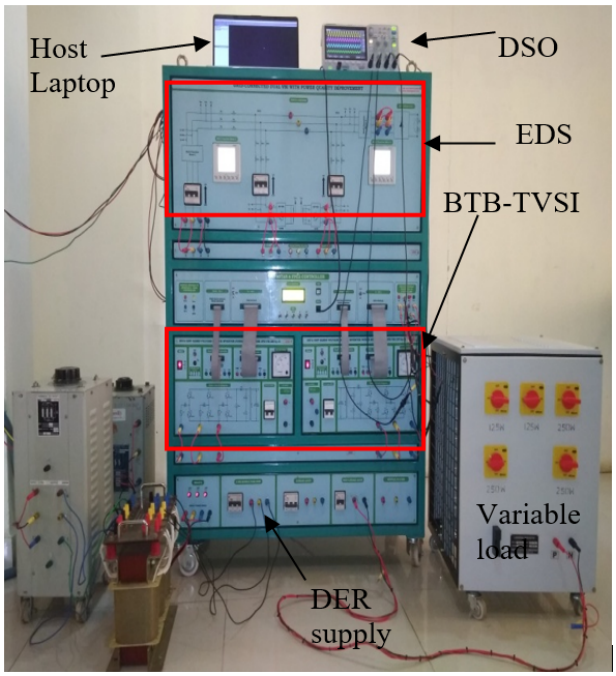

Fig. 4: *Hardware unit of the proposed topology with different apparatus.*

3.5 Estimation of Switching Signal Generation

The three-phase instantaneous reference source active component is calculated as:

$$\begin{aligned} i_{aa} &= w_{sp}u_{pa} \\ i_{ab} &= w_{sp}u_{pb} \\ i_{ac} &= w_{sp}u_{pc} \end{aligned} \tag{22}$$

Similarly, the three-phase instantaneous reference source reactive component is calculated as:

$$\begin{aligned} i_{ra} &= w_{sq}u_{qa} \\ i_{rb} &= w_{sq}u_{qb} \\ i_{rc} &= w_{sq}u_{qc} \end{aligned} \tag{23}$$

The summation of the active and reactive components of the current are the reference source currents, obtained as:

$$\begin{aligned} i^*_{sa} &= i_{aa} + i_{ra} \\ i^*_{sb} &= i_{ab} + i_{rb} \\ i^*_{sc} &= i_{ac} + i_{rc} \end{aligned} \tag{24}$$

Both the actual source currents (i_{sa}, i_{sb}, i_{sc}) and reference source currents (i^*_{sa}, i^*_{sb}, i^*_{sc}) of the respective phases are compared and the current error signals subsequently fed to a hysteresis current controller (HCC). Their outputs are used to feed the insulated-gate bipolar transistors (IGBTs) S_1 to S_6 of the VSI-1 and S'_1 to S'_6 of the VSI-2 serving as a BTB-TVSI-based DSTATCOM.

Table 1: *Apparatus values of the hardware unit.*

Input elements	Values
Source voltage	200 V/phase
Source current	10 A
DER voltage	415 V (line to line)
Fundamental frequency	50 Hz
Source resistance	5 Ω
Source inductor	5 mH
Output elements	
Non-linear load	3-Ø diode bridge rectifier with *R-L*
Load inductance	60 mH
Variable load	1 kW
Diode no.	MUR30120
Diode rating	1200 V/30 A
Filter elements	
Compensator inductance	5 mH
Other elements	
Three-phase auto-transformer (2 No)	5 kVA, 10 A
Isolation transformer	5 kVA/10 A

4. EXPERIMENTAL EVALUATIONS

4.1 Apparatus and Hardware Unit Description

The proposed topology circuit configuration in Fig. 1 is designed to investigate the validation of the proposed scheme. In order to verify the effectiveness of the BTB-TVSI, an experimental unit is built with a field programmable controller array (FPGA) for experimental verification, as shown in Fig. 4.

In this work, a balanced three-phase AC source is utilized as the three-phase DER power and EDS power, the frequency and voltage of which are 50 Hz and 415 V (line voltage), respectively. The BTB-TVSI consists of two-level VSIs, with the main circuit of the VSI being a three-phase DSTATCOM, choosing IGBT as the main circuit switching device. The signal testing point unit consists of hall effect voltage sensors (7840IC) and hall effect current sensors (HE055T01(55A)) to collect the corresponding voltage and current signals. These signals are obtained from the FPGA SPARTAN-6 controller through analog to digital in the testing point section of the hardware setup. The control technique is developed in XILINX SP6 LX25 and converted for implementation in the FPGA hardware interface toolbox. These signals are then sent out to the IGBT driver (SKYPER 32R) by 20 pin FRC cables to the individual VSI. The non-linear loads are composed of a three-phase uncontrolled bridge rectifier with *R-L* load, the details of the parameters used in the load are shown in Table 1. The signal circuits and driver circuits are supplied by a DC auxiliary power source. Two multifunction meters (MFMs) are connected at the source and load sides of the EDS for voltage, current, THD, PF, and power measurement applications. A four-channel digital storage oscilloscope (DSO) (SIGLENT,

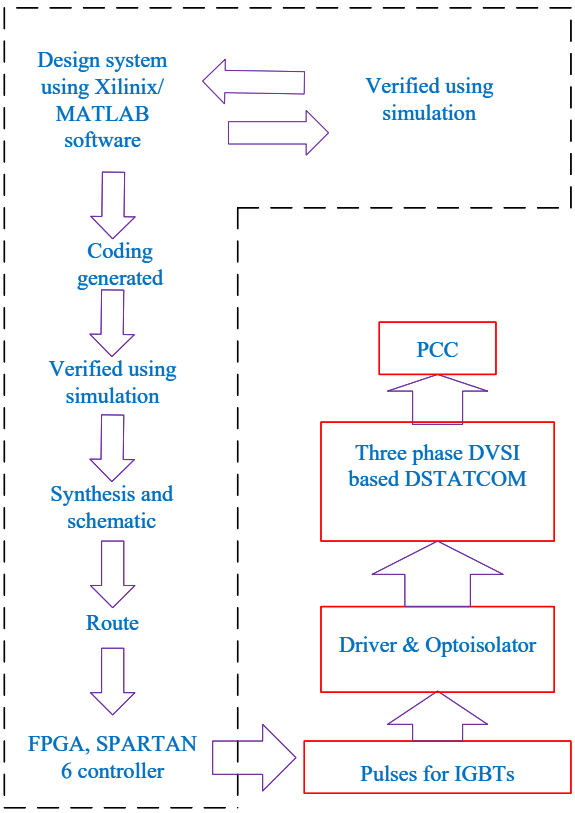

Fig. 5: *Flow chart of the pulse generation process.*

SDS1104X-E-5100) is used to record voltage and current waveforms, in which yellow, pink, blue, and green are marked for channels 1, 2, 3, and 4, respectively. Two auto-transformers are connected at the input side of the DER and EDS to perform the experiment at different laboratory scales. An isolation transformer is connected between the DER output and the BTB-TVSI input for ease of isolation and protection purposes.

The step-by-step procedure of switching signal generation for IGBT using the FPGA SPARTAN-6 controller is shown in Fig. 5. Different MCB ratings and MCCB are connected for circuit protection at different input AC and DC source sides, such as the three-phase main supply, EDS, DER, and BTB-TVSI.

4.2 Performance Evaluations of VSI-Based DSTATCOM

The EDS-connected VSI performance associated with PQ issues is demonstrated in Fig. 6. The experimental waveform of three-phase supply voltages, phase-a supply voltages with three-phase source currents before compensation, and phase-a supply voltages with three-phase load currents after compensation are shown in Figs. 6(a)–6(c).

The phase relationships between the phase-a source voltage and the corresponding source current and DC link voltage and current of a single VSI are shown in Figs. 6(d)–6(e). It can be observed that the ALMS controller is able to compensate the source current harmonics as per the suggested grid code. The experimental waveforms are under non-linear load conditions when the VSI-based DSTATCOM is not in operation, and therefore, whatever load current draw is supplied from the EDS only. The waveform initially from the EDS supplies the non-linear load demand. When DSTATCOM is switched on, the source currents become perfectly sinusoidal and in phase with the source voltages, as shown in Fig. 6(d).

Fig. 6(e) shows the DC link voltage and currents, where initially, some disturbance in the DC link voltage can be observed for a transient period, but after that, it becomes stable and constant at 610 V. Distortion is found in the load current (28.9%) and source current (28.7%) before compensation. As can be observed, after compensation, the three-phase source currents THDs are reduced to 7.8, 0.0, 5.8, and 4.5% on average, respectively, as shown in Fig. 6(f). The average PF after compensation is 0.984.

4.3 Performance Evaluation of BTB-TVSI-Based DSTATCOM

The experimental waveform shows that the ALMS controller is able to compensate the source current harmonics as per the suggested grid code with OAPFC at the EDS from DER through BTB-TVSI. After DSTATCOM is switched on, the profile of the source currents becomes sinusoidal and distortion-free in nature, as shown in Fig. 7(a). The phase angle between the source voltage and

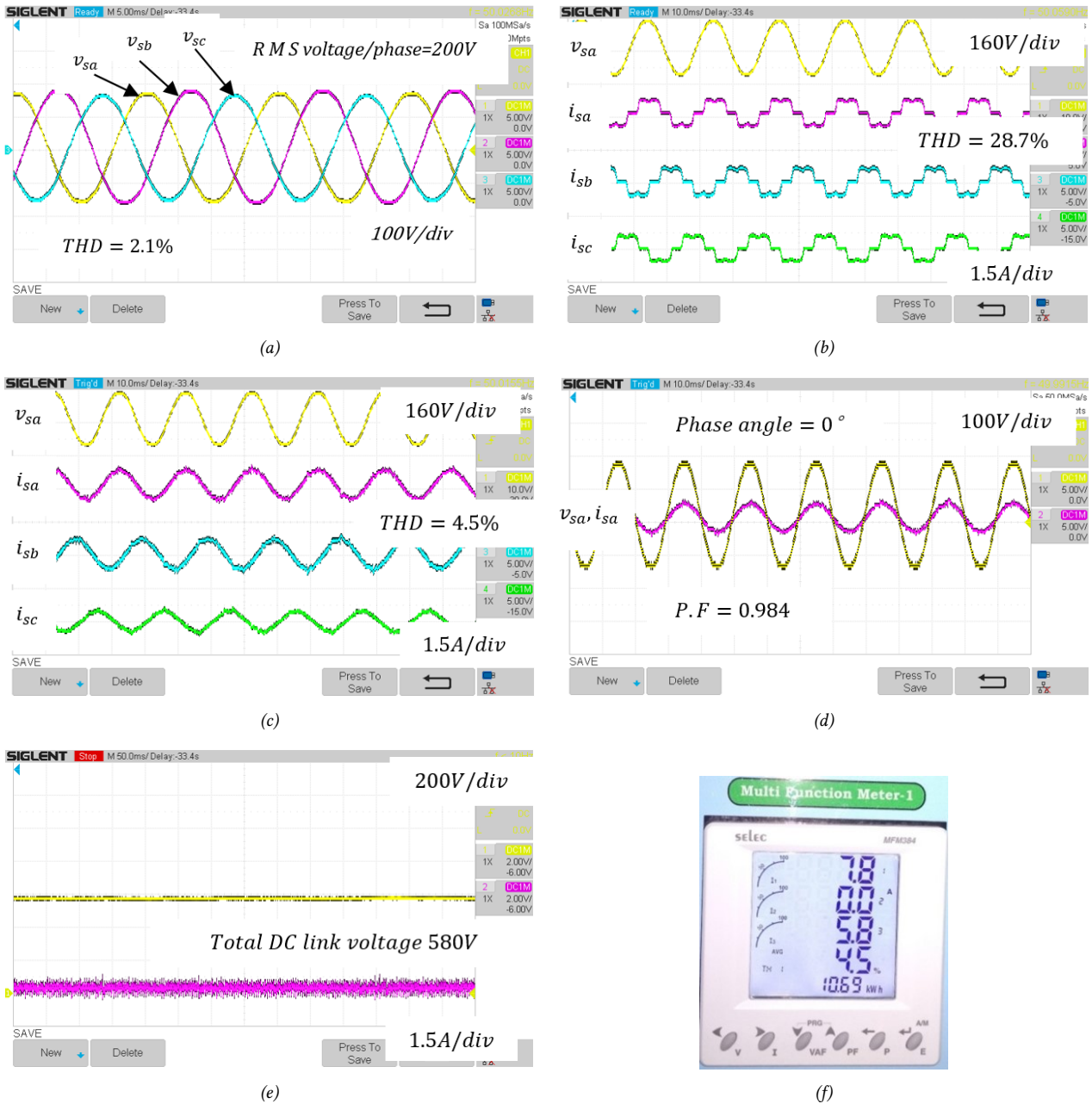

***Fig. 6**: Experimental results: (a) three-phase source voltage; (b) phase-a source voltage and three-phase source currents before compensation; (c) phase-a source voltage and three-phase source currents after compensation; (d) phase-a source voltage and current after compensation; (e) DC link voltage and DC link current; and (f) after compensation source side THD measurement using a multifunction meter.*

current of phase-a is 180°, as shown in Fig. 7(b).

Fig. 7(c) shows the DC link voltage of the BTB-TVSI. During operation, the stable voltage of the BTB-TVSI is 650 V. Specification of the BTB-TVSI-based DSTATCOM is illustrated in Table 2. Fig. 7(d) shows the dynamic system performance, during DER supported mode, with the load demand being supported by the DER-generated power. Hence, when the load demand increases, the source current decreases.

In Fig. 7(e), channel-1 represents the phase-a supply voltage, channel-2 represents the phase-a supply current, channel-3 represents the phase-a load current, and channel-4 represents the phase-a compensating current waveforms. It shows the grid injection mode, in which the proposed system not only compensates the reactive power but also supplies the active power to load demand and surplus power injection to the EDS. It contains both an active and reactive component, and the phase angle between the source voltage and source current of the corresponding phase is 180°. Thus, the waveform of the VSI supply current after compensation with the BTB-TVSI seems asymmetrical. The performance of

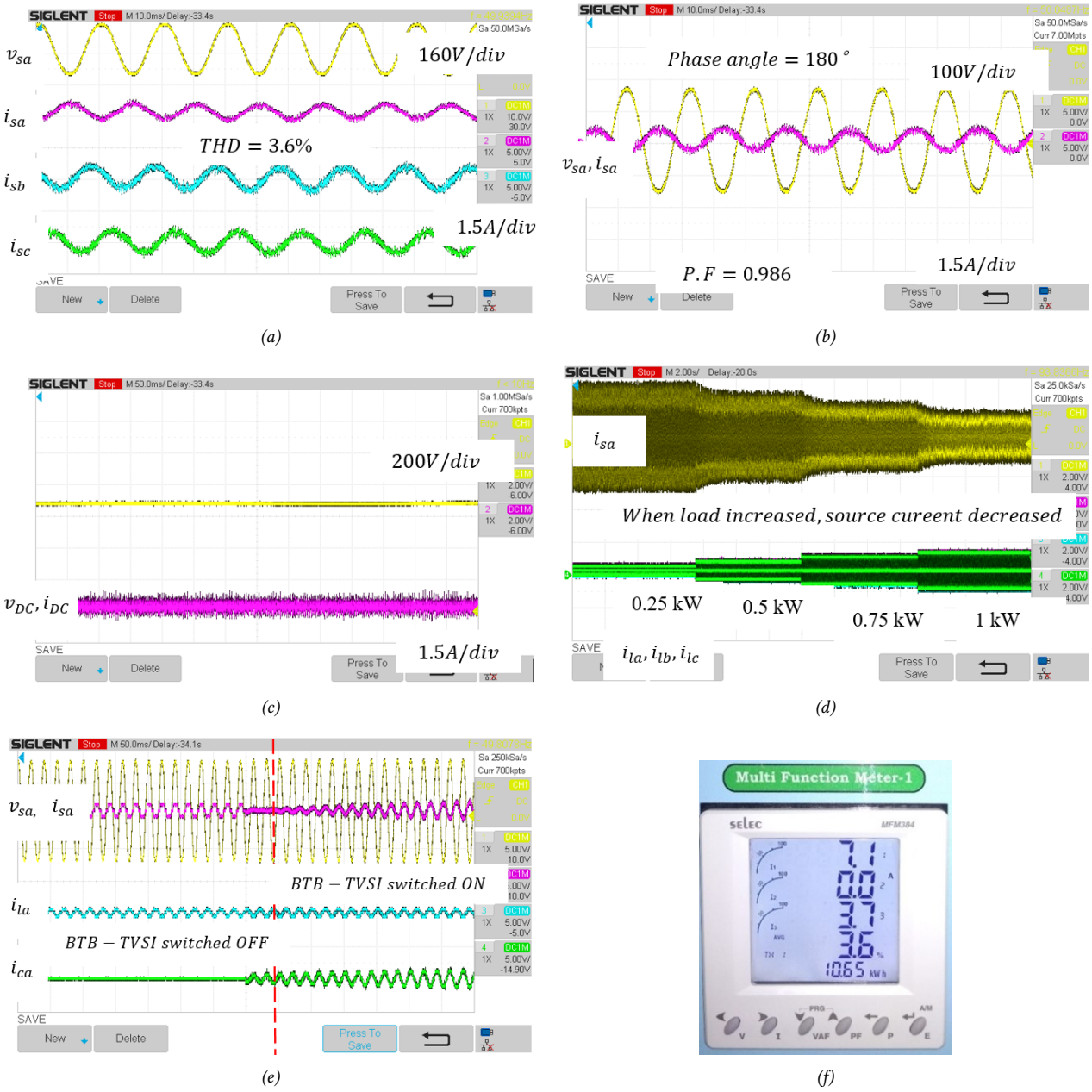

***Fig**. 7: Experimental results: (a) phase-a source voltage and three-phase source currents after compensation; (b) phase-a source voltage and current after compensation, (c); DC link voltage and DC link current; (d) dynamic performance of BTB-TVSI; (e) before and after the compensation performance of the BTB-TVSI-based DSTATCOM; and (f) after compensation of the source side THD measurement using a multifunction meter.*

the BTB-TVSI shows that even after the load change, the displacement power factor is improved. After compensation, the three-phase source currents (THDs) are reduced to 7.1, 0.0, 3.7, and 3.6% on average, as shown in Fig. 7(f). The average PF after compensation is 0.986.

Graphical analysis of the source current and load current THD of the VSI and BTB-TVSI topologies are depicted in Fig. 8.

In the case of the BTB-TVSI, in comparison to the VSI, the DC link voltage increases, but when considering the merits of the former, this increase in voltage can be neglected. To achieve better voltage regulation at the DC side, the actual and reference DC link voltage are considered, while for the AC side, the PCC voltage and reference AC voltage are considered. The detailed voltage regulation is explained in Eqs. (16)–(21) of the control section. The total load current supplied by the BTB-TVSI is divided by VSI-1 and VSI-2. Hence, the switching stress and filter sizes of the BTB-TVSI are reduced in comparison to the VSI. The operation of BTB-TVSI consists of dual inverters with power control capability, which increases the reliability of the EDS. Since the reliability, robustness, and tuning of the BTB-TVSI using an ALMS control technique is better, it shows

Table 2: *Specification of the BTB-TVSI.*

Parameters	Magnitude
VSI rating	2 kVA
IGBT no.	SKM100GB12T4
IGBT rating	1200 V/100 A
Switching frequency	20 kHz (max)
Driver no.	SKYPER32R
Current sensor	4no's, 55 A
Voltage sensing	1no's, 750 V
DC link voltage	750 V (max)

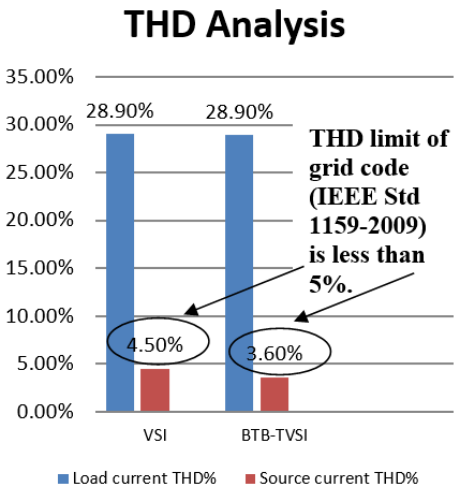

Fig. 8: *Analysis of supply current and load current THD of VSI and BTB-TVSI .*

improved stability in comparison to the VSI.

Therefore, the above experimental waveform and different parameters measurement of VSI-based DSTATCOM and BTB-TVSI-based DSTATCOM shows that the proposed topology performs better than VSI. It also provides reliable and flexible services in relation to shunt compensation and DER integration application in a three-phase EDS. The performance comparison of both topologies between different parameters is given in Table 3.

5. CONCLUSION

The improved ALMS controller for the control of a BTB-TVSI is presented in this paper. From the experimental results, it can be observed that the suggested controller has better shunt compensation capability and additional OAPFC ability with a BTB-TVSI in comparison to a VSI. Key advantages of the proposed ALMS control solution are as follows:

(i) The topology configuration is designed using a dual VSI but has the ability to operate in a standalone capacity which increases the reliability of the system.

(ii) Generates a noticeable THD reduction from 4.5% to 3.6% in the source side when a BTB-TVSI is used instead of a VSI and supported the EDS for normal operation.

(iii) Round-the-clock power supply to the client of the EDS even after a source side failure since it is supported by DER.

(iv) The ALMS control solution is easy to implement, which is an important criterion in practical application.

(v) It is the first time an ALMS control solution has been applied to a back-to-back configuration of a VSI, resulting in improved shunt compensation with OAPFC.

Table 3: *Performance comparison of the VSI and BTB-TVSI.*

Parameters	DSTATCOM	
	VSI	BTB-TVSI
Supply current (THD)	2.1 A (4.5%)	2.19 A (3.6%)
Supply voltage (THD)	203 V (2.1%)	202.5 V (2%)
Load current (THD)	1.67 A (28.9%)	1.6 A (28.9%)
Load voltage (THD)	194.5 V (5.1%)	197.6 V (5%)
Power factor	0.984	0.986
DC link voltage	610 V	650 V
Voltage regulation	Good	Better
Switching stress	High	Low
Filter size	Big	Small
Reliability	Good	Better
Stability	Poor	Better

Experimental results are provided for validation purposes. In this study, the PQ issues are compensated in such a way that the source side currents are always maintained, balanced, and sinusoidal.

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Jogeswara Sabat received the B.Tech. in Electrical and Electronics Engineering from B.P.U.T, India in 2016. He received the M.Tech. in Power System Engineering from P.M.E.C, India in 2018. He was working as a Senior Research Fellow in EEE Dept. of LIET Vizianagaram, India under DST/SERB project. His area of research interest includes Power Quality, Design and modelling of custom power Devices, etc.

Mrutyunjaya Mangaraj received the B.Tech. (Hons.) in Electrical Engineering from Berhampur University, India in 2006. He received the M.Tech. in Power System Engineering from VSSUT, Burla, India in 2010. He served as Assistant professor in the Department of Electrical Engineering at NIST Berhampur, India from 2010 to 2013. He obtained Ph.D. from National Institute of Technology, Rourkela, India in 2018. He rejoined at NIST Berhampur for one and half years and currently continuing as an Associate Professor in the Department of Electrical & Electronics Engineering at LIET Vizianagaram, India. He is associated as Principal Investigator in SERB sponsored project under the SRG grant. His area of research interest includes Power System Economics, Design and modelling of d-FACTS devices with Embedded Controller, Soft computing techniques, etc.