A Simple and Fast Voltage Disturbance Detection and Voltage Reference Generation Approach for Dynamic Voltage Restorer (DVR) to Compensate Unbalanced Voltage Sag and Swell in Three-Phase System: Simulation and Experimental Testing

Taweesak Thongsan and **Theerayuth Chatchanayuenyong**[†], Non-members

ABSTRACT

The dynamic voltage restorer (DVR) is an important device for coping with voltage sag, swell, and unbalance. However, it is a real-time mechanism and must operate as quickly as possible to protect the sensitive and critical load from supply-side voltage anomalies. Hence, fast detection of voltage disturbances and reference voltage generation is essential for the DVR. This paper proposes a simple and fast voltage disturbance detection approach based on a simple three-phase phasor diagram which is easy to implement. The controller employed for the DVR uses a sliding mode control, making the entire system robust and insensitive to system parameter variations. Three different scenarios are simulated according to arbitrarily imposed supply conditions, verified in laboratory tests using the DSP R&D controller board. The results demonstrate a simpler, faster voltage-anomaly detection process which is easier for implementation compared to the other methods in the literature. The best and worst detection times (DTs) of the proposed approach are 1 and 4 ms, respectively. It yields a rapid response, accurate compensation, and robustness in restoring the load voltage to its nominal value within two cycles.

Keywords: Dynamic Voltage Restorer, DVR, Voltage Sag, Voltage Swell, Voltage Unbalance, Sliding Mode Control, SMC

1. INTRODUCTION

Power quality problems related to voltage such as sag, swell, unbalance, harmonics, fluctuations, and interruptions must be avoided when sensitive and critical loads are utilized. These voltage anomalies can lead to serious and costly consequences such as sensitive load tripping, data loss, decreased production, and financial loss. Nowadays, voltage quality also plays an important role in the field of renewable power generation systems due to the sensitivity of power generators to grid voltage imperfections [1]. The output grid voltage fluctuation might occur due to variations in renewable energy sources. According to [2], voltage sag is caused by short circuit faults when switching heavy loads on and starting large motors. Voltage swell is much less common than voltage sag and caused by short circuit faults, switching off large loads, load shedding, and switching on large capacitor banks. Voltage unbalance is the result of unbalanced single-phase loads on three-phase circuits, capacitor bank anomalies, and single-phasing conditions. To cope with these voltage problems, dynamic voltage restorer (DVR) is an effective option.

The DVR is an inherent real-time mechanism that protects the sensitive and critical loads from supply-side voltage anomalies as quickly as possible. The performance of the DVR control system depends heavily on the speed and accuracy of the detection method. Therefore, rapid detection of voltage disturbances and reference voltage generation is crucial for the DVR to perform its functions. The simplest and easiest method for implementing voltage sag/swell is peak value monitoring (PVM) [3], although it may be susceptible to noise and take up to a half cycle to detect the voltage sag. Another simple and traditional method is the root mean square (rms) voltage calculation method, but it yields a low-speed response with the detection time (DT) being up to two cycles. Hence, it is not suitable for DVR application [4, 5].

The dq transformation method is extremely fast and simple to implement; however, it cannot detect a single-phase voltage sag with a depth of less than 30% of the normal value. As a result, it is impractical despite being fast, accurate, and stable [5]. The Fourier transform is another method for detecting sag/swell but, like the rms, it has a slow response.

Alternatively, wavelet transform applications to detect sag/swell have been reported and tested [6–10], but they are quite complicated and very difficult to implement in reality. Kalman filtering (KF) is another method utilized in sag/swell detection [11–14], but it has been reported that the more complicated the model of the

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The authors are with the Faculty of Engineering, Mahasarakham University, Maha Sarakham, Thailand.

[†]Corresponding author: theerayuth.c@msu.ac.th

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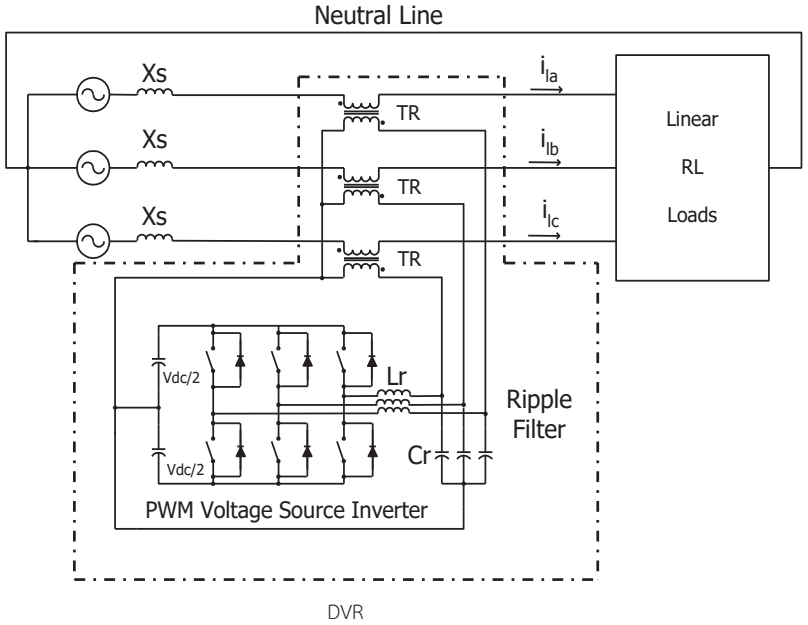

***Fig. 1**: DVR configuration and topology.*

system, the slower the dynamic response of the KF.

Various control strategies have been proposed in the literature, such as PI control [15–17], fuzzy logic control [18–20], neural network control [21, 22], adaptive neuro-fuzzy inference system (ANFIS) control [16], and sliding mode control (SMC) [23, 24]. Among these control strategies, the SMC is a robust control which provides a satisfactory performance with a simple control structure. It possesses two advantageous characteristics. Firstly, SMC is insensitive to model imprecision caused by unmodelled dynamics, variations in system parameters, or the approximation of complex plant behavior by a simplified model. Secondly, SMC allows nth-order problems to be represented by the equivalent 1st-order problems, reducing the complexity of the control algorithm [25, 26].

In this paper, a fast voltage disturbance detection approach for DVR is proposed. The proposed technique is based on a simple phasor diagram of a three-phase system, which is easy to implement. It yields a fast response and when working with the robust SMC, it is insensitive to model imprecisions and system parameter variations [27, 28]. The performance of the proposed approach is first investigated using MATLAB/Simulink and then validated by experimental testing in the laboratory using a dSPACE DS1104 DSP controller board.

The paper is organized as follows. Section 2 presents the configuration and topology of the DVR. The proposed voltage disturbance detection and voltage reference generation method are then introduced in Section 3. In Section 4, the controller utilized for the DVR is illustrated. Finally, the simulation results and the corresponding experimental investigation of the proposed approach are presented in Section 5.

2. MATERIALS AND METHODS

2.1 Configuration and Topology of the Dynamic Voltage Restorer (DVR)

The DVR structure is shown in Fig. 1. It consists of a three-phase voltage source inverter, a DC-link with two capacitors, a low pass LC filter and three single-phase injection transformers. The DC-link capacitor is used for energy storage and charged by another supply source through a passive shunt converter. The output of the inverter is filtered by an LC-ripple filter (L_r, C_r) to attenuate the 4 kHz switching effect of the inverter. This high switching frequency is chosen for ease in filtering harmonics voltage without going into the 6 kHz–20 kHz audible range.

According to the DVR configuration in Fig. 1, the load voltage of each phase can be written as

$$v_L(t) = v_s(t) - Ri(t) - L\frac{d}{dt}i(t) + u(t) \qquad (1)$$

where $v_s(t)$ is the source voltage applied on the point of common coupling, R is the resistance of the series coupling transformer, L is the inductance of the series coupling transformer, $v_L(t)$ is the load voltage and $u(t)$ is the compensating voltage generated by the DVR.

2.2 Control of the DVR

The main control system of the DVR detects the start and end of the voltage disturbance, voltage reference generation, and the controller to control the transient and steady states of the compensating voltage. A block diagram of the DVR control is presented in Fig. 2.

The DVR control requires the measurement of three-phase source voltages before the coupling transformer to detect a voltage disturbance (voltage sag, swell, and

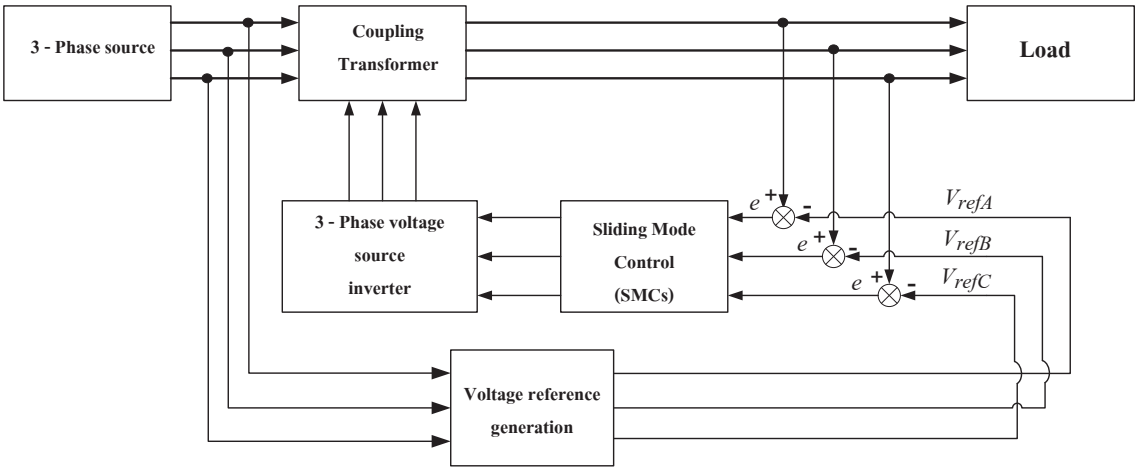

Fig. 2: *Block diagram of the DVR control.*

unbalance), three-phase load voltages after the coupling transformer for feedback control, and the DC-link voltage to provide energy storage information.

2.3 Proposed Voltage Disturbance Detection and Voltage Reference Generation Method

The performance of the control algorithm depends entirely on the quality and accuracy of the detection method [27]. Voltage disturbances must be detected quickly and compensated promptly. Hence, the ease and speed of detection and reference voltage generation for the controller are crucial in such a real-time mechanism.

The concept of the proposed voltage disturbance detection method in the three-phase system is shown in Fig. 3. The method is based on a simple phasor diagram of a three-phase system implemented in the real system.

As shown in Fig. 3, v_{ab}, v_{bc}, v_{ca} and v_a, v_b, v_c represent the line-to-line voltages and phase voltages of the source voltages, respectively. v_{aa} is a voltage in phase with v_a and has the amplitude of V_{aa} as

$$v_{aa}(t) = V_{aa} \sin(\omega t + \phi) \tag{2}$$

where v_{aa} can be obtained from

$$v_{aa}(t) = v_{ab}(t) - v_{ca}(t) \tag{3}$$

In [26], the peak detection method is much quicker than the other rms techniques. Hence, the amplitude or peak voltage, V_{aa} of $v_{aa}(t)$, is selected to calculate the reference voltages and can be found using data in a brief time window. It is based on two samples of $v_{aa}(t)$ as in Eq. (4) [28].

$$V_{aa} = \frac{\left[v_{aa(k+1)}^2 + v_{aa(k)}^2 - 2v_{aa(k+1)}v_{aa(k)}\cos\left(\omega T_s\right)\right]^{0.5}}{\sin\left(\omega T_s\right)} \tag{4}$$

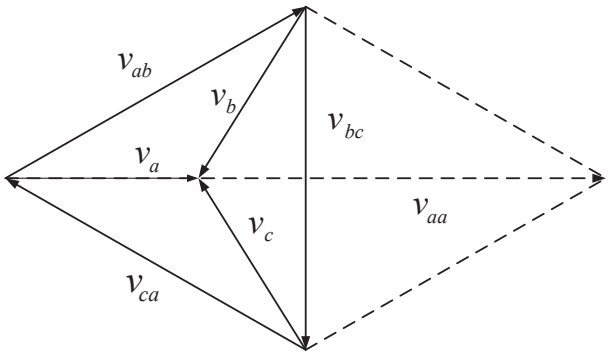

Fig. 3: *Phasor diagram of a balanced three-phase system.*

where $v_{aa(k+1)}$ and $v_{aa(k)}$ represent the v_{aa} signal at instant t_{k+1} and t_k, respectively, and $T_s = t_{k+1} - t_k$ is the sampling period.

The three reference voltages for the controller can be calculated as

$$v_{ref}(t) = \frac{V_{rated}}{V_{aa}} \times v_{aa}(t) \tag{5}$$

$$\begin{bmatrix} v_{refA} \\ v_{refB} \\ v_{refC} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix} \begin{bmatrix} 0 \\ v_{ref} \\ 0 \end{bmatrix} \tag{6}$$

where V_{rated} represents the load-rated voltage and $\alpha = \exp(j2\pi/3)$ represents the 120° phase-shift operator.

From Eqs. (5) and (6), it can be seen that only the phase-A reference voltage is to be calculated while the other phase-B and phase-C reference voltages can be obtained by 120° and 240° phase-shifting of the phase-A reference voltages, respectively. These reference voltages are sent to be compared with the instantaneous load voltages resulting in the voltage disturbance or voltage error being fed to the controller as shown in Fig. 2.

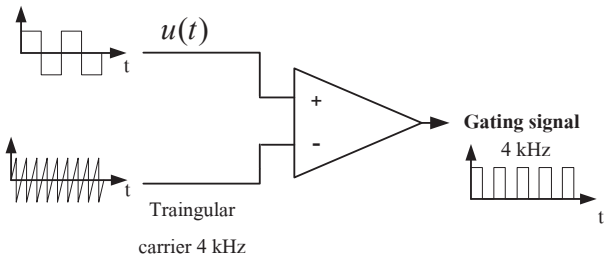

***Fig. 4**: Diagram of gating signal generator.*

***Table 1**: Simulation system parameters for the DVR.*

Parameter	Value
Supply frequency	50 Hz
Load rated phase voltage	110 V_{rms}
R-L linear load	250 Ω, 550 mH
Coupling transformer turn ration	1:1
DC-link voltage	200 V
Inverter switching frequency	4 kHz
Filter inductance	2 mH
Filter capacitance	12 μF

2.4 Controller

As shown in Fig. 2, the controller utilized for the DVR is the sliding mode control (SMC), considered to be a combination of subsystems in which each has a fixed control structure and is effective in particular regions of system behavior [15]. It is a robust control which is inherently insensitive to model imprecisions caused by unmodelled dynamics, variations in system parameters, or the approximation of complex plant behavior by a simplified model. A possible variable structure control law of SMC is given by

$$u(t) = -\rho \,\mathrm{sgn}\,(s(t)) \tag{7}$$

or

$$u(t) = \begin{cases} -\rho & \text{if } s(x,t) > 0 \\ \rho & \text{if } s(x,t) < 0 \end{cases} \tag{8}$$

where ρ is the sliding gain and sgn$(\cdot)$ is the signum or sign function. The switching function $s(x,t)$ is defined by

$$s(x,t) = e \tag{9}$$

where $e = v_{load} - v_{ref}$ is the tracking error in the variable and v_{ref} is desired state.

The sliding gain in this research was selected to be 1.0. In the DVR application, this value allows the SMC yields to control input for comparison with the triangular carrier and generate the gating signal for the inverter.

The reference voltages to be injected by the DVR are calculated by subtracting the reference source voltages obtained from Eq. (6) with the actual load voltages, with the errors fed directly to the SMC. The outputs of the SMC are employed to switch the three-phase inverter.

The gating signals of the inverter are generated by comparing the control input in Eq. (7) with a triangular carrier of 4 kHz as shown in Fig. 4 to establish the compensating voltages corresponding to the reference voltages, filtered by the low pass filter before being injected into the coupling transformers.

3. RESULTS AND DISCUSSION

In order to quantify the degree of unbalance in the three-phase voltages, the unbalance factor (UF) is defined, according to the IEC, as the ratio between negative sequence voltage V_2 and the positive sequence voltage V_1.

$$\mathrm{UF} = \frac{V_2}{V_1} \tag{10}$$

Similarly, the difference between the load voltage and the required rated voltage can be quantified using a magnitude factor (MF). The MF is the ratio between the positive sequence voltage and a rated voltage of load V_{rated}.

$$\mathrm{MF} = \frac{V_1}{V_{rated}} \tag{11}$$

The proposed DVR is firstly verified by simulation and then realized by testing.

3.1 Simulation Results and Discussion

The simulation results are divided into three categories according to the arbitrary imposed supply conditions, as shown in Figs. 5–10. The simulation system parameters for the DVR are listed in Table 1.

Case 1: Balanced voltage sag with |MF| = 0.8273, |UF| = 0, $V_a = V_b = V_c = 91\,V_{rms}$ or $129\,V_{peak}$

In this case, a balanced voltage sag of the supply voltage starts at time $t = 0.15$ s. The voltage sag is 82.73% with respect to the rated voltage. As can be observed from Fig. 5, the DVR rapidly detects the sag and injects the necessary compensating voltage to restore the three-phase load voltages to their rated value. The |MF| after compensation is 1.0. Fig. 5 shows the supply sag voltage, the compensated load voltage, and the necessary compensating voltages.

Fig. 6 depicts the rms values of supply, compensating, load, and reference voltages in phase-A of this case. The voltage sag detection time (DT) is measured and shown in the figure.

From the result in Fig. 6, it was found that the sag voltage occurred at 0.15 s and was detected within 0.003 s (3 ms) and then the DVR started generating the compensating voltage. The DT in this case is 3 ms (0.15 cycle).

Case 2: Balanced voltage swell with |MF| = 1.155, |UF| = 0, $V_a = V_b = V_c = 127\,V_{rms}$ or $180\,V_{peak}$

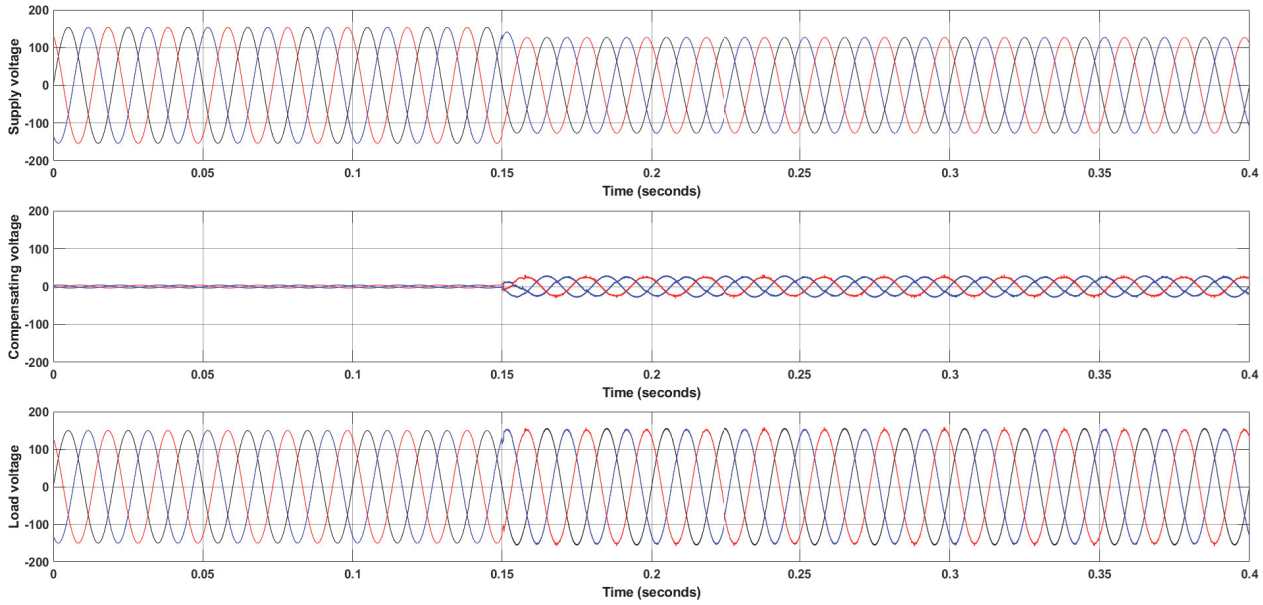

Fig. 5: Supply (top), compensating (middle), and load (bottom) voltage (phase to neutral) in the case of a balanced voltage sag with $|MF| = 0.8273$.

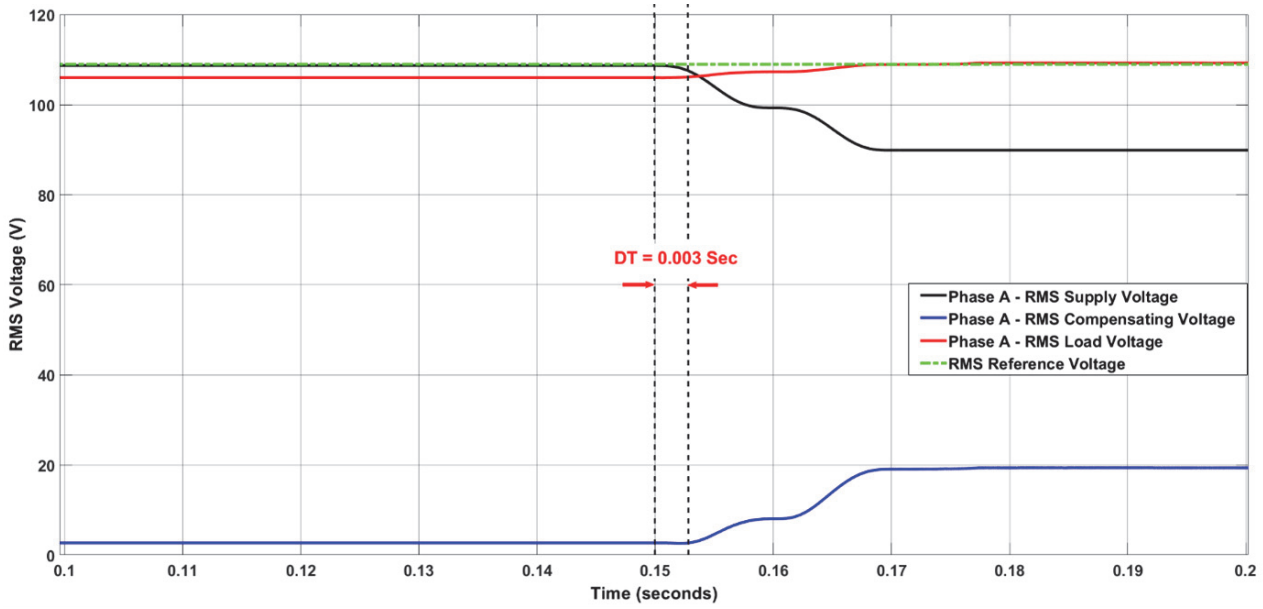

Fig. 6: Rms values of phase-A supply, compensating, load, and reference voltage (phase to neutral) in the case of a balanced voltage sag with $|MF| = 0.8273$.

In this case, a balanced voltage swell starts at the time $t = 0.15$ s. The supply swell voltage is 115.5% with respect to the rated voltage. Fig. 7 depicts the supply swell voltage, the compensated load voltage, and the necessary compensating voltages. It can be found from the figure that the DVR is able to inject the corresponding compensating voltages and maintain the load voltages at their rated value. The |MF| after compensation is 1.0.

Fig. 8 shows rms values of supply, compensating, load, and reference voltages in phase-A of this case. The voltage swell detection time (DT) is measured and included in the figure.

According to Fig. 8, the swell voltage occurred and was detected at 0.15 s and 0.18 s, respectively. The DT in this case is 3 ms (0.15 cycle).

Case 3: Unbalanced voltage sag with |MF| = 0.892, |UF| = 0.551, $V_a = 95\,V_{rms}$, V_b = nominal voltage, and $V_c = 89\,V_{rms}$

In this case, an unbalanced voltage sag starts at time $t = 0.15$ s. The voltages in phase-A and phase-B decrease to 86.4% and 80.9%, respectively, according

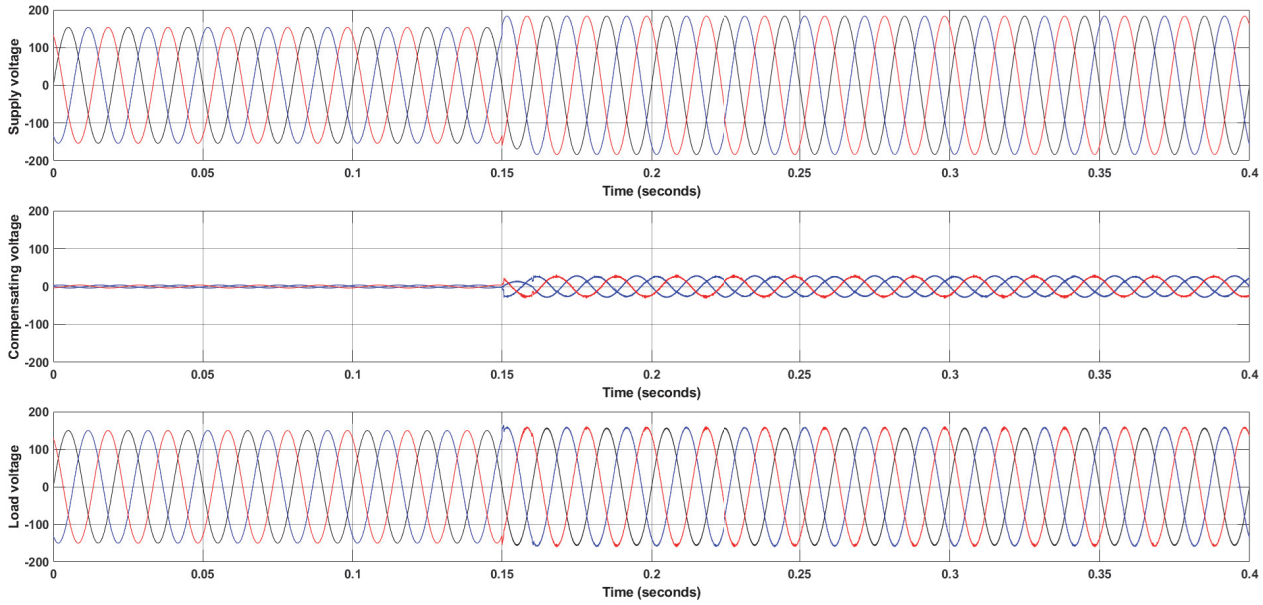

Fig. 7: Supply (top), compensating (middle), and load (bottom) voltage (phase to neutral) in the case of a balanced voltage swell with $|MF| = 1.155$.

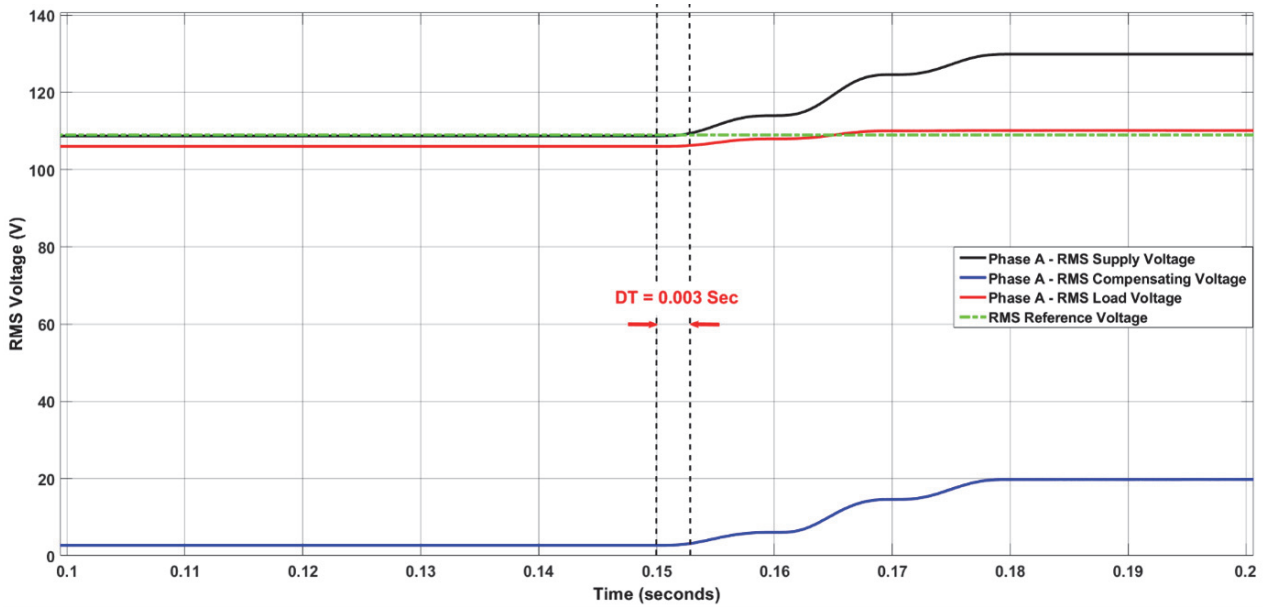

Fig. 8: Rms values of phase-A supply, compensating, load, and reference voltage (phase to neutral) in the case of a balanced voltage swell with $|MF| = 1.155$.

to the rated voltages. Fig. 9 shows the supply swell voltage, the compensated load voltage, and the necessary compensating voltages. It can be seen from Fig. 9 that the DVR detects the sag voltages in each phase and rapidly injects the compensating voltages to keep the load voltages in balance. The |MF| and |UF| after compensation are 1.0 and 0.0, respectively.

Figs. 10(a) and 10(b) illustrate the rms values of supply, compensating, load, and reference voltages in phase-A and phase-C of this case, respectively. The voltage sag DTs are also shown in the figures.

According to the results in Fig. 10, the unbalanced voltage swell occurred at 0.15 s and was detected at 0.18 s in phase-A, and 0.16 s in phase-C. The DT in this case is 3 ms (0.15 cycle) in phase-A and 1 ms (0.05 cycle) in phase-C.

Table 2 illustrates the performance comparison among various detection methods. According to the Table, PVM and RMS calculation methods are simple but yield long detection times. The DQT method gives a quick detection time in the case of pure sinusoidal voltage. However, the grid voltage is harmonically distorted in practice, the

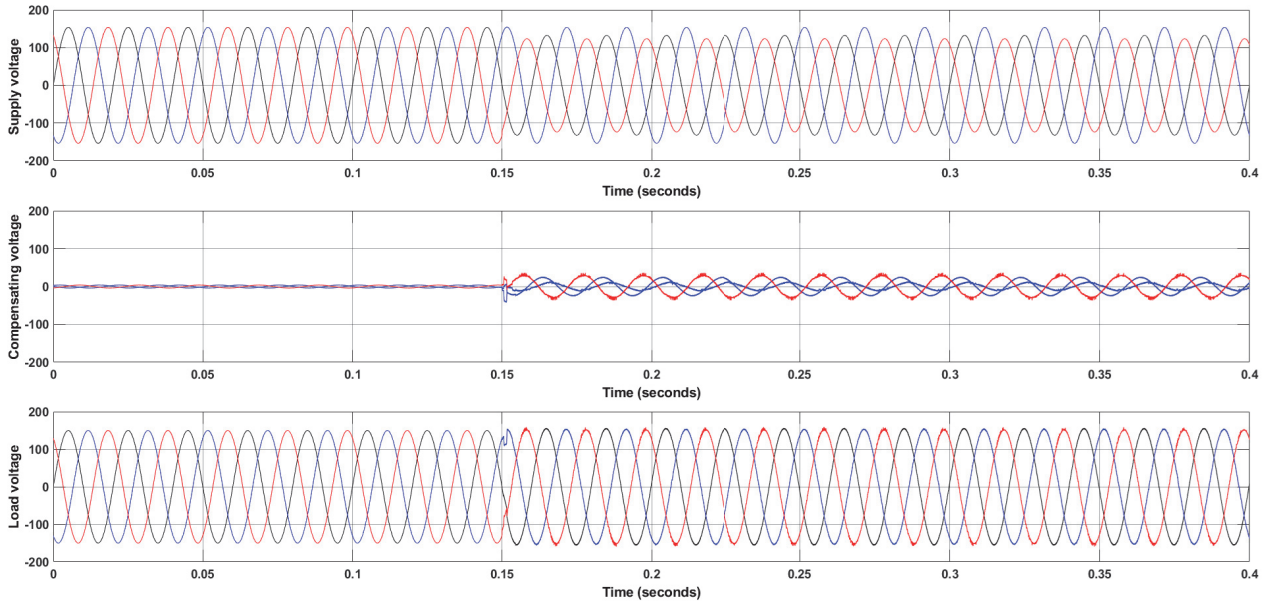

Fig. 9: *Supply (top), compensating (middle), and load (bottom) voltage (phase to neutral) in the case of a balanced voltage swell with $|MF| = 0.85$ and $|UF| = 0.14$.*

Table 2: *Comparison of detection methods.*

Detection Method	Detection Time (DT)	Remark
Peak value monitoring (PVM) [3]	Half cycle (10 ms)	–
RMS calculation [4, 5]	Two cycles (33.3–40 ms)	– –
dq transformation (DQT) [5]	Less than 1 ms in the case of pure sinusoidal	Harmonically distorted voltage increases the DT significantly
Single-phase rotating frame [5]	1–8.8 ms	Complicate/computational burden process
Proposed method	1–4 ms	Simple and fast

Table 3: *Parameters used in the experimental test.*

Parameter	Value
Supply frequency	50 Hz
Load rated phase voltage	110 V_{rms}
R-L linear load	250 Ω, 550 mH
Coupling transformer turn ration	1:1
DC-link voltage	200 V
Inverter switching frequency	4 kHz
Filter inductance	2 mH
Filter capacitance	12 μF

low pass filter must be added, and the DT significantly increases [5]. The single-phase rotating frame method has a good detection time but at the cost of a complicated and computationally burdensome process. The proposed method could detect voltage anomalies with the best and worst DT within 1 and 4 ms, respectively. It yields a fast DT and the process is simple.

The results from the simulation study illustrate the feasibility of the proposed method. In addition to the simple and fast DT process, they clearly show the capability of the proposed method to restore the drop, boost, and unbalance in the supply voltage within 4 ms. The |MF| at 0.8273 in case 1, 1.155 in case 2 and 0.892 with |UF| at 0.0551 in case 3 are restored to their nominal value |MF| at 1.0 and |UF| at 0.0. The fast response and accurate performance to correct and regulate the anomaly supply voltage are obvious. The DVR is functioning when the voltage anomalies occur and efficiently compensates to yield sag-free, swell-free, and balanced load voltages.

3.2 Experimental Verifications and Discussion

An experimental set-up was established in the laboratory to realize the proposed algorithm of the DVR system. The experimental parameters are shown in Table 3.

The supply voltage at 110 V_{rms}, corresponding to the simulation is used for the laboratory test. The hardware prototype schematic diagram of the DVR is depicted in Fig. 11 and its photograph shown in Fig. 12.

An adjustable 3-phase AC source supplies the R-L load through the rheostats to establish the unbalance, sag, and swell voltage sources. The proposed algorithm was implemented in a PC with a DSP R&D controller board [29] to generate the PWM switching signal for the voltage source inverter (VSI). The VSI comprises six insulated gate bipolar transistor (IGBT) switches and connected to the coupling transformer's primary windings. A filter inductor and capacitor set was employed to mitigate the switching harmonics. The DC-

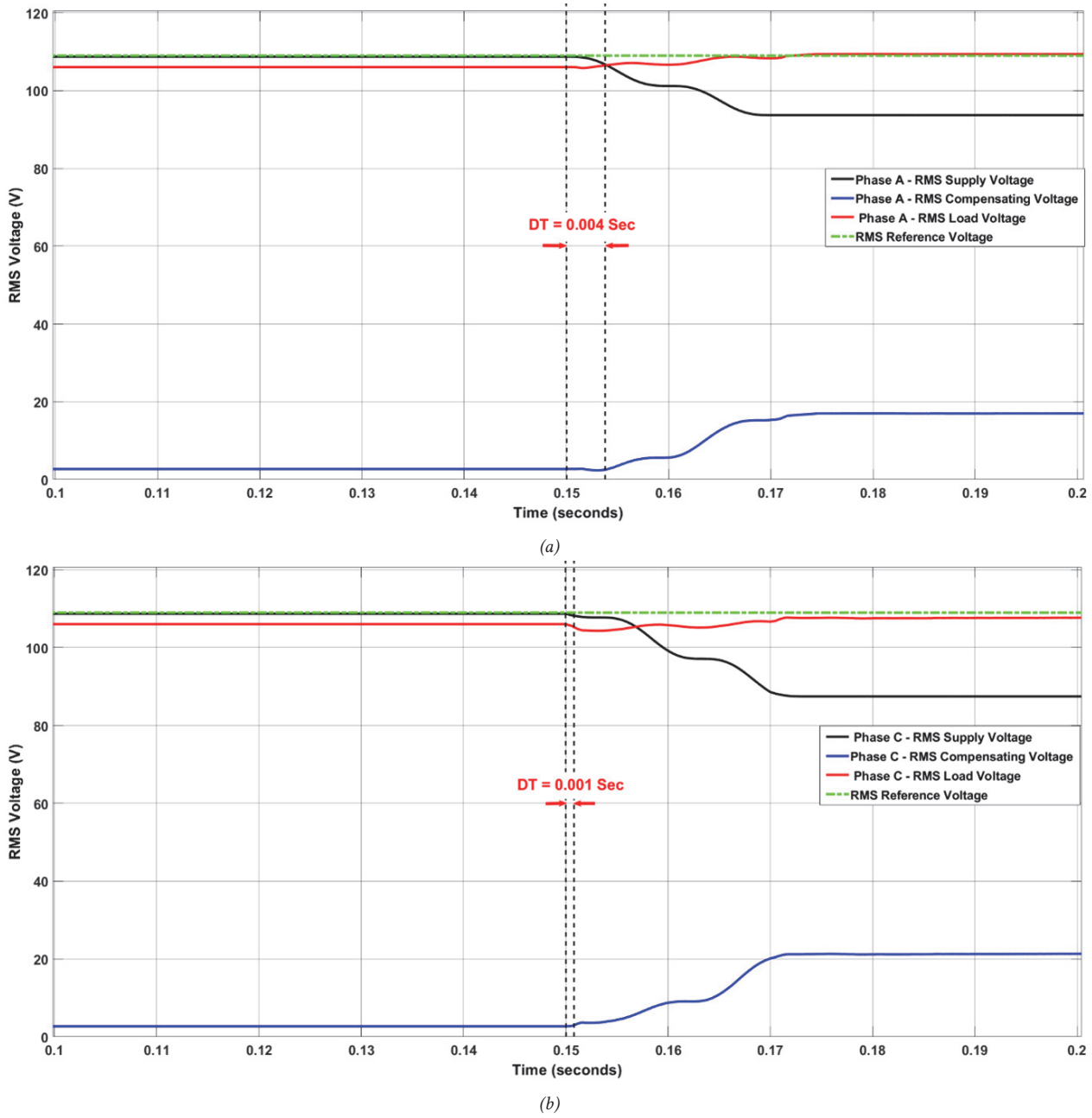

***Fig. 10**: Rms values of supply, compensating, load, and reference voltage (phase to neutral) in the case of unbalanced voltage sag with $|MF| = 0.892$, $|UF| = 0.0551$, $V_a = 95\,V_{rms}$, V_b = nominal voltage, and $V_c = 89\,V_{rms}$; (a) phase-A and (b) phase-B.*

link of the VSI was supplied by an independent source. The source, load, and capacitor DC-link voltages were measured by transducers in the isolation amplifiers and sent to the DSP card for real-time control. The same three imposed supply conditions as those applied in the simulation were tested and their results are shown in Figs. 13–23.

Case 1: Balanced voltage sag with |MF| = 0.8273, |UF| = 0, $V_a = V_b = V_c = 91\,V_{rms}$ or $129\,V_{peak}$

In this case, a balanced sag of the supply voltage starts at time interval $t = 0.07$ s to 0.27 s. The three-phase voltages decreased to 82.73% with respect to the rated voltage. Fig. 13 depicts the supply sag voltage, the restored load voltage, and the capacitor DC-link voltage, which is maintained constant with a passive rectifier supplied from an independent energy source as shown in Fig. 13(c). The DVR injects the necessary compensating voltages and enhances the load voltage to its rated value.

Fig. 14 shows an example comparison between the rms value of phase-A load voltage and the reference voltage. It can be observed from the figure that at the time the voltage sag occurs, the rms load voltage decreases from the reference voltage for 34 ms (1.7 cycles). When the

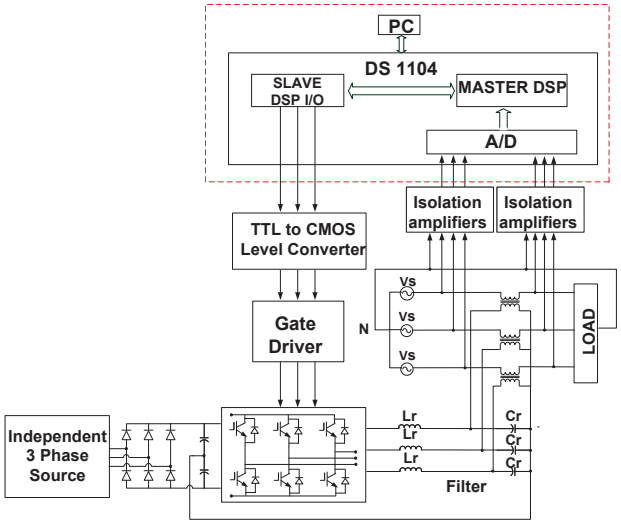

Fig. 11: Hardware prototype schematic diagram of the DVR.

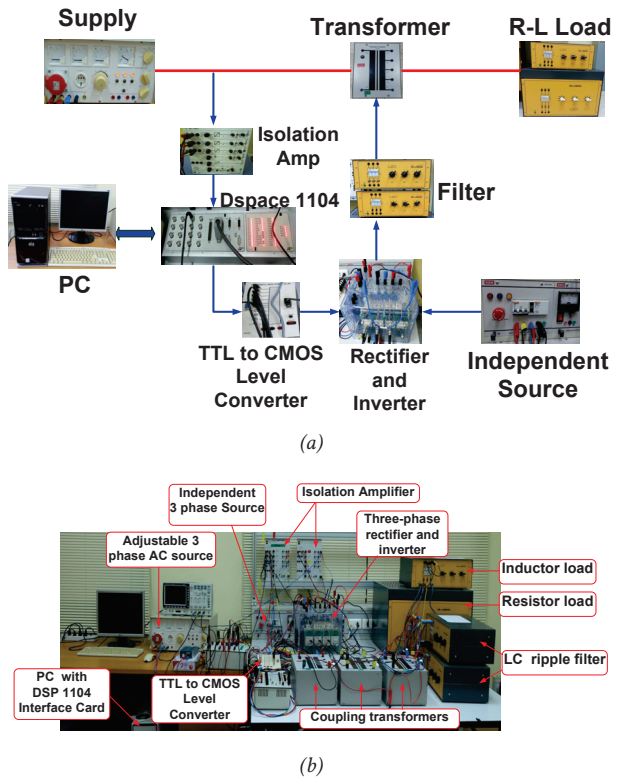

Fig. 12: Photograph of the hardware prototype; (a) connection and (b) laboratory test rig.

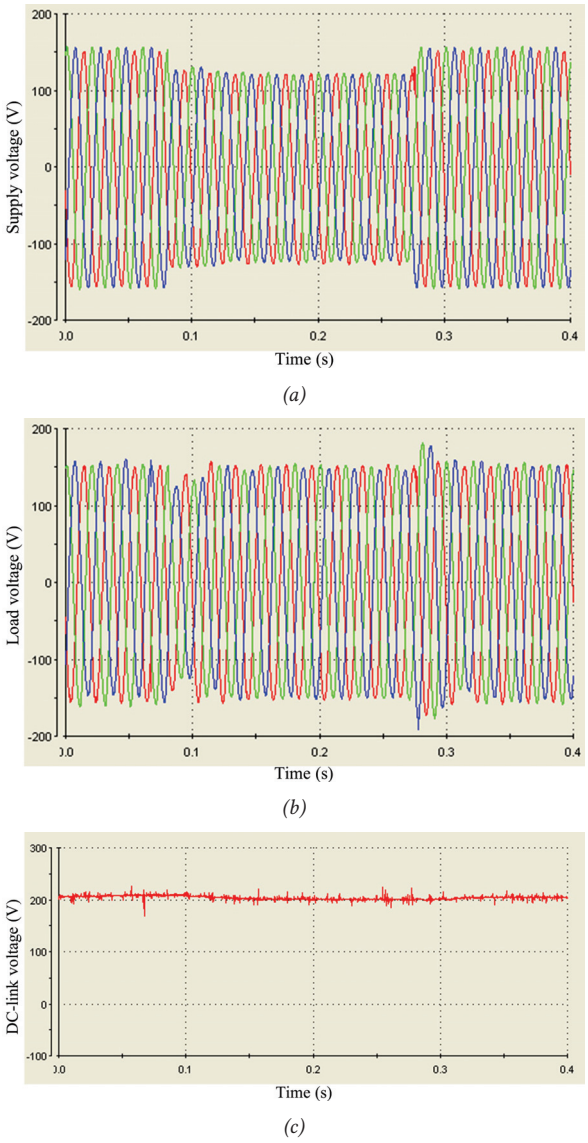

Fig. 13: (a) Supply, (b) load, and (c) capacitor DC-link voltage of case 1.

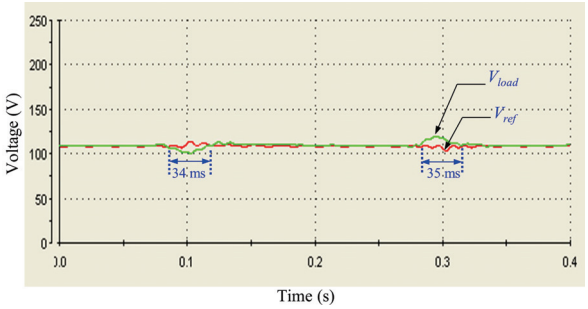

Fig. 14: Comparison between the rms value of phase-A load voltage and the reference voltage of case 1.

voltage sag occurs, the DVR is switched on and efficiently generates the compensating voltage to restore the load voltage to its rated value within 34 ms. At time $t = 0.27$ s when the supply voltage sag disappears, the DVR detects the sag-free supply voltage and is switched off. The load voltage overshoots from the reference voltage for 35 ms (1.75 cycles), which is the dynamic response time of the DVR.

It can also be observed from Fig. 15 that during the time of the voltage sag, the load voltage and reference voltage of phases A, B, and C are different in magnitude and when the sag has been compensated, the two voltages are almost similar.

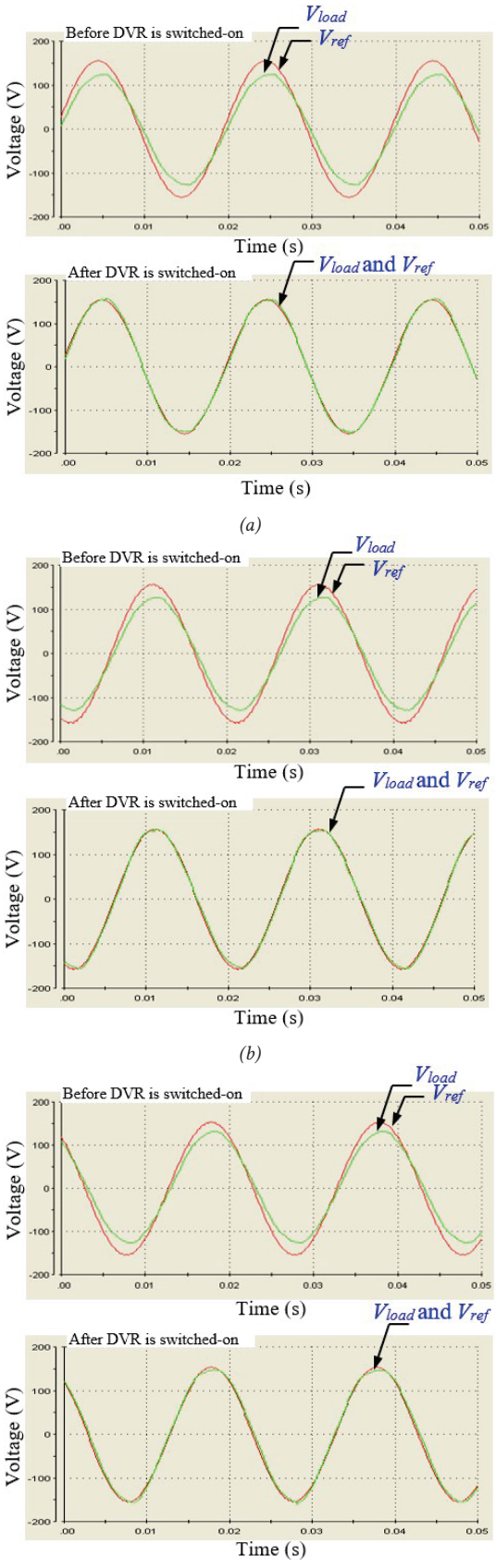

Fig. 15: Comparison of (a) phase-A, (b) phase-B, and (c) phase-C load voltage, and reference voltage before and after the DVR is switched on (case 1).

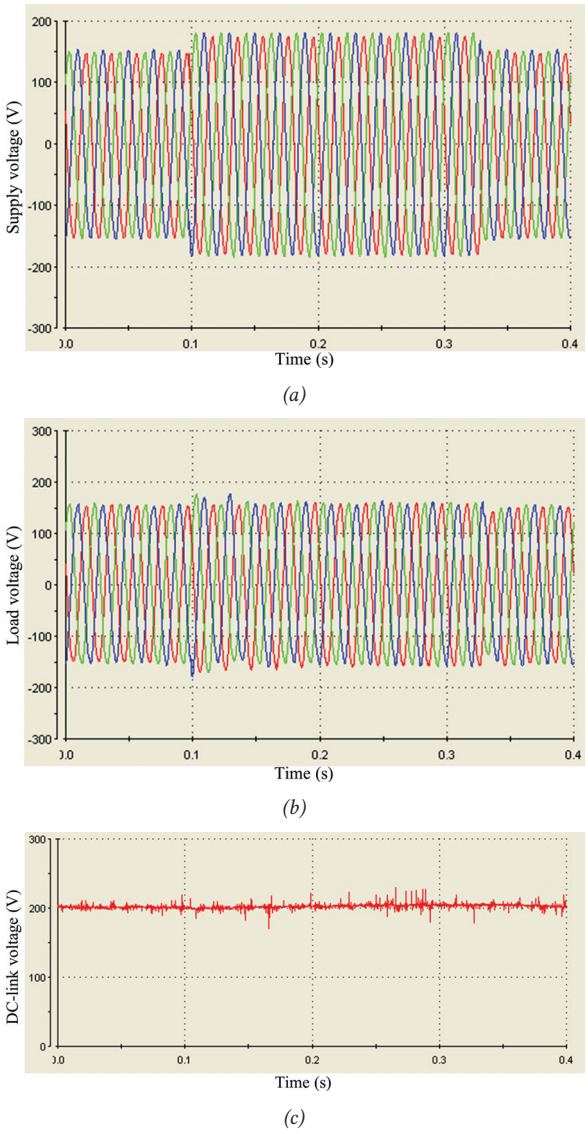

Fig. 16: (a) Supply, (b) load, and (c) capacitor DC-link voltage of case 2.

Case 2: Balanced voltage swell with |MF| = 1.155, |UF| = 0, $V_a = V_b = V_c = 127\,V_{rms}$ or $180\,V_{peak}$

In this case, a balanced swell of the supply voltage started at time interval $t = 0.1$ s to 0.33 s. The three-phase voltage increased to 115.5% with respect to the rated voltage. Fig. 16 shows the supply swell voltage, the restored load voltage, and the capacitor DC-link voltage which is maintained constant with a passive rectifier supplied from an independent energy source as shown in Fig. 16(c). The DVR injected the necessary compensating voltages and reduced the load voltage to its rated value.

Fig. 17 illustrates an example of a comparison between the rms value of phase-A load voltage and reference voltage, and it can be observed from the figure that at the time when the voltage swell occurs, the rms load voltage increased from the reference voltage for 39 ms (1.95 cycles). When the voltage swell occurred, the DVR switched on and efficiently generated the compensating

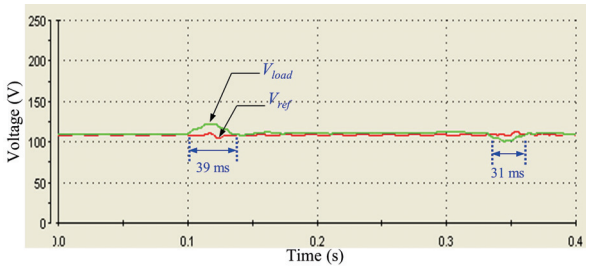

Fig. 17: Comparison between the rms value of phase-A load voltage and the reference voltage of case 2.

voltage to reduce the load voltage to its rated value within 39 ms. At $t = 0.33$ s, when the supply voltage swell disappeared, the DVR detected the swell-free supply voltage and switched off. The load voltage dropped from the reference voltage for 31 ms (1.55 cycles) which was the dynamic response time of the DVR.

It can also be observed from Fig. 18 that before the DVR was switched on, the load and reference voltages of phase-A, B, and C were different in magnitude and phase but after the DVR switched on and the swell was already compensated, the two voltages nearly coincide.

Case 3: Unbalanced voltage sag with |MF| = 0.892, |UF| = 0.551, $V_a = 95\,V_{rms}$, V_b = nominal voltage, and $V_c = 89\,V_{rms}$

In this case, an unbalanced voltage swell occurs from 0.03 s to 0.33 s in phases A and C of the supply voltage, decreasing to 86.36% and 80.9%, respectively, according to the rated voltage. Fig. 19 depicts the supply unbalanced voltage, the balanced load voltage, and the capacitor DC-link voltage which is maintained constant with a passive rectifier supplied from an independent energy source as shown in Fig. 19(c). It can be observed from the figure that the DVR rapidly detects the voltage sag in phases A and C and injects the necessary compensating voltage both in magnitude and phase to keep the load voltage in balance.

Fig. 20 shows a comparison between the rms value of phase-A, phase-B, and phase-C load voltage and reference voltage, from which it can be observed that the dynamic response time to clear the voltage sag in phases A and C are 33 ms (1.65 cycles) and 40 ms (two cycles), respectively.

At time $t = 0.33$ s when the supply voltage is balanced, the DVR is switched off and the load voltages overshoots the reference voltage due to the dynamic response of the DVR for 33 ms (1.65 cycles) and 32 ms (1.6 cycles) in phases A and C, respectively.

Fig. 21 shows a comparison between the phase-A, phase-B, and phase-C load voltages and reference voltages before and after the DVR is switched on. It can be observed that before the DVR is switched on, the load voltage and reference voltage in phases A and C are different in magnitude and phase. However, after the DVR is switched on and the load voltage keeps in balance,

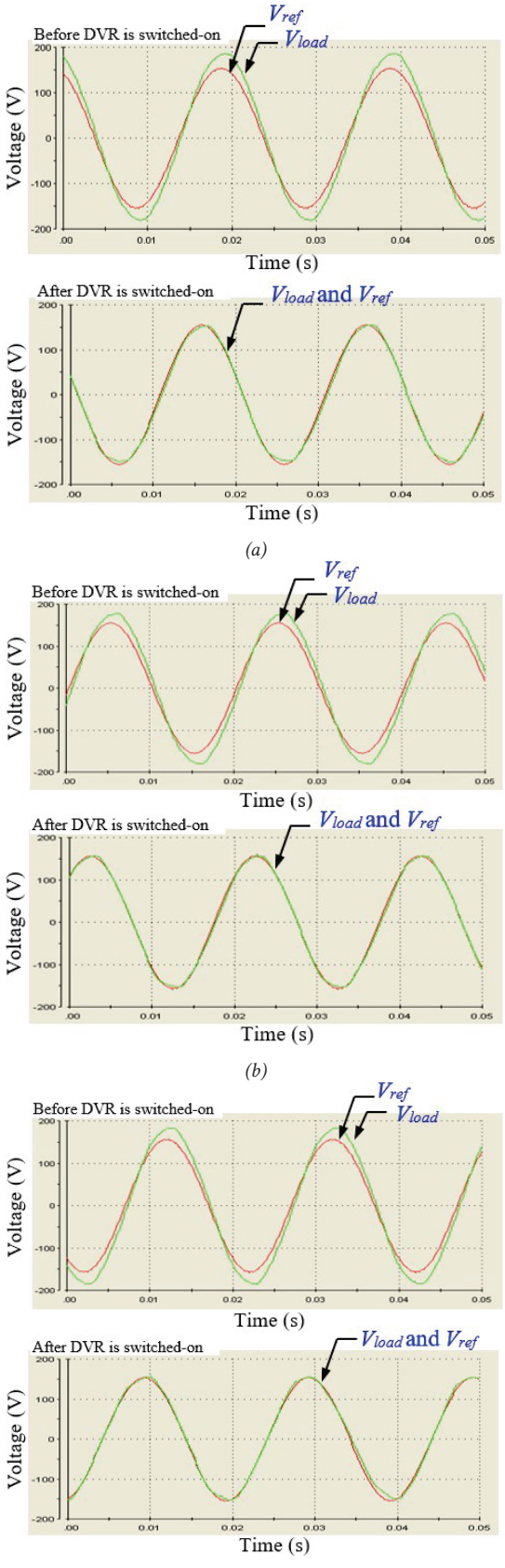

Fig. 18: Comparison of (a) phase-A, (b) phase-B, and (c) phase-C load voltage and reference voltage before and after the DVR is switched on (case 2).

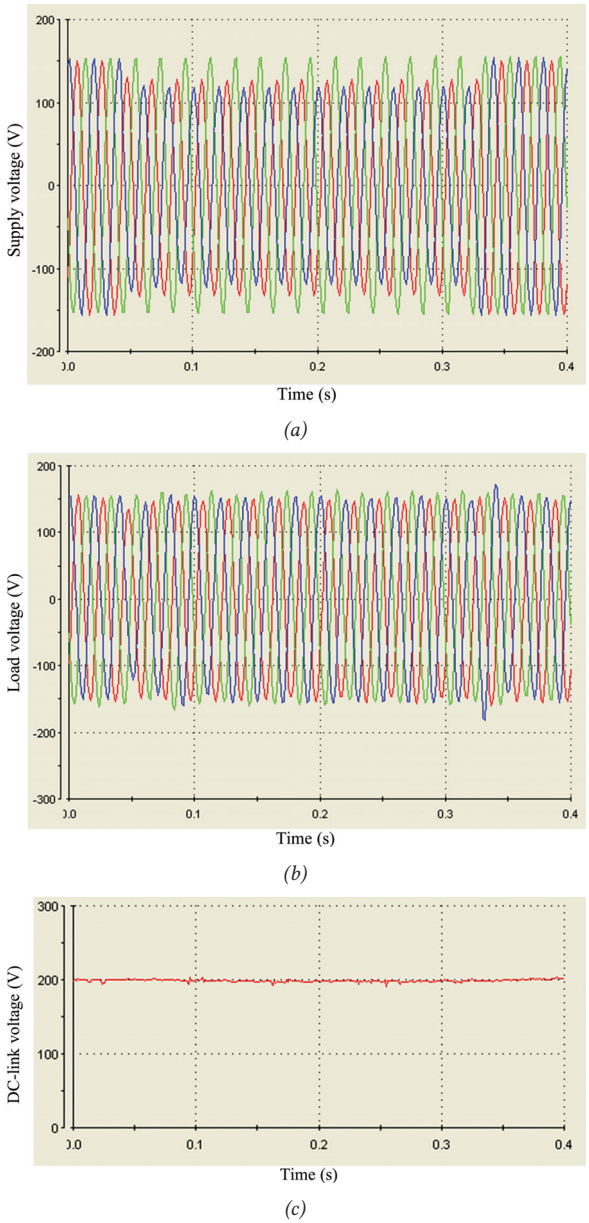

Fig. 19: *(a) Supply, (b) load, and (c) capacitor DC-link voltage of case 3.*

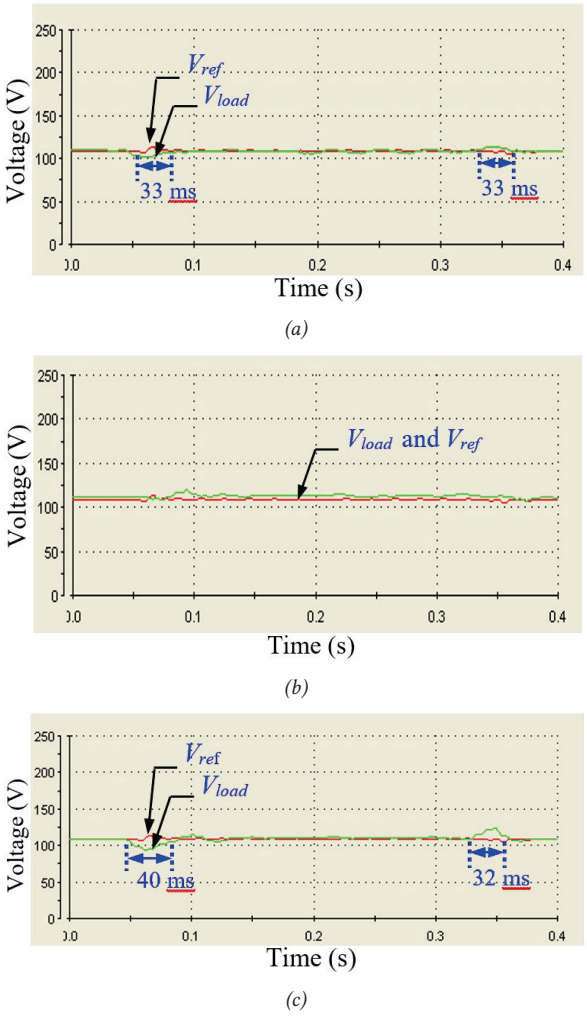

Fig. 20: *Comparison between the rms values of (a) phase-A, (b) phase-B, and (c) phase-C load voltages and the reference voltages of case 3.*

Table 4: *Dynamic response of the three voltage disturbance cases from the experimental test compared to the ITIC standard [30].*

Case	Description	Response Time (ms) (1)	Response Time (ms) (2)	ITIC (ms)
1	Balanced voltage sag (82.7%)	34	35	<500
2	Balanced voltage swell (115.5%)	39	31	<700
3	Unbalanced voltage sag (86.4% phase-A, 0% phase-B, and 80.9% phase-C)	33 (phase-A) 40 (phase-C)	33 (phase-A) 32 (phase-C)	<500

Note: (1) Response time from the start of voltage anomalies until being restored to their nominal value.
(2) Response time from the end of voltage anomalies until they recover to their nominal value.

the two voltages nearly coincide.

From the above three experimental cases, the DVR is switched on at the moment the voltage anomalies occur and efficiently generates the compensating voltage to yield the normal load voltage. The voltage anomalies can be restored to their nominal value at 110 V_{rms} within two cycles (< 40 ms). These results confirm the efficient performance of the DVR, resulting from the proposed voltage disturbance detection approach and the robustness of the sliding mode control system.

Table 4 presents a comparison of time responses during different voltage disturbances with the ITIC standards. The dynamic response times of all cases fall into the safety power quality area according to the ITIC.

An example of phase-A supply voltage, load voltage, and the compensating voltage plotted in the same graph in the case of voltage sag and voltage swell are shown in

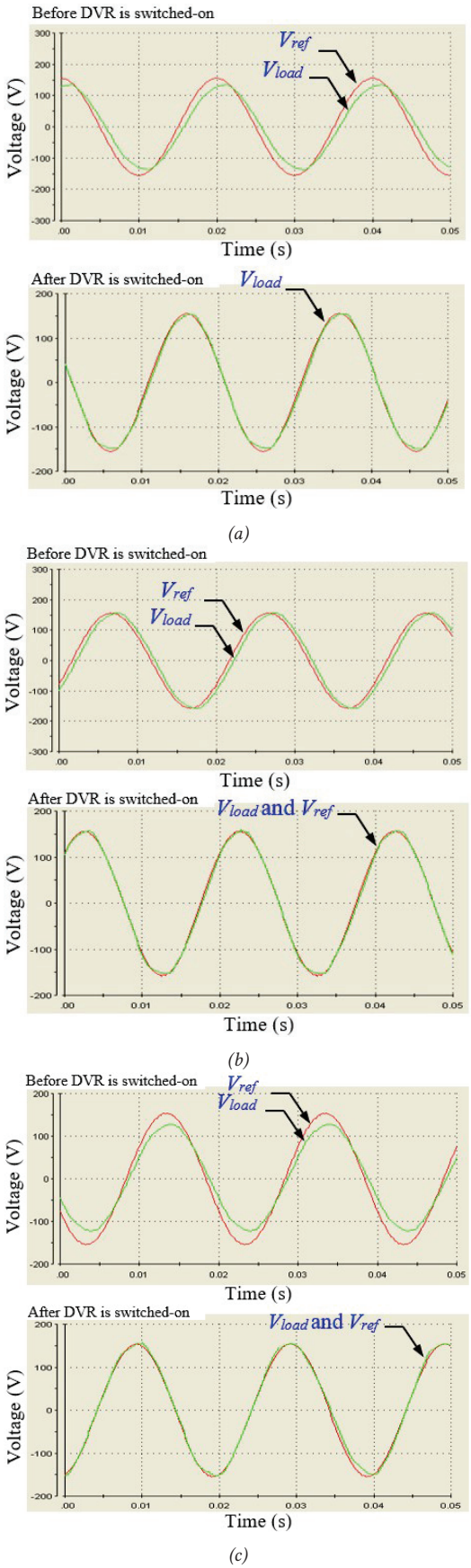

Fig. 21: *Comparison of (a) phase-A, (b) phase-B, and (c) phase-C load voltage and reference voltage before and after the DVR is switched on (case 3).*

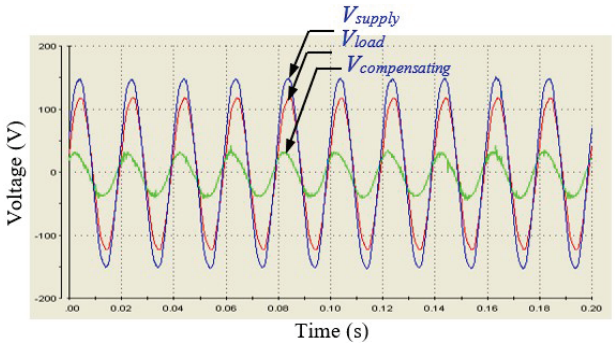

Fig. 22: *Phase-A supply voltage, load voltage, and compensating voltage in case of voltage sag.*

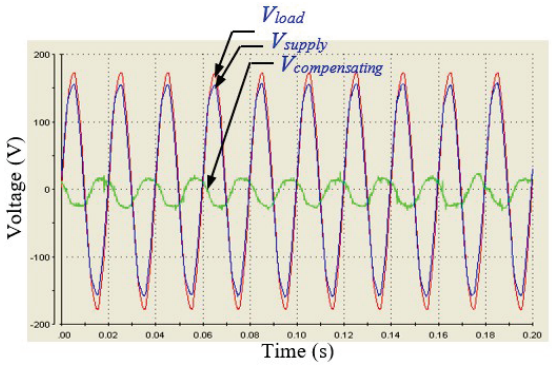

Fig. 23: *Phase-A supply voltage, load voltage, and compensating voltage in case of voltage swell.*

Figs. 22 and 23, respectively. These two figures depict the corresponding compensating voltages required to correct them to their nominal value according to the voltage sag and swell of the load voltage. The controller is able to generate the correct compensating voltages both in magnitude and phase although a phase shift occurs between the supply and load voltages as shown in the figures.

4. CONCLUSION

This paper presents a fast and simple approach for detecting voltage sag, voltage swell, and voltage unbalance and generating the reference voltage for the DVR. The proposed method is based on a simple three-phase phasor diagram and can be easily implemented. The SMC was employed, making the whole system robust and insensitive to variations in the system parameters. The proposed approach was simulated in three different cases according to arbitrarily imposed supply conditions to assess its potential application. The results were then verified by laboratory experiments using the DSP card in the same way as in the simulation. The experimental verification with respect to the simulation results demonstrates the fast response, accurate compensation, and robustness of the proposed approach in restoring the load voltage to its nominal values.

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Taweesak Thongsan received his bachelor degree in Electrical and Computer Engineering from Kasetsart University, Thailand in 2008. He received his master degree and Ph.D. in Electrical and Computer Engineering from Mahasarakham University, Thailand in 2015 and 2022, respectively. His research interests include dynamic voltage restorer, control systems engineering and optimization techniques.

Theerayuth Chatchanayuenyong received his bachelor degree (Honors) in Electrical Engineering from Prince of Songkhla University, Thailand in 1989. He received his master degree in Electrical Engineering from Khon Kaen University, Thailand in 2001 and his D.Eng. in Mechatronics Engineering from Asian Institute of Technology (AIT), Thailand, in 2006. He is currently an Assistant Professor at the Faculty of Engineering and an Acting Director of the Academic Service, Mahasarakham University, Thailand. His research interests include series active filter, dynamic voltage restorer, robust and intelligent control and autonomous underwater robot.