Experimental Validation of a Phase Lead-Lag Synchronous Frame Phase-Locked Loop Under Different Voltage Conditions

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ABSTRACT

Due to the rapid increase in single-phase inverters tied to the grid, fast and robust phase-locked loop algorithms have become indispensable. In previous work, a phase lead-lag synchronous reference frame phase-locked loop (PLL) was proposed. The method makes use of two single-tuned filters that perform as a phase detector. They are capable of shifting the phase of the grid voltage to be advanced or delayed by 45° with respect to the grid voltage phase. The generated orthogonal signals are transformed by Park transformation. The quadrature voltage is regulated to zero by means of a PI controller, while its output determines the frequency of the grid voltage and the phase angle obtained by integrating the estimated frequency. In this paper, deficiencies in the previous work are addressed. A small signal model of the method which takes into account frequency variation, voltage variation, and harmonic distortion is derived and presented. The design guidelines are discussed and an example illustrated. The method is validated through simulations and experiments under various voltage conditions while the algorithm is implemented on a rapid prototyping MicroLabBox. It is tested under different voltage scenarios, generated by a programmable AC source. The experimental results show that the method can track the phase angle of the grid voltage with nearly zero phase error under normal voltage conditions. It can track the phase of the grid voltage under 45° step phase jumps in 2.75 cycles, achieve harmonic attenuation of -15 dB under 15% third harmonic distortion, and attain an adequate phase margin near 45°. This confirms that the method is fast and robust under adverse voltage conditions.

Keywords: Phase lead-lag, Synchronous reference frame, Single-phase, Phase-locked loop

1. INTRODUCTION

Electrical power systems have recently been migrating from radial power toward the paradigm of distributed generations (DGs). It allows alternative energy sources, such as wind turbines, water turbines, and solar cells to be integrated into the grid. The integration of DGs into the utility grid requires power inverters to control the real power and reactive power fed into the grid, as well as regulating harmonic currents in compliance with the utility grid's requirements. Fig. 1 shows a control scheme for single-phase grid-tied inverters. The synchronization unit is one of the most important power inverter control parts since it detects the magnitude, frequency, and phase angle of the grid voltage. Accurate, fast, and robust phase detection is essential when the penetration level of grid-tied power inverters is high [1].

The main contribution of the paper is to address the limitations of the previous work [1]. A small signal model which considers frequency variation, harmonic distortion, and voltage variation, is derived and simplified to a first-order linear time-invariant system. The design guidelines for meeting the requirements of single-tuned filters and a PI controller are discussed. The findings of the study reveal that single-tuned filters and a PI controller cannot be designed separately since they are dependent on each other. To simplify the design process, a load quality factor is selected as a design parameter for single-tuned filters. It must be properly selected since it simultaneously compromises the dynamic response and harmonic attenuation. The symmetrical optimum method is employed in this study to determine the gains of the PI controller, revealing an optimal damping factor of 0.7 and yielding a phase margin of 45°. The design

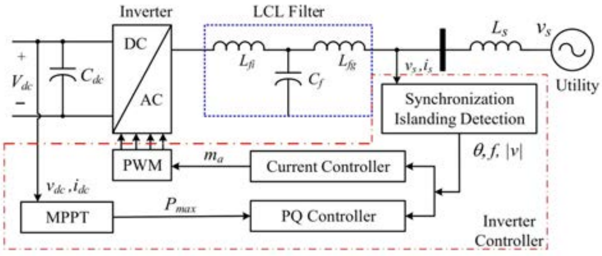

***Fig. 1**: Control structure of a single-phase grid-connected inverter.*

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example is presented here. The algorithm is implemented on a rapid prototyping MicroLabBox and tested under different voltage conditions. The simulation results and experimental results confirm that the method is practical, fast, and robust under adverse power quality events.

The paper is organized as follows. The background of the phase lead-lag synchronous reference frame PLL is summarized in section 2. The small signal model is derived and discussed in section 3, while the design guidelines and examples are presented in section 4. In section 5, the viability and effectiveness of the proposed method are validated through simulations and experiments. Section 6 presents the conclusion.

2. BACKGROUND OF A PHASE LEAD-LAG SYNCHRONOUS REFERENCE FRAME PLL

The phase lead-lag synchronous reference frame was first proposed in [1]. The functional block diagram is shown in Fig. 2. The algorithm has two single-tuned filters which perform as a phase detector. Orthogonal two-phase voltages are realized by a 45° phase-lead tuned filter and a 45° phase-lag tuned filter. The frequency variation compensation is introduced to correct the amplitude and phase of the outputs from two single-tuned filters when the frequency varies from the nominal level. The compensated orthogonal voltages are transformed by Park transformation. The quadrature voltage is regulated to zero by a PI controller whose output yields the estimated frequency. An integrator is employed as a voltage control oscillator to estimate the phase angle of the grid voltage. The acquired phase advances the phase of the grid by +45°. Thus, the 45° phase must be subtracted from the integrator's output so that the estimated phase angle is in phase with that of the grid voltage.

The utilization of +45° and −45° tuned filters emanates from the desirable characteristics of a series RLC circuit, as shown in Fig. 3. It is capable of low pass filtering, DC blocking, and performing as an integrator. It is suitable for performing as a phase detector to create two orthogonal signals and robust against poor power quality grid voltage. The relationship between the input voltage and the current through the RLC series circuit can be expressed by a transfer function in the frequency domain as,

$$T(s) = k_L \frac{s}{s^2 + \frac{\omega}{Q}s + \omega_n^2}$$

$$k_L = \frac{1}{L},\ \omega_n = \frac{1}{\sqrt{LC}},\ \zeta = \frac{1}{2Q},\ Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{1}$$

where ω_n, ζ, and Q are the natural frequency, damping ratio, and load quality factor respectively.

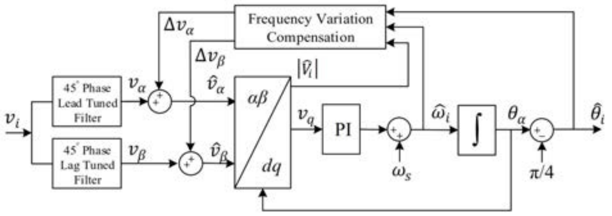


Fig. 2: *Phase lead-lag synchronous reference frame PLL.*

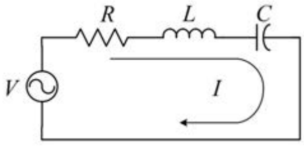


Fig. 3: *Series RLC circuit.*

2.1 45° Phase-Lead Tuned Filter

The 45° phase-lead tuned filter must be designed to achieve a unity gain and +45° phase displacement at the nominal frequency of 50 Hz. They are expressed as,

$$\angle T(s)|_{s=j\omega_s} = \frac{\pi}{4} \tag{2}$$

$$|T(s)|_{s=j\omega_s} = 1 \tag{3}$$

where the nominal frequency is denoted by ω_s (rad/sec). The natural frequency $\omega_{n\alpha}$ yielding a +45° phase lead at 50 Hz and the constant gain $k_{L\alpha}$ yielding the unity gain are expressed as,

$$\omega_{n\alpha} = \frac{\frac{\omega_s}{Q_\alpha} + \sqrt{\left(\frac{\omega_s}{Q_\alpha}\right)^2 + (2\omega_s)^2}}{2} \tag{4}$$

$$k_{L\alpha} = \sqrt{\left(\frac{\omega_{n\alpha}^2 - \omega_s^2}{\omega_s}\right)^2 + \left(\frac{\omega_{n\alpha}}{Q_\alpha}\right)^2} \tag{5}$$

It should be noted that the natural frequency of the filter is slightly higher than the nominal level.

2.2 45° Phase-Lag Tuned Filter

The phase-lag tuned filter can be designed in a similar way to the phase-lead tuned filter. The unity gains and a −45° phase-lag at the power frequency of 50 Hz can be obtained by the following equations.

$$\angle T(s)|_{s=j\omega_s} = -\frac{\pi}{4} \tag{6}$$

$$|T(s)|_{s=j\omega_s} = 1 \tag{7}$$

The natural frequency $\omega_{n\beta}$ and the constant gain $k_{L\beta}$ are solved and expressed as,

$$\omega_{n\beta} = \frac{-\frac{\omega_s}{Q_\beta} + \sqrt{\left(\frac{\omega_s}{Q_\beta}\right)^2 + (2\omega_s)^2}}{2} \tag{8}$$

$$k_{L\beta} = \sqrt{\left(\frac{\omega_{n\beta}^2 - \omega_s^2}{\omega_s}\right)^2 + \left(\frac{\omega_{n\beta}}{Q_\beta}\right)^2} \tag{9}$$

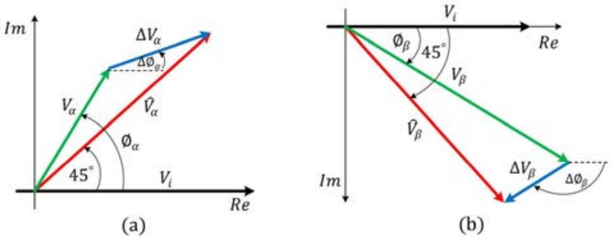


Fig. 4: *Steady-state phasor of the grid voltage after filtering by the tuned filters: (a) phase-lead voltage (b) phase-lag voltage.*

However, the natural frequency of the filter is slightly less than the nominal frequency. The design guidelines and example of single tuned filters will be discussed and illustrated in Section 3.

2.3 Frequency Variation Compensation

Under poor quality conditions, the power frequency may vary slightly between 47° and 52 Hz [2], causing phase displacement and gains in phase-lead and phase-lag tuned filters differing from 45° and unity respectively.

Fig. 4 (a) shows a steady-state phasor of the grid voltage after being filtered by the phase-lead tuned filter. If the frequency of the grid voltage is slightly less than the nominal level, the magnitude of a phasor of the phase-lead voltage will be slightly less than that of the grid voltage and the phase angle greater than 45°. The phase-lead compensation voltage ΔV_α is added to correct the magnitude and phase angle of the phase-lead voltage $\hat{V}_\alpha$. The compensated phase-lead voltage is expressed as,

$$\hat{V}_\alpha = V_\alpha + \Delta V_\alpha \tag{10}$$

It should be noted that a variable with a circumflex refers to an estimate hereafter. Let the grid voltage v_i and the phase-lead voltage v_α be expressed in sinusoidal or complex exponential functions by Eqs. (11) and (12). The phase-lead compensation voltage Δv_α can be solved as follows:

$$v_i = |V_i| \sin(\omega_i t) = \mathrm{Im}\left\{ |V_i|\, e^{j\omega_i t} \right\} \tag{11}$$

$$v_\alpha = |V_\alpha| \sin(\omega_i t + \phi_\alpha) = \mathrm{Im}\left\{ |V_\alpha|\, e^{j(\omega_i t + \phi_\alpha)} \right\} \tag{12}$$

$$\begin{aligned} \Delta v_\alpha = {} & \mathrm{Re}\left\{ |\Delta V_\alpha|\, e^{j\Delta\phi_\alpha} \right\} \sin(\hat{\omega}_i t) + \\ & \mathrm{Im}\left\{ |\Delta V_\alpha|\, e^{j\Delta\phi_\alpha} \right\} \cos(\hat{\omega}_i t) \end{aligned} \tag{13}$$

$$\begin{aligned} \mathrm{Re}\left\{ |\Delta V_\alpha|\, e^{j\Delta\phi_\alpha} \right\} = {} & \frac{|V_s|}{\sqrt{2}} \\ & - \left| \frac{j\hat{\omega}_i k_\alpha}{(\omega_{n\alpha}^2 - \hat{\omega}_i^2) + j\frac{\omega_{n\alpha}\hat{\omega}_i}{Q_\alpha}} \right| |\hat{V}_i| \cos(\phi_\alpha) \end{aligned} \tag{14}$$

$$\begin{aligned} \mathrm{Im}\left\{ |\Delta V_\alpha|\, e^{j\Delta\phi_\alpha} \right\} = {} & \frac{|V_s|}{\sqrt{2}} \\ & - \left| \frac{j\hat{\omega}_i k_\alpha}{(\omega_{n\alpha}^2 - \hat{\omega}_i^2) + j\frac{\omega_{n\alpha}\hat{\omega}_i}{Q_\alpha}} \right| |\hat{V}_i| \sin(\phi_\alpha) \end{aligned} \tag{15}$$

$$\phi_\alpha = \frac{\pi}{2} - \tan^{-1}\left(\frac{\omega_{n\alpha}\hat{\omega}_i}{(\omega_{n\alpha}^2 - \hat{\omega}_i^2)Q_\alpha} \right) \tag{16}$$

$$|\hat{V}_i| = \sqrt{v_d^2 + v_q^2} \tag{17}$$

where $|V_s|$ and $|\hat{V}_i|$ denote the magnitude of the nominal voltage and estimated grid voltage respectively, $\hat{\omega}_i$ is the estimated frequency, and ϕ_α is a phase angle of the phase-lead voltage.

Fig. 4 (b) shows a phasor of the phase-lag voltage V_β. The magnitude and phase of the phase-lag voltage V_β are corrected in a similar manner to that previously mentioned. The phase-lag compensation voltage $\hat{V}_\beta$ is expressed as,

$$\hat{V}_\beta = V_\beta + \Delta V_\beta \tag{18}$$

Let the phase-lag voltage v_β be expressed as a sinusoidal or complex exponential function by Eqs. (19) and (20). The phase-lag compensation voltage Δv_β can be solved as follows:

$$v_\beta = |V_\beta| \sin(\omega_i t + \phi_\beta) = \mathrm{Im}\left\{ |V_\beta|\, e^{j(\omega_i t + \phi_\beta)} \right\} \tag{19}$$

$$\begin{aligned} \Delta v_\beta = {} & \mathrm{Re}\left\{ |\Delta V_\beta|\, e^{j\Delta\phi_\beta} \right\} \sin(\hat{\omega}_i t) + \\ & \mathrm{Im}\left\{ |\Delta V_\beta|\, e^{j\Delta\phi_\beta} \right\} \cos(\hat{\omega}_i t) \end{aligned} \tag{20}$$

$$\begin{aligned} \mathrm{Re}\left\{ |\Delta V_\beta|\, e^{j\Delta\phi_\beta} \right\} = {} & \frac{|V_s|}{\sqrt{2}} \\ & - \left| \frac{j\hat{\omega}_i k_\beta}{(\omega_{n\beta}^2 - \hat{\omega}_i^2) + j\frac{\omega_{n\beta}\hat{\omega}_i}{Q_\beta}} \right| |\hat{V}_i| \cos(\phi_\beta) \end{aligned} \tag{21}$$

$$\begin{aligned} \mathrm{Im}\left\{ |\Delta V_\beta|\, e^{j\Delta\phi_\beta} \right\} = {} & -\frac{|V_s|}{\sqrt{2}} \\ & - \left| \frac{j\hat{\omega}_i k_\beta}{(\omega_{n\beta}^2 - \hat{\omega}_i^2) + j\frac{\omega_{n\beta}\hat{\omega}_i}{Q_\beta}} \right| |\hat{V}_i| \sin(\phi_\beta) \end{aligned} \tag{22}$$

$$\phi_\beta = \frac{\pi}{2} - \tan^{-1}\left(\frac{\omega_{n\beta}\hat{\omega}_i}{(\omega_{n\beta}^2 - \hat{\omega}_i^2)Q_\beta} \right) \tag{23}$$

where ϕ_β denotes phase angle of the phase-lag voltage v_β, even though the compensated voltages are derived in the stead-state basis. It will be validated by experiments to show that the method is capable of tracking phase and frequency of the grid voltage during a transient period from one steady-state condition to another under a step frequency change or a frequency ramp.

The calculations of $\left|G_\alpha(s)\}\right|$ and $\left|G_\beta(s)\right|$ in Eqs. (14), (15), (21), and (22) seem to be computationally troublesome for a low cost processor. Each can be computed offline as a function of frequency and programmed into the memory of a processor instead.

3. SMALL SIGNAL MODEL

The small signal model is essential because it enables the use of linear system analysis tools in designing a feedback controller to achieve the required performance. For simplicity, it is assumed that the grid voltage is purely sinusoidal. The harmonic voltage is treated separately in steady state as a disturbance, while the DC offset is removed by the tuned filters. The grid voltage is defined by a sinusoidal function as,

$$v_i(t) = \left|V_i\right| \cos(\omega_i t + \phi_i) \tag{24}$$

where amplitude, frequency and phase angle of the grid voltage are denoted by $\left|V_i\right|$, ω_i, and ϕ_i respectively. At the instant, the grid voltage is applied to the single tuned filters, two orthogonal voltages $\hat{v}_\alpha$ and $\hat{v}_\beta$ in Fig. 2 are generated. Assume the load quality factors are greater than 0.5. They are expressed as follows:

$$\hat{v}_\alpha = v_\alpha(t) + \Delta v_\alpha(t) \tag{25}$$

$$\begin{aligned} v_\alpha(t) = {} & \left|V_i\right| \left|G_\alpha(j\omega_i)\right| \cos\left(\omega_i t + \phi_i + \angle G_\alpha(j\omega_i)\right) + \\ & A_\alpha \cos\left(\omega_{n\alpha}\sqrt{1-\left(\frac{1}{2Q_\alpha}\right)^2}\, t + \varphi_\alpha\right) e^{-\frac{\omega_{n\alpha}}{2Q_\alpha}t} \end{aligned} \tag{26}$$

$$\begin{aligned} \Delta v_\alpha(t) = {} & \left|V_s\right| \cos\left(\hat{\omega}_i t + \phi_i + \frac{\pi}{4}\right) - \\ & \left|\hat{V}_i\right| \left|G_\alpha(j\hat{\omega}_i)\right| \cos\left(\hat{\omega}_i t + \phi_i + \angle G_\alpha(j\hat{\omega}_i)\right) \end{aligned} \tag{27}$$

$$\hat{v}_\beta = v_\beta(t) + \Delta v_\beta(t) \tag{28}$$

$$\begin{aligned} v_\beta(t) = {} & \left|V_i\right| \left|G_\beta(j\omega_i)\right| \cos\left(\omega_i t + \phi_i + \angle G_\beta(j\omega_i)\right) + \\ & A_\beta \sin\left(\omega_{n\beta}\sqrt{1-\left(\frac{1}{2Q_\beta}\right)^2}\, t + \varphi_\beta\right) e^{-\frac{\omega_{n\beta}}{2Q_\beta}t} \end{aligned} \tag{29}$$

$$\begin{aligned} \Delta v_\beta(t) = {} & \left|V_s\right| \cos\left(\hat{\omega}_i t + \phi_i - \frac{\pi}{4}\right) - \\ & \left|\hat{V}_i\right| \left|G_\beta(j\hat{\omega}_i)\right| \cos\left(\hat{\omega}_i t + \phi_i + \angle G_\beta(j\hat{\omega}_i)\right) \end{aligned} \tag{30}$$

where A_α and A_β are amplitudes of the oscillating terms and φ_α and φ_β their phase shifts, accordingly. They are functions of the magnitude and phase angle of the grid voltage and load quality factors. The load quality factors should be greater than 0.5 to achieve a fast dynamic response, otherwise, the poles of their characteristic equations will split into two different real numbers. A slow dynamic response will then dominate due to a small negative real root.

Park transformation is employed to transform the two orthogonal voltages into the dq-synchronous reference frame and is given by the following equation.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\theta_\alpha) & \sin(\theta_\alpha) \\ -\sin(\theta_\alpha) & \cos(\theta_\alpha) \end{bmatrix} \begin{bmatrix} \hat{v}_\alpha \\ \hat{v}_\beta \end{bmatrix} \tag{31}$$

$$\theta_\alpha(t) = \int \hat{\omega}_i dt + \hat{\phi}_i + \frac{\pi}{4} \tag{32}$$

Under a quasi-frequency locked state, let us assume that the estimated magnitude and frequency are essentially equal to that of the grid voltage as follows:

$$\left|\hat{V}_i\right| \approx \left|V_s\right| \tag{33}$$

$$\hat{\omega}_i \approx \omega_i \tag{34}$$

Applying Taylor's series approximation, the small phase difference between the estimated phase and actual phase of the grid voltage is approximated as follows:

$$\sin(\phi_i - \hat{\phi}_i) \approx \phi_i - \hat{\phi}_i \tag{35}$$

$$\cos(\phi_i - \hat{\phi}_i) \approx 1 \tag{36}$$

Substituting Eqs. (25) and (28) into Eq. (31) and applying the assumptions in Eqs. (35) and (36), the quadrature voltage v_q is expressed as, (detailed in Appendix)

$$v_q(t) = \left|V_s\right| (\phi_i - \hat{\phi}_i) + g(t) + h(t) \tag{37}$$

$$\begin{aligned} g(t) = {} & -e^{-\frac{t}{\tau_\alpha}} \\ & \left(A_\alpha \cos(\omega_{n\alpha}\sqrt{1-\left(\frac{1}{2Q_\alpha}\right)^2}\, t + \varphi_\alpha) \sin(\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4})\right) \end{aligned}$$

$$\begin{aligned} h(t) = {} & -e^{-\frac{t}{\tau_\beta}} \\ & \left(A_\beta \sin(\omega_{n\beta}\sqrt{1-\left(\frac{1}{2Q_\beta}\right)^2}\, t + \varphi_\beta) \cos(\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4})\right) \end{aligned}$$

$$\tau_\alpha = \frac{2Q_\alpha}{\omega_{n\alpha}}, \ \tau_\beta = \frac{2Q_\beta}{\omega_{n\beta}}$$

where τ_α and τ_β denote time constants of the oscillating terms $g(t)$ and $h(t)$.

When a sudden phase jump occurs, they will exponentially decay to zero with the corresponding time constants. Thus, dynamic response of the quadrature-phase v_q due to a step phase change can be modeled by a first-order transfer function in frequency domain as,

$$\frac{V_q(s)}{\Phi_i(s) - \hat{\Phi}_i(s)} = \frac{|V_s|}{\tau_p s + 1} \tag{38}$$

$$\tau_p = \min(\tau_\alpha, \tau_\beta) \tag{39}$$

where τ_p denotes a time constant of the small signal model. It is chosen by minimum value of the time constants τ_α and τ_β so that fast dynamic response is achieved and worst case attenuation can be guaranteed. As a result of the frequency variation compensation, the small signal model has a constant DC gain of the nominal magnitude $|V_s|$ in spite of the occurrences of voltage sag, swell or flicker.

The steady state effect of the harmonic voltage is treated as a disturbance. Let the harmonic voltage be defined by sum of sinusoidal functions as,

$$v_h(t) = \sum_{h=3,5,7\ldots} |V_h| \cos(h\omega_i t + \phi_h) \tag{40}$$

where h and ϕ_h denote the harmonic order and phase shift respectively. When it enters the tuned filters, two harmonic voltages in the $\alpha\beta$-stationary reference frame are generated and expressed as,

$$v_{\alpha h}(t) = \\ |G_\alpha(j\omega_i)| \sum_{h=3,5,7\ldots} |V_h| \cos(h\omega_i t + \phi_h + \angle G_\alpha(j\omega_i)) \tag{41}$$

$$v_{\beta h}(t) = \\ |G_\beta(j\omega_i)| \sum_{h=3,5,7\ldots} |V_h| \cos(h\omega_i t + \phi_h + \angle G_\beta(j\omega_i)) \tag{42}$$

Applying Park transformation in Eq. (31), they can be transformed to the dq-synchronous reference frame with the quadrature harmonic voltage expressed as,

$$v_{qh}(t) = \sum_{h=3,5,7\ldots} (v_{q,(h+1)} + v_{q,(h-1)}) \tag{43}$$

$$v_{q,(h+1)}(t) = |V_{q,(h+1)}| \cos\left((h+1)\omega_i t + \phi_{q,(h+1)}\right) \tag{44}$$

$$v_{q,(h-1)}(t) = |V_{q,(h-1)}| \cos\left((h-1)\omega_i t + \phi_{q,(h-1)}\right) \tag{45}$$

where

$$|V_{q,(h+1)}| = \frac{|V_h|}{2} \cdot \\ (|G_\alpha(j\omega_i)|^2 + |G_\beta(j\omega_i)|^2 - 2\,|G_\alpha(j\omega_i)|\,|G_\beta(j\omega_i)| \\ \sin(\angle G_\alpha(j\omega_i) - \angle G_\beta(j\omega_i)))^{\frac{1}{2}}$$

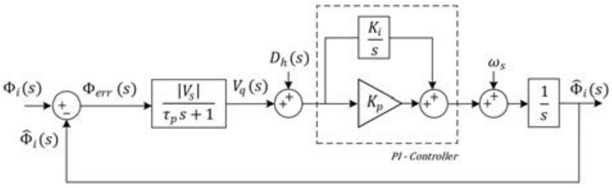


***Fig. 5**: The small signal model of the proposed method.*

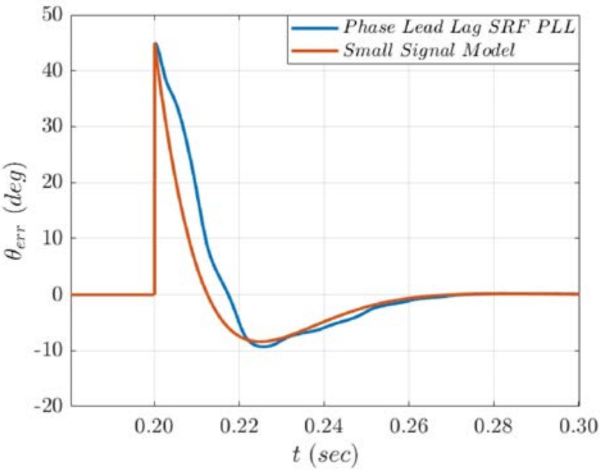


***Fig. 6**: Phase error under a sudden 45° phase jump.*

$$|V_{q,(h-1)}| = \frac{|V_h|}{2} \cdot \\ (|G_\alpha(j\omega_i)|^2 + |G_\beta(j\omega_i)|^2 + 2\,|G_\alpha(j\omega_i)|\,|G_\beta(j\omega_i)| \\ \sin(\angle G_\alpha(j\omega_i) - \angle G_\beta(j\omega_i)))^{\frac{1}{2}}$$

and $\phi_{q,(h+1)}$ and $\phi_{q,(h-1)}$ denote the phase angle of their respective harmonic voltages. Applying Laplace transform, the quadrature harmonic voltage in Eq. (43) is represented in frequency domain as,

$$D_h(s) = \mathscr{L}\left\{\sum_{h=3,5,7,\ldots} v_{qh}(t)\right\} \tag{46}$$

where $\mathscr{L}$ denotes the Laplace operator.

Fig. 5 shows a block diagram of the small signal model. The phase error is proportional to the quadrature voltage v_q. It is regulated to zero by a PI-controller to estimate the grid frequency. The phase angle is obtained by integrating the estimated frequency. To transform the h-order harmonic voltage into the dq-synchronous reference frame, a pair of $(h \pm 1)$ order harmonic voltages, attenuated by a PI controller.

Fig. 6 shows the simulation results of the phase error with the small signal model and the proposed method when a sudden +45° phase jump occurs. The simulation is performed based on the same PI controller. The small signal model yields a slightly faster rise-time than the proposed method. Both models have almost comparable overshoots and approach the steady state with the same

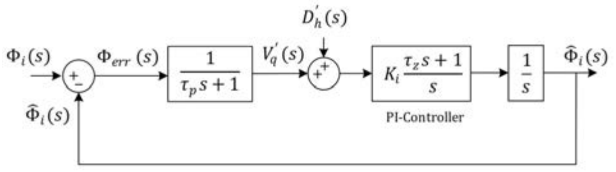


***Fig. 7**: Normalized feedback loop.*

settling time. The results confirm that the small signal model is valid and can be used to design the PI-controller present in the next section.

4. DESIGN GUIDELINES

In this section, the design guidelines for compromising the fast transient response, acceptable phase margin, and sufficient harmonic attenuation are presented and discussed. In practice, this involves the selection of two primary parameters: damping ratio and load quality. The design criteria for meeting the required specification or performance is as follows:

Transient Performance:

Let the magnitude of the grid voltage be normalized to one. The small signal model and disturbance transfer function are divided by $|V_s|$ and expressed as,

$$G'_p(s) = \frac{1}{\tau_p s + 1} \tag{47}$$

$$D'_h(s) = \frac{D_h(s)}{|V_s|} \tag{48}$$

The transfer function of a PI-controller is expressed as,

$$C(s) = K_i \frac{\tau_z s + 1}{s} \tag{49}$$

where $\tau_z = \frac{K_p}{K_i}$, an integrator has a transfer function in frequency domain which is expressed as,

$$H(s) = \frac{1}{s} \tag{50}$$

Fig. 7 shows the normalized feedback loop of the proposed method. The transfer function between the phase error and the input phase is defined by the expression.

$$G_e(s) = \left.\frac{\Phi_{err}(s)}{\Phi_i(s)}\right|_{D'_h(s)=0} = \frac{1}{1 + G_{OL}(s)} \tag{51}$$

where $G_{OL}(s) = G'(s)C(s)H(s)$.

Using the symmetrical optimum method [3-4], the transfer function in Eq. (51) is written in a general form using the following expression.

$$G_e(s) = \frac{s^2(s + (2\zeta + 1)\omega_n)}{(s + \omega_n)(s^2 + 2\zeta\omega_n s + \omega_n^2)} \tag{52}$$

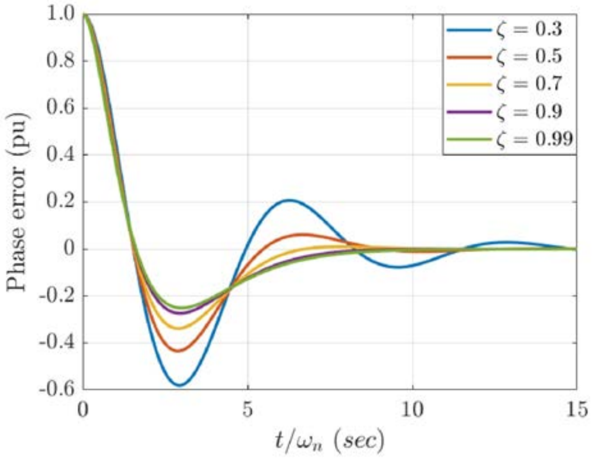


***Fig. 8**: Transient response of the phase error for different values of the damping ratio.*

where ζ and ω_n denote the damping ratio and the natural frequency, respectively. Their relationships with the time constants are expressed as follows:

$$\frac{\tau_z}{\tau_p} = (2\zeta + 1)^2 \tag{53}$$

$$\tau_z \tau_p = \frac{1}{\omega_n^2} \tag{54}$$

Let a step phase change be represented by a unit step function and expressed as,

$$\Phi_i(s) = \frac{\Delta\phi}{s} \tag{55}$$

The response of the phase error subject to the step phase change Eq. (55) is expressed as,

$$\Phi_{err}(s) = \frac{s(s + (s\zeta + 1)\omega_n)\Delta\phi}{(s + \omega_n)(s^2 + 2\zeta\omega_n s + \omega_n^2)} \tag{56}$$

Applying the inverse Laplace transform, the phase error in Eq. (56) is expressed in the time domain as, [4-5]

$$\phi_{err}(s) = \begin{cases} \frac{\Delta\phi}{\zeta-1}(\zeta e^{-\omega_n t} - e^{-\omega_n t}\cos(\sqrt{1-\zeta^2}\omega_n t)) & ;\zeta < 1 \\ \Delta\phi e^{-\omega_n t}(1 - \omega_n t + \omega_n^2 t^2) & ;\zeta = 1 \\ \frac{\Delta\phi}{\zeta-1}(\zeta e^{-\omega_n t} - \frac{1}{2}e^{-\left(\zeta-\sqrt{\zeta^2-1}\right)\omega_n t} & \\ -\frac{1}{2}e^{-(\zeta+\sqrt{\zeta^2-1})\omega_n t}) & ;\zeta > 1 \end{cases} \tag{57}$$

Fig. 8 shows the transient response of the phase error for different values of damping ratios as the time is normalized by the natural frequency ω_n. The optimal damping ratio is about 0.7 because it yields the least settling time with an acceptable overshoot.

Stability:

After determining the damping ratio, the phase margin of the feedback loop is evaluated. Neglecting the disturbance, the open-loop transfer function of the normalized feedback loop in Fig. 7 is expressed as,

$$G_{ol}(s) = \left.\frac{\hat{\Phi}_i(s)}{\Phi_i(s)}\right|_{D'_h(s)=0} = K_i \frac{\tau_Z s + 1}{s^2(\tau_p s + 1)} \tag{58}$$

It has one zero and one pole in the left half-plane and two poles at the origin. The role of a zero-pole pair in Eq. (58) is to provide a phase boost where the maximum phase margin (PM) occurs at the gain crossover frequency ω_c and is expressed as,

$$PM = \tan^{-1}(\omega_c \tau_z) - \tan^{-1}(\omega_c \tau_p) \tag{59}$$

where $\omega_c = \omega_n = \frac{1}{\sqrt{\tau_z \tau_p}}$
The gains of PI-controller can be calculated as follows:

$$K_p = \omega_c \tag{60}$$

$$K_i = \tau_p K_p^2 \tag{61}$$

The time constant τ_p has direct impact on transient performance and the harmonic attenuation. It is determined through the selection of load quality factors, as discussed in the following step.

Harmonic Attenuation:

The selection of the load quality factors is a compromise. That is, the smaller the load quality factor, the faster the transient response but this results in less attenuation. The transfer function of the estimated phase and the disturbance is defined in a general form as follows:

$$\begin{aligned} G_d(s) &= \left.\frac{\hat{\Phi}_i(s)}{D'_h(s)}\right|_{\Phi_i(s)=0} \\ &= \frac{\omega_n(s + \omega_n/(2\zeta + 1))(s + \omega_n(2\zeta + 1))}{(s + \omega_n)(s^2 + 2\zeta\omega_n s + \omega_n^2)} \end{aligned} \tag{62}$$

According to Eq. (43), the second harmonic is of the lowest order in the quadrature-phase voltage v_q. It must be attenuated as much as possible to reduce phase error oscillation. Let it be considered as a disturbance. The second harmonic attenuation can be calculated by the following equation.

$$\begin{aligned} Atten|_{s=j2\omega_s} &= \\ &\frac{1}{2}\left|G_d(j2\omega_i)\right|(\left|G_\alpha(j3\omega_i)\right|^2 + \left|G_\beta(j3\omega_i)\right|^2 \cdots \\ &+ 2\left|G_\alpha(j3\omega_i)\right|\left|G_\beta(j3\omega_i)\right|\sin(\phi_{\alpha\beta,h=3})) \end{aligned} \tag{63}$$

where $\phi_{\alpha\beta,h=3} = \angle G_\alpha(j3\omega_i) - \angle G_\beta(j3\omega_i)$.
The attenuation involves two undetermined variables: Q_α and Q_β. Let the damping ratio be set to the optimal value $\zeta = 0.7$. The time constants τ_α and τ_β are calculated as a function of the load quality factor, shown in Fig. 9. The load quality factor Q_β should be set to 0.5 because it yields the minimum time constant τ_β of 7.685 ms.

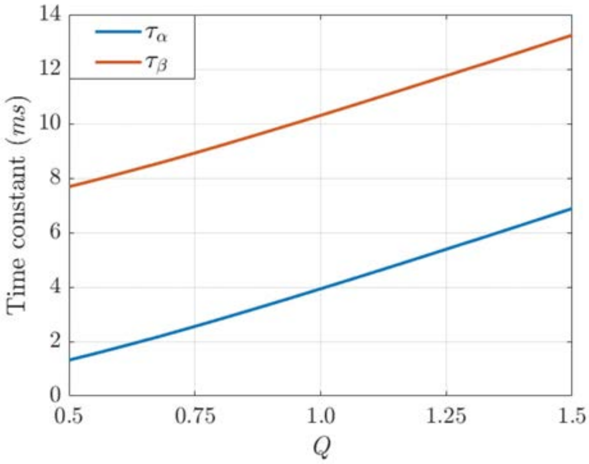


***Fig. 9**: Time constants of a phase-lead tuned filter and a phase-lag tuned filter as a function of a load quality factor.*

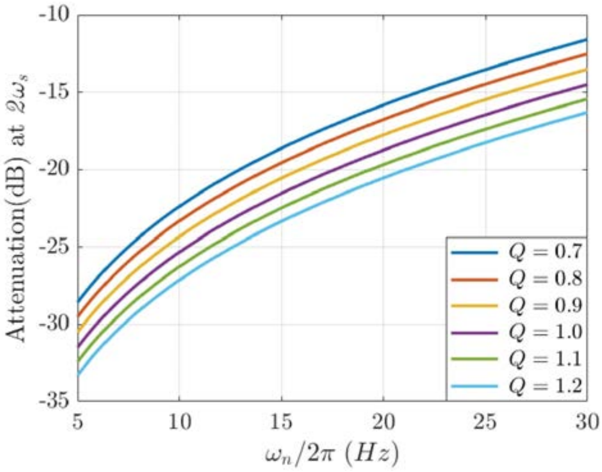


***Fig. 10**: Harmonic attenuation as a function of the natural frequency at damping ratio $\zeta = 0.7$.*

Fig. 10 shows the harmonic attenuation as a function of the natural frequency for different values of the load quality factor Q_α. The phase margin is evaluated for different values of the damping ratio, as shown in Fig. 11. While the phase margin and the harmonic attenuation are taken into consideration concurrently, the load quality factor Q_α should be chosen within the range of 0.8 – 1.0. Thus, the worst-case attenuation of -14 dB can be obtained, whereas the minimum phase margin of 40° is guaranteed at the natural frequency of 25 Hz. The design guidelines are summarized and examples are illustrated in Table 1.

Design Example:

Following the design example in Table 1, the frequency response of the phase-lead and phase-lag tuned filters are shown in Fig. 12. The unity gains and phase displacement of 45° at the nominal frequency are obtained. It should be noted that when the load quality factor Q_α is less than 0.9, the third harmonic

***Table 1**: Design guideline and example.*

Parameters	Design Guidlines	Design Example
Load quality factor, Q_α	0.8–1.0	0.9
Load quality factor, Q_β	0.5	0.5
Damping ratio, ζ	0.7	0.7
Natural frequency, ω_n	20–25 Hz	19.7 Hz
Phase margin (PM)	40° – 45°	44.8°
Attenuation (dB) at $2\omega_s$	-14– -18 dB	-17 dB
Proportional gain K_P	Eq. (60)	124
Proportional gain K_I	Eq. (61)	6.365

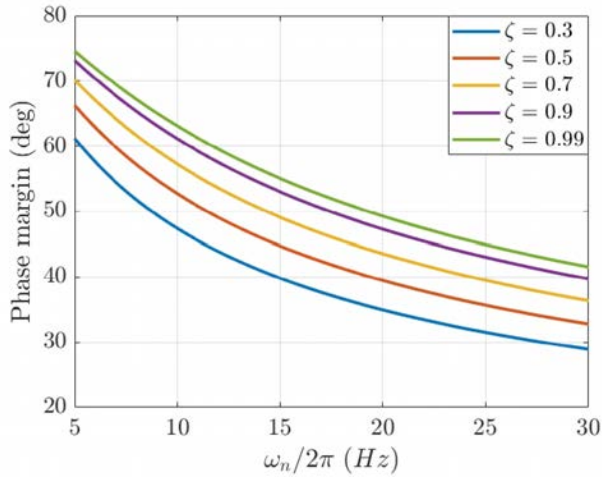


***Fig. 11**: Phase margin for different values of the damping ratio.*

may be amplified, and filtering capability of the feedback loop degraded. Thus, appropriate selection of the load quality factor may require a power quality assessment beforehand. Fig. 13 shows the frequency response of the opened loop $G_{ol}(s)$, ensuring that the feedback loop is stable. The phase margin of 44.8° at the crossover frequency of 19.7 Hz is obtained. The design example yields harmonic attenuation of -17 dB at twice the nominal frequency. The validation and effectiveness of the proposed method are presented and discussed in the following section.

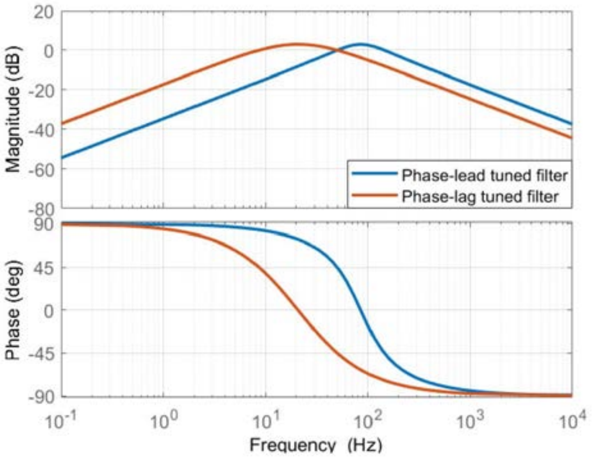


***Fig. 12**: Frequency response of the phase-lead tuned filter and the phase-lag tuned filter.*

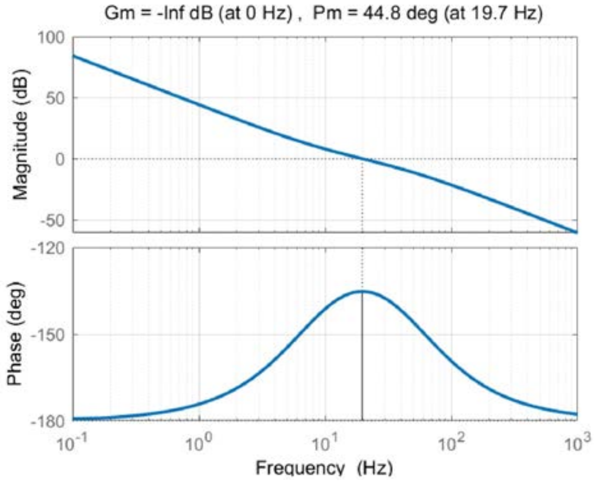


***Fig. 13**: Frequency response and phase margin of the design example.*

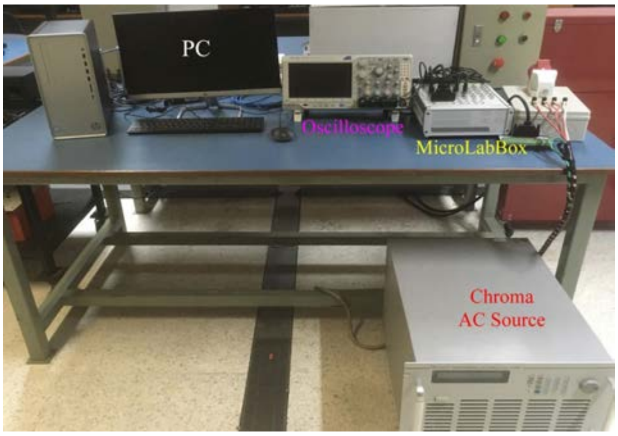


***Fig. 14**: Hardware setup.*

5. EXPERIMENTAL VALIDATION

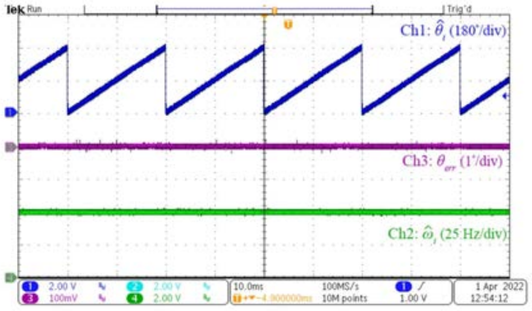
The phase lead-lag synchronous reference frame phase-locked loop is implemented in real time using a rapid prototyping MicroLabBox. It has an NXP (Freescale) QorlQ P5020 dual-core real-time processor running at 2 GHz; a user-programmable FPGA; 16-bit analog-to-digital conversion inputs (ADC); and digital to analog conversion outputs (DAC), etc. The algorithm is programmed on the dSPACE Real-Time Interface for Simulink®. The parameters of the design example presented in Table 1 are used for implementation. Fig. 14 shows the hardware setup in a laboratory. Different voltage conditions are created using computational block sets in MATLAB/Simulink, scaled by a factor of 0.02, and converted to analog control signals in a range of ±10 V by a 16-bit DAC. It is then sent to a programmable AC source Chroma 61704. When the control signal is received, the programmable AC source amplifies it by a factor of 50 and generates the output voltage which is used as a reference voltage for the experiments. Due to the low operating voltage range of an analog-to-digital converter, the reference voltage is attenuated by a resistive divider circuit within a range of ±10 V before it can be interfaced with the MicroLabBox. While the algorithm is being executed, the attenuated reference voltage is sampled via a 16-bit ADC and processed repeatedly at 10 kHz. The experimental and simulation results are discussed case by case as follows:

A. Normal Voltage

Fig. 15 shows the experimental results of the proposed method in the steady state under normal voltage conditions. Fig. 15(a) shows a triangular waveform as the estimated phase of the grid voltage. At zero crossing, the estimated phase is wrapped or reset to zero. Afterward, it increases by 1.8° every time step of $100\mu s$ until it reaches 360° when it is reset to zero and begins to repeat the tracking phase for the next cycle. The results confirm that the algorithm can track the phase and estimated frequency of the grid voltage accurately with almost zero errors. Fig. 15(b) shows the waveforms of the compensated voltages $\hat{v}_\alpha$ and $\hat{v}_\beta$. These have the same magnitude as the grid voltage but ±45° phase displacement with respect to the grid voltage. Fig. 15(c) and (d), show the compensation voltages Δv_α and Δv_β. They are equal to zero since the frequency of the grid voltage is constant at 50 Hz. Fig. 16 shows the simulation results. The method can track the phase of the grid voltage with zero steady state error.

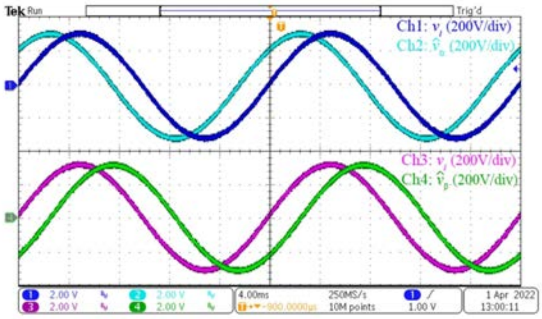
B. Distorted Harmonic Voltage

Fig. 17 presents the experimental results of the proposed method under distorted harmonic voltage conditions. The third harmonic voltage with a magnitude of 15% is added to the grid voltage. Fig. 17(a) shows the phase error fluctuation with twice the grid frequency and an amplitude of 3° peak-peak, corresponding to an attenuation of 15dB, which is higher than the expected attenuation of -17 dB. As can be observed, the estimated frequency varies in the vicinity of 50 Hz with an amplitude of 5 Hz peak-peak. Fig. 17(b) indicates the compensated voltages $\hat{v}_\alpha$ and $\hat{v}_\beta$. The third harmonic voltage is better attenuated in the compensated phase-lag voltage $\hat{v}_\beta$ than the other. Fig. 17(c)–(d) shows the frequency compensation voltages Δv_α and Δv_β. They are not equal to zero due to the presence of estimated frequency and magnitude variation. In the case where less phase error fluctuation is required, the higher load quality factor Q_α can be chosen but the tradeoff is a slow transient response. Fig. 18 presents the simulation results. The method yields a phase error of about 3.2° peak-peak and a frequency error of 6 Hz peak-peak. The simulation results are consistent with the experimental results.



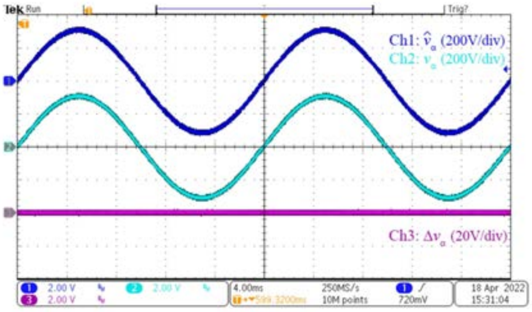
Ch1: Estimated phase, $\hat{\theta}_i$
Ch2: Estimated frequency, $\hat{\omega}_i$
Ch3: Phase error, θ_{err}

(a)



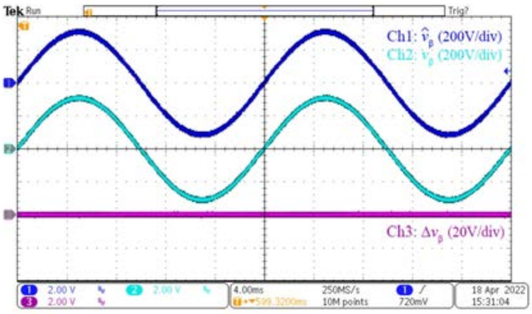
Ch1,Ch3: Grid voltage, v_i
Ch2: Compensated phase-lead voltage, $\hat{v}_\alpha$
Ch4: Compensated phase-lag voltage, $\hat{v}_\beta$

(b)



Ch1: Compensated phase-lead voltage, $\hat{v}_\alpha$,
Ch2: Phase-lead voltage, v_α
Ch3: Phase-lead compensation voltage, Δv_α

(c)



Ch1: Compensated phase-lag voltage, $\hat{v}_\beta$,
Ch2: Phase-lag voltage, v_β
Ch3: Phase-lag compensation voltage, Δv_β

(d)

***Fig. 15**: Experimental results under normal voltage.*

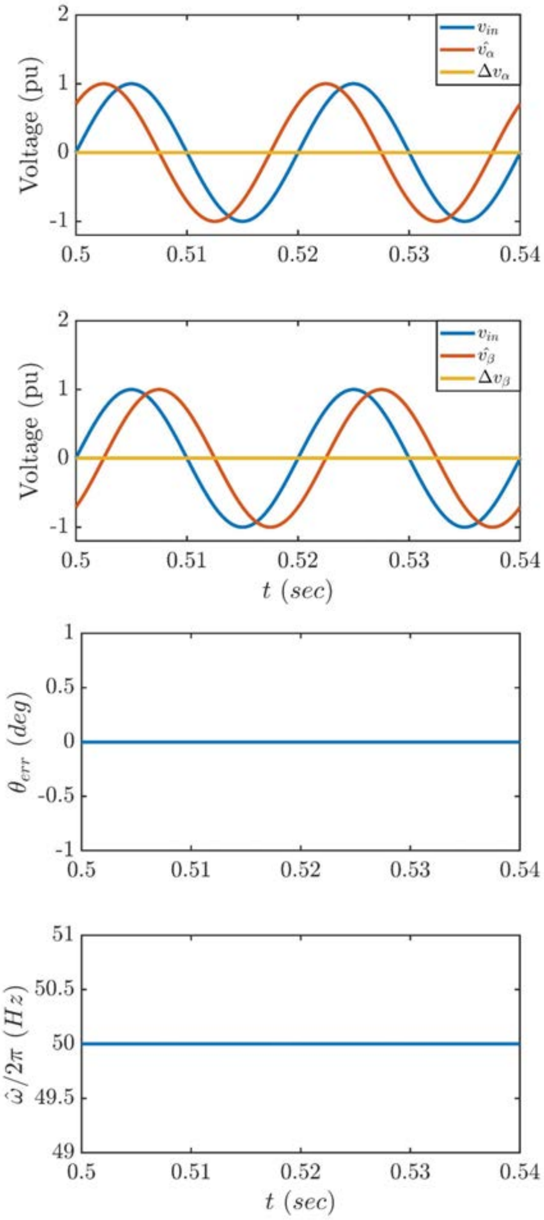
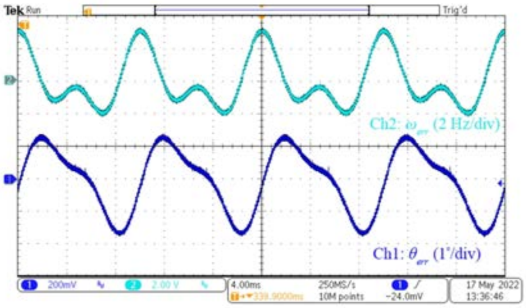


***Fig. 16**: Simulation results under the normal voltage.*

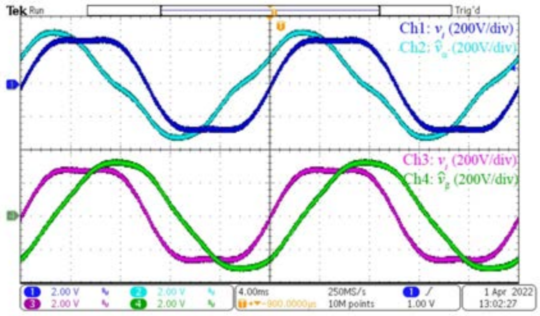
C. Phase Jump

Fig. 19(a) shows the dynamic responses of the phase error and estimated frequency when a sudden phase jump of +45° occurs. The phase error abruptly rises to +45° and then rapidly returns to zero within 55 ms or 2.75 cycles with an undershoot of 17° as shown in Fig. 19(b). The estimated frequency peaks at almost 10 Hz above the grid frequency at 50 Hz and returns to steady state in 2 cycles. The sudden phase jump of −45° is repeated. The phase error and estimated frequency can return to steady state within 2.5 cycles and 2 cycles, respectively. Fig. 19(c) shows the compensated phase-lead and phase-lag voltage in comparison to the grid voltage while the phase jump occurs. After the phase error is regulated to zero, the phase displacement becomes 45° with respect to the phase of the grid voltage. Fig. 19(d)–(e) shows



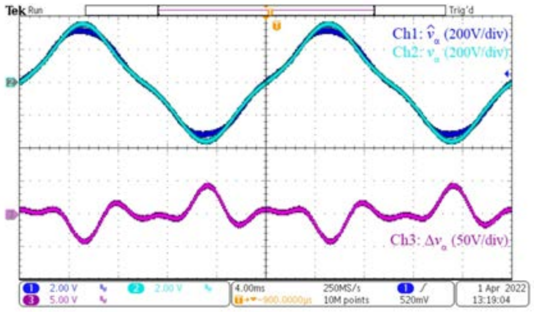
Ch1: Phase error, θ_{err}
Ch2: Frequency error, ω_{err}

(a)



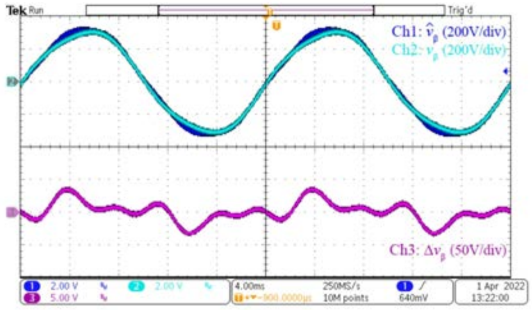
Ch1,Ch3: Grid voltage, v_i
Ch2: Compensated phase-lead voltage, $\hat{v}_\alpha$
Ch4: Compensated phase-lag voltage, $\hat{v}_\beta$

(b)



Ch1: Compensated phase-lead voltage, $\hat{v}_\alpha$,
Ch2: Phase-lead voltage, v_α
Ch3: Phase-lead compensation voltage, Δv_α

(c)



Ch1: Compensated phase-lag voltage, $\hat{v}_\beta$,
Ch2: Phase-lag voltage, v_β
Ch3: Phase-lag compensation voltage, Δv_β

(d)

***Fig. 17**: Experimental results under the distorted harmonic voltage.*

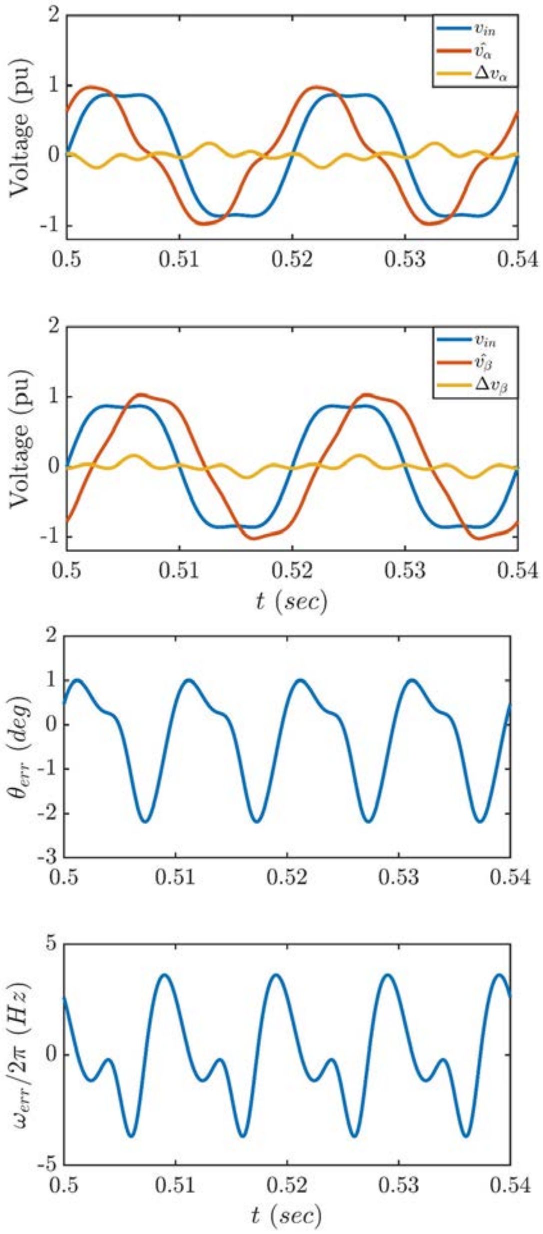
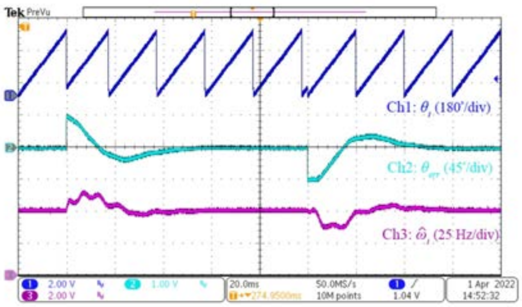


Fig. 18: *Simulation results under the distorted harmonic voltage.*

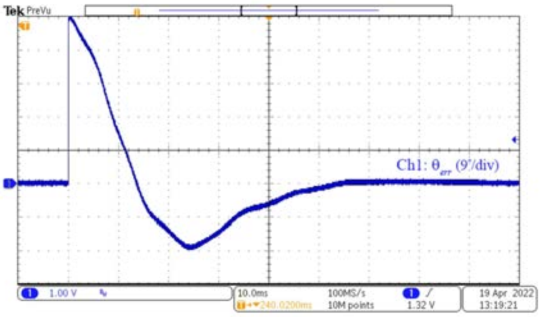
the compensation voltages Δv_α and Δv_β. They fluctuate momentarily, but return to zero in 2 cycles. Fig. 20 shows the simulation results. It should be noted that the phase error and estimated frequency exhibit similar dynamic responses to the experimental results. Once the 45° phase jump occurs, the method can regulate the phase error almost to zero with a settling time of 55 ms, coinciding with the experimental results.

D. Frequency Jump and Frequency Ramp

Fig. 21(a) shows the responses of the phase error under the frequency jump. When the frequency immediately drops from 50 Hz to 47 Hz, the phase error undershoots by nearly 10° and returns to zero in 2 cycles. The estimated frequency quickly drops to 47 Hz in 2

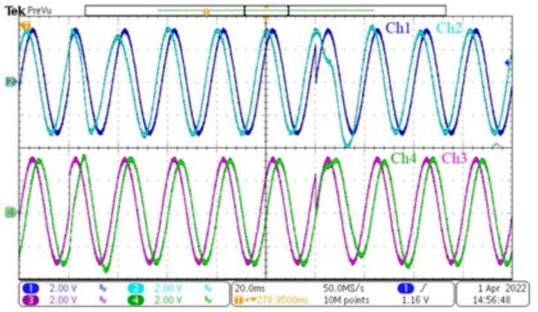


Ch1: Reference phase, θ_i
Ch2: Phase error, θ_{err}
Ch3: Estimated frequency, $\hat{\omega}_i$
(a)

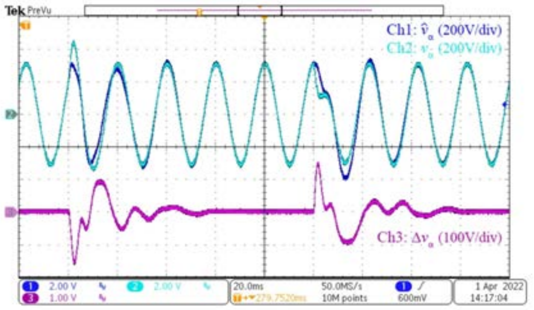


Ch2: Phase error, θ_{err}

(b)

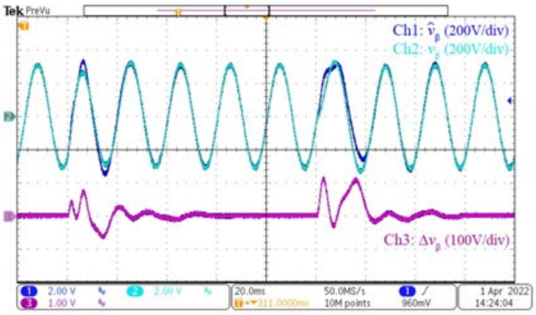


Ch1,Ch3: Grid voltage, v_i (200 V/div)
Ch2: Compensated phase-lead voltage, $\hat{v}_\alpha$ (200 V/div)
Ch4: Compensated phase-lag voltage, $\hat{v}_\beta$ (200 V/div)
(c)



Ch1: Compensated phase-lead voltage, $\hat{v}_\alpha$,
Ch2: Phase-lead voltage, v_α
Ch3: Phase-lead compensation voltage, Δv_α
(d)

Fig. 19: *Experimental results under the 45° phase jump.*



Ch1: Compensated phase-lag voltage, $\hat{v}_\beta$,
Ch2: Phase-lag voltage, v_β
Ch3: Phase-lag compensation voltage, Δv_β
(e)

Fig. 19: *Experimental results under the 45° phase jump (continue).*

cycles. In the following event, a frequency jump of +5 Hz occurs, and the method can regulate the phase error to zero with an overshoot of 16°, tracking the frequency of the grid voltage with an overshoot of 2 Hz in 2 cycles. The frequency then steps down from 52 Hz to the nominal frequency of 50 Hz.

Fig. 21(b)–(c) show the compensated phase-lead voltages $\hat{v}_\alpha$ and the compensated phase-lag voltage $\hat{v}_\beta$ during a frequency jump. Their amplitudes are compensated to the same value as the nominal voltage with phase displacements of 45° with respect to the phase of the grid voltage.

Fig. 21(d) shows the grid voltage, whose frequency linearly decreases from 50 Hz to 47 Hz over a short period of 0.3 s. During a frequency ramp, the proposed method can track the reference frequency with almost zero error. However, during the period in which the frequency variation takes place, a constant phase error of about 0.8° exists. This is because the feedback loop in Fig. 7 is a type II system, which means a constant error exists while it tracks a ramp reference. After the frequency remains constant at 47 Hz, a small magnitude of oscillation takes place on the estimated phase and frequency of 0.1° and 0.2 Hz, respectively.

Fig. 21(e)–(f) show the compensated phase-lead voltages $\hat{v}_\alpha$ and the compensated phase-lag voltage $\hat{v}_\beta$ in the presence of a frequency ramp. The frequency variation compensation successfully corrects their amplitudes and phase displacements as in the case of a frequency jump. It should be noted that the frequency variation compensation acts responsively as soon as the frequency jump or ramp arises.

Fig. 22 shows the simulation results under a series of frequency jumps. It can be observed that the overshoots of the phase error and estimated frequency are slightly less than that obtained from the experiment. Fig. 23 shows the simulation results under frequency variation. While the frequency decreases linearly, the method can track the phase of the grid voltage with a constant error of 0.6°. After the frequency has stabilized at 47 Hz, the phase error and frequency error oscillate at twice the grid frequency with amplitudes of 0.1° and 0.2 Hz peak-peak, respectively, confirming the validity of the experimental results.

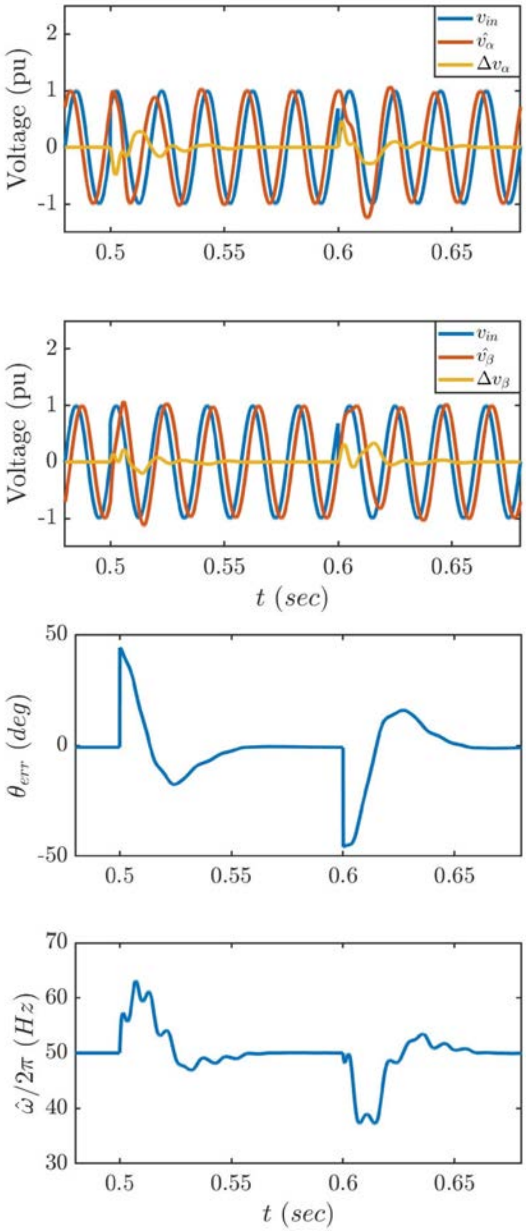
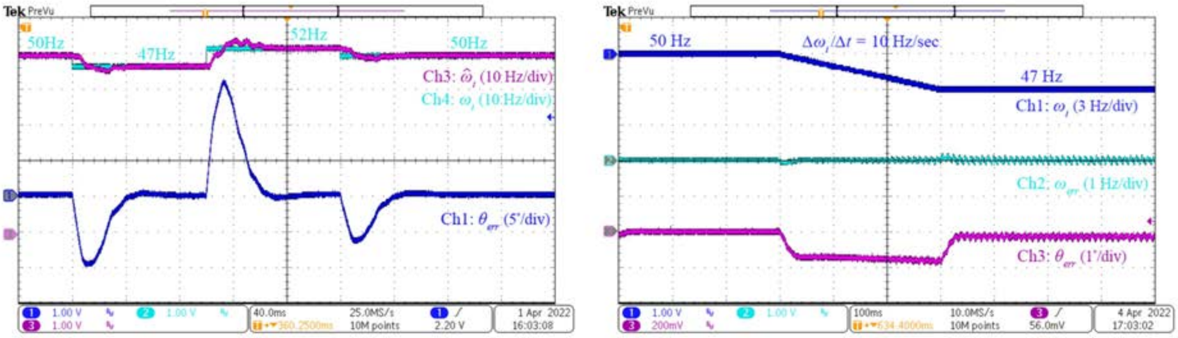


Fig. 20: *Simulation results under the 45° phase jump.*

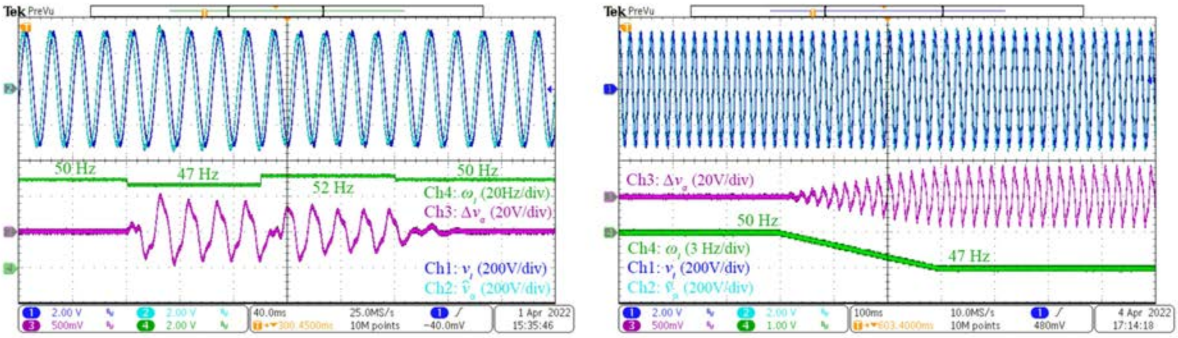
E. DC Offset

Fig. 24(a)–(b) show the compensated phase-lead voltages $\hat{v}_\alpha$ and the compensated phase-lag voltage $\hat{v}_\beta$ while a step DC offset of 10% is added to the grid voltage. The phase-lead and phase-lag tuned filters are capable of filtering the DC offset effectively in 2 cycles. According to Fig. 24(c), at the beginning of perturbation, the estimated frequency varies by about ±2 Hz at a grid frequency of 50 Hz while the phase error fluctuates at an amplitude of 7° peak to peak. After 2 cycles, the estimated frequency remains constant at 50 Hz, and the phase error



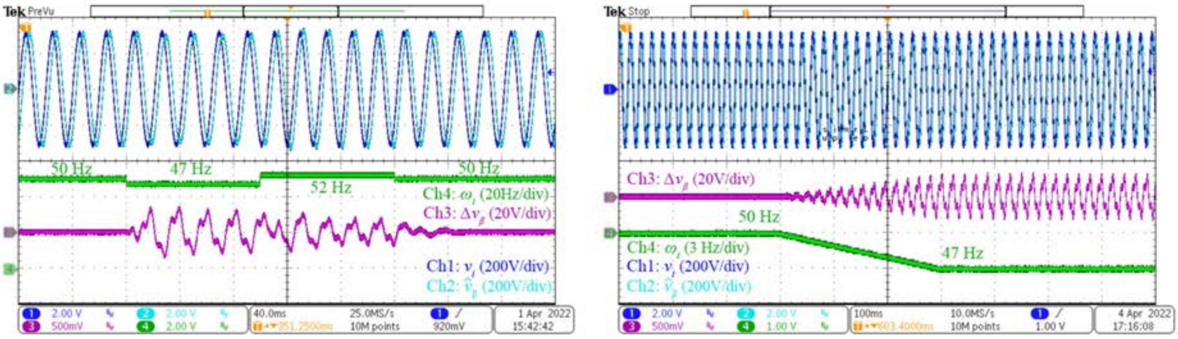
Ch1: Phase error, θ_{err}
Ch2: Reference frequency, ω_i
Ch3: Estimated frequency, $\widehat{\omega}_i$
(a)

Ch1: Reference or input frequency, ω_i
Ch2: Frequency error, ω_{err}
Ch3: Phase error, θ_{err}
(d)



Ch1: Grid voltage, v_i
Ch2: Compensated phase-lead voltage, $\hat{v}_\alpha$,
Ch3: Phase-lead compensation voltage, Δv_α
Ch4: Reference frequency, ω_i
(b)

Ch1: Grid voltage, v_i
Ch2: Compensated phase-lead voltage, $\hat{v}_\alpha$,
Ch3: Phase-lead compensation voltage, Δv_α
Ch4: Reference frequency, ω_i
(e)



Ch1: Grid voltage, v_i
Ch2: Compensated phase-lag voltage, $\hat{v}_\beta$,
Ch3: Phase-lag compensation voltage, Δv_β
Ch4: Reference frequency, ω_i
(c)

Ch1: Grid voltage, v_i
Ch2: Compensated phase-lag voltage, $\hat{v}_\beta$,
Ch3: Phase-lag compensation voltage, Δv_β
Ch4: Reference frequency, ω_i
(f)

Fig. 21: *Experimental results under the frequency jump (a-c) and the frequency ramp (d-f).*

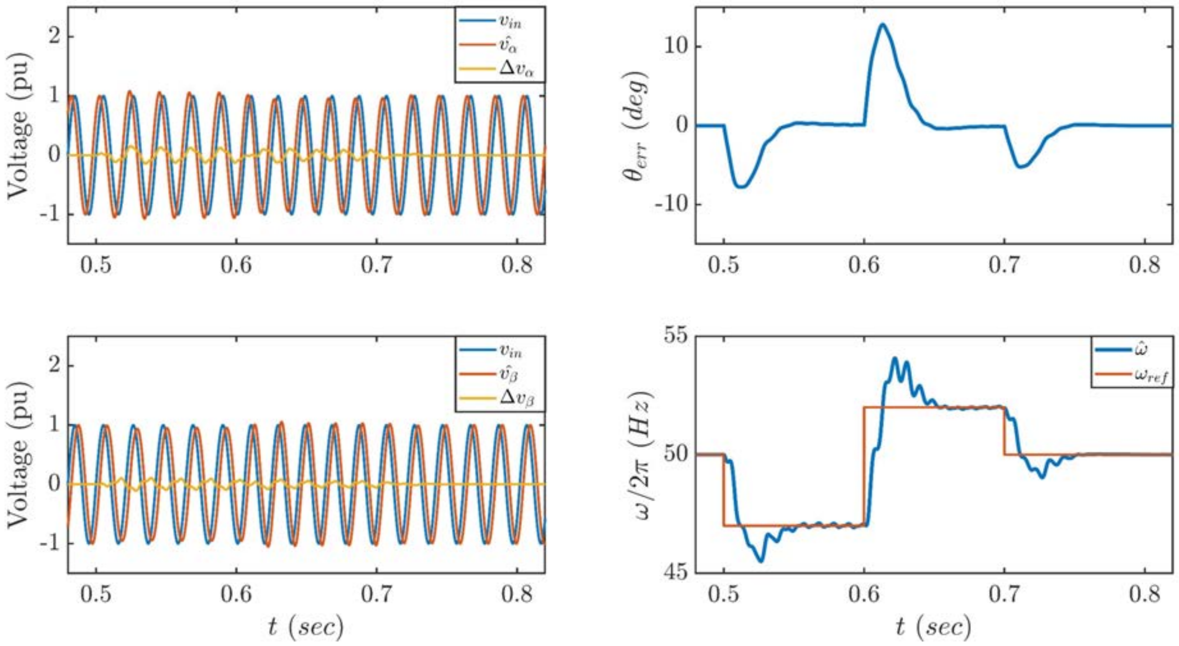


Fig. 22: *Simulation results under the frequency jump.*

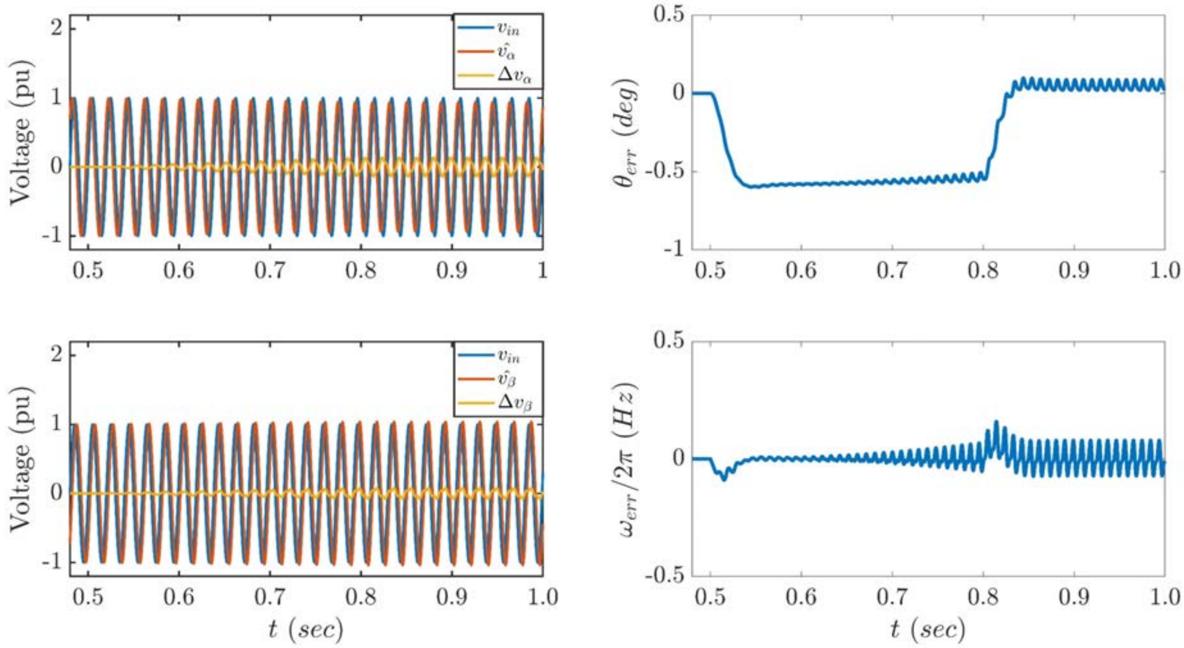
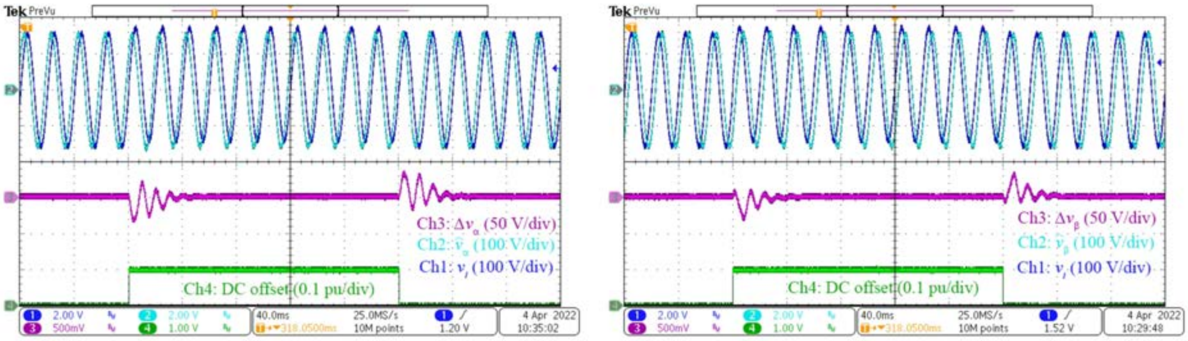


Fig. 23: *Simulation results under the frequency ramp.*

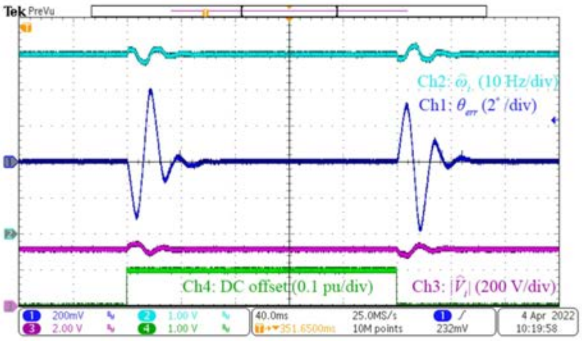


Ch1: Grid voltage, v_i
Ch2: Compensated phase-lead voltage, $\hat{v}_\alpha$,
Ch3: Phase-lead compensation voltage, Δv_α
Ch4: DC offset

(a)

Ch1: Grid voltage, v_i
Ch2: Compensated phase-lag voltage, $\hat{v}_\beta$,
Ch3: Phase-lag compensation voltage, Δv_β
Ch4: DC offset

(b)



Ch1: Phase error, θ_{err}
Ch2: Estimated frequency, $\hat{\omega}_i$
Ch3: Estimated magnitude, $|\hat{V}_i|$
Ch4: DC offset

(c)

***Fig. 24:** Experimental results under the DC offset.*

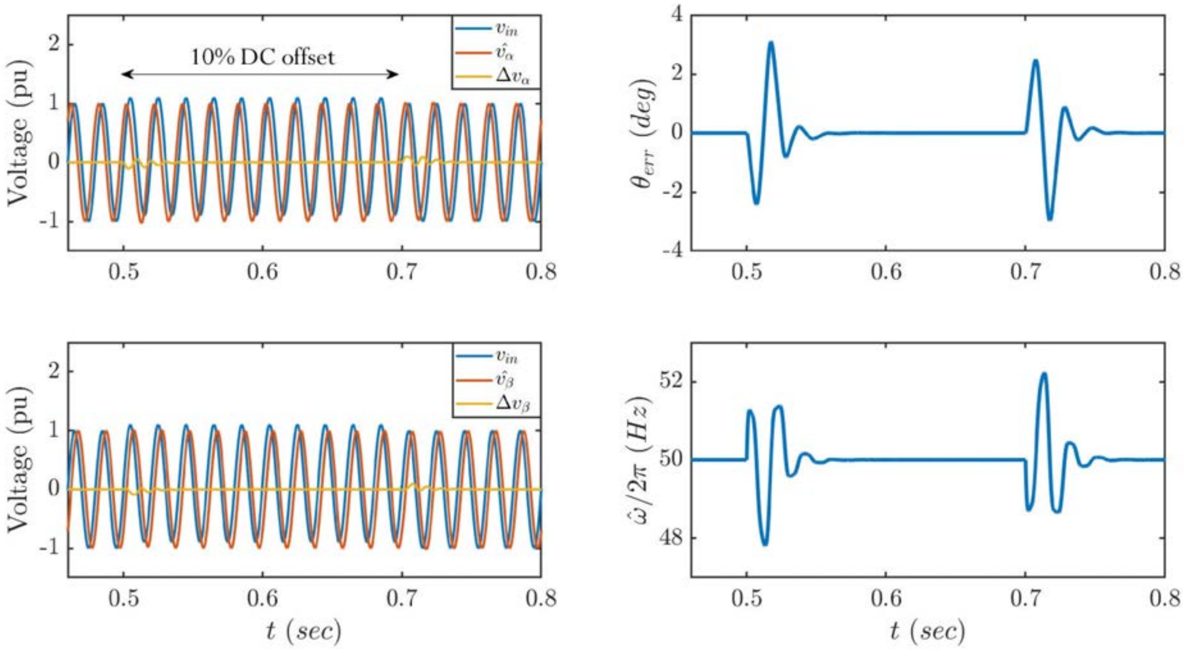
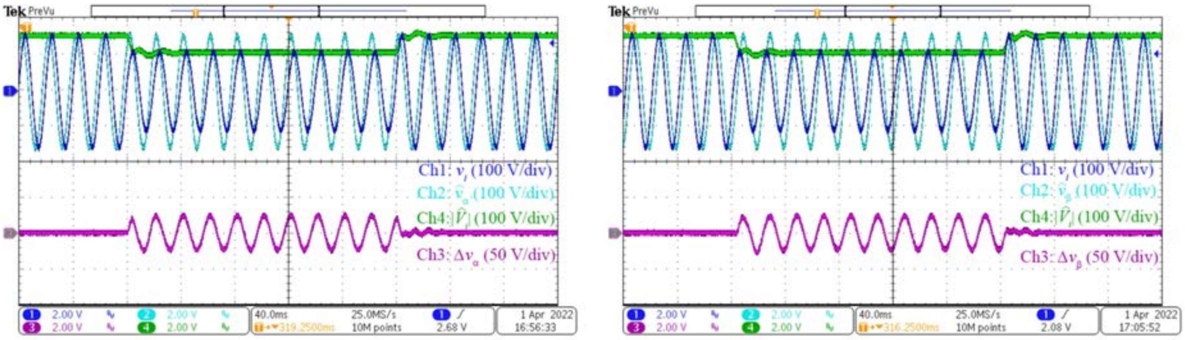
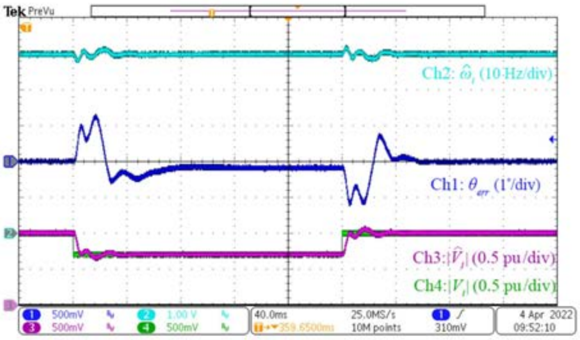


***Fig. 25:** Simulation results under the DC offset.*



Ch1: Grid voltage, v_i
Ch2: Compensated phase-lead voltage, $\hat{v}_\alpha$,
Ch3: Phase-lead compensation voltage, Δv_α
Ch4: Estimated magnitude, $|\hat{V}_i|$
(a)

Ch1: Grid voltage, v_i
Ch2: Compensated phase-lag voltage, $\hat{v}_\beta$,
Ch3: Phase-lag compensation voltage, Δv_β
Ch4: Estimated magnitude, $|\hat{V}_i|$
(b)



Ch1: Phase error, θ_{err}
Ch2: Estimated frequency, $\hat{\omega}_i$
Ch3: Estimated magnitude, $|\hat{V}_i|$
Ch4: Reference magnitude, $|V_i|$
(c)

Fig. 26: *Experimental results under the voltage sag.*

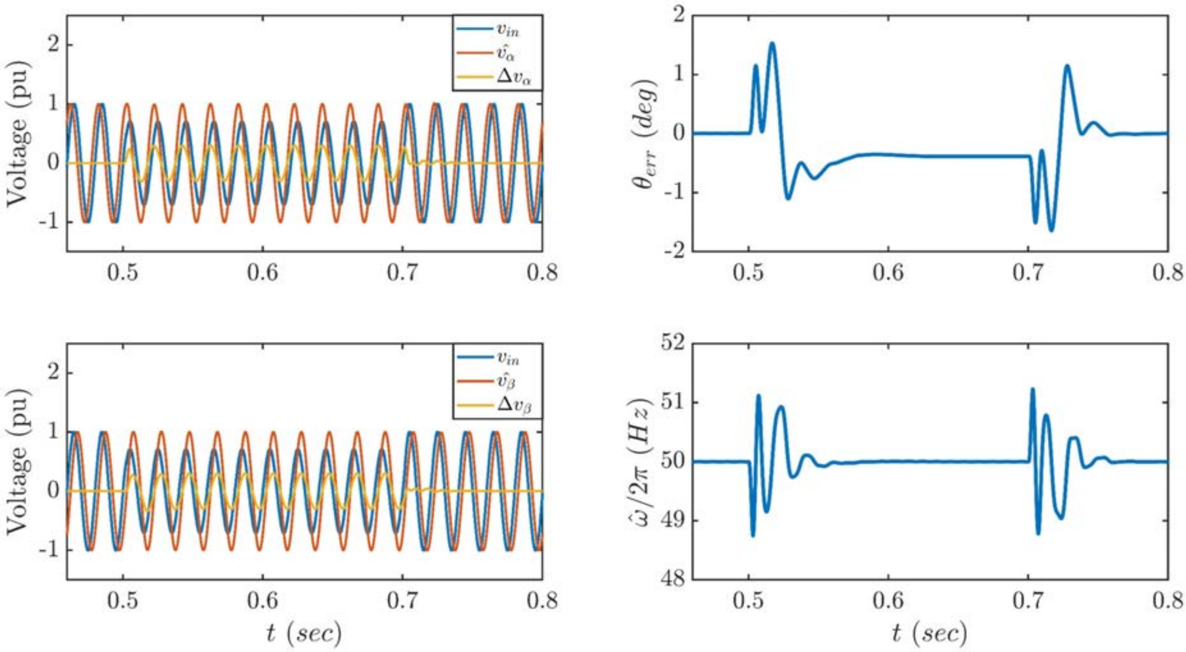
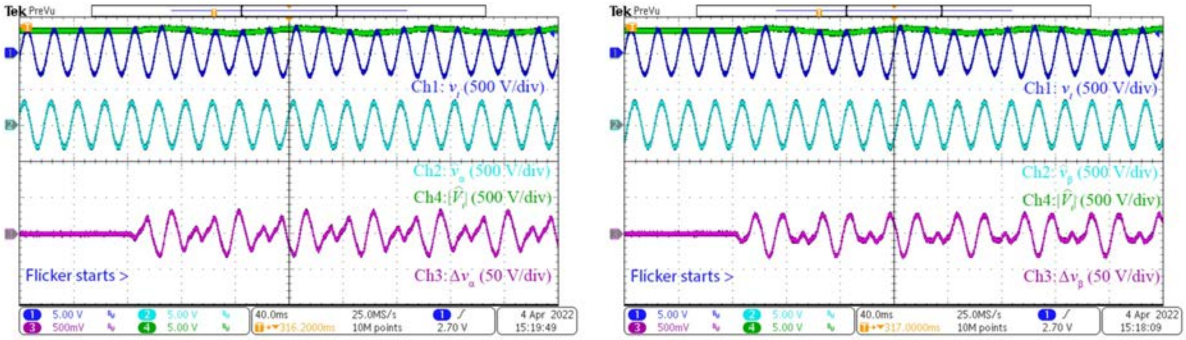


Fig. 27: *Simulation results under the voltage sag.*

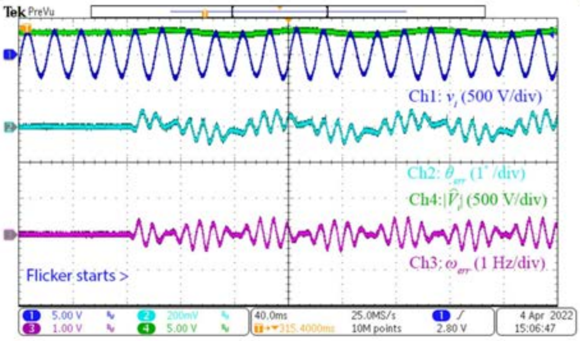


Ch1: Grid voltage, v_i
Ch2: Compensated phase-lead voltage, $\hat{v}_\alpha$,
Ch3: Phase-lead compensation voltage, Δv_α
Ch4: Estimated magnitude, $|\hat{V}_i|$

(a)

Ch1: Grid voltage, v_i
Ch2: Compensated phase-lag voltage, $\hat{v}_\beta$,
Ch3: Phase-lag compensation voltage, Δv_β
Ch4: Estimated magnitude, $|\hat{V}_i|$

(b)



Ch1: Grid voltage, v_i
Ch2: Phase error, θ_{err}
Ch3: Frequency error, ω_{err}
Ch4: Estimated magnitude, $|\hat{V}_i|$

(c)

Fig. 28: *Experimental results under the voltage flicker.*

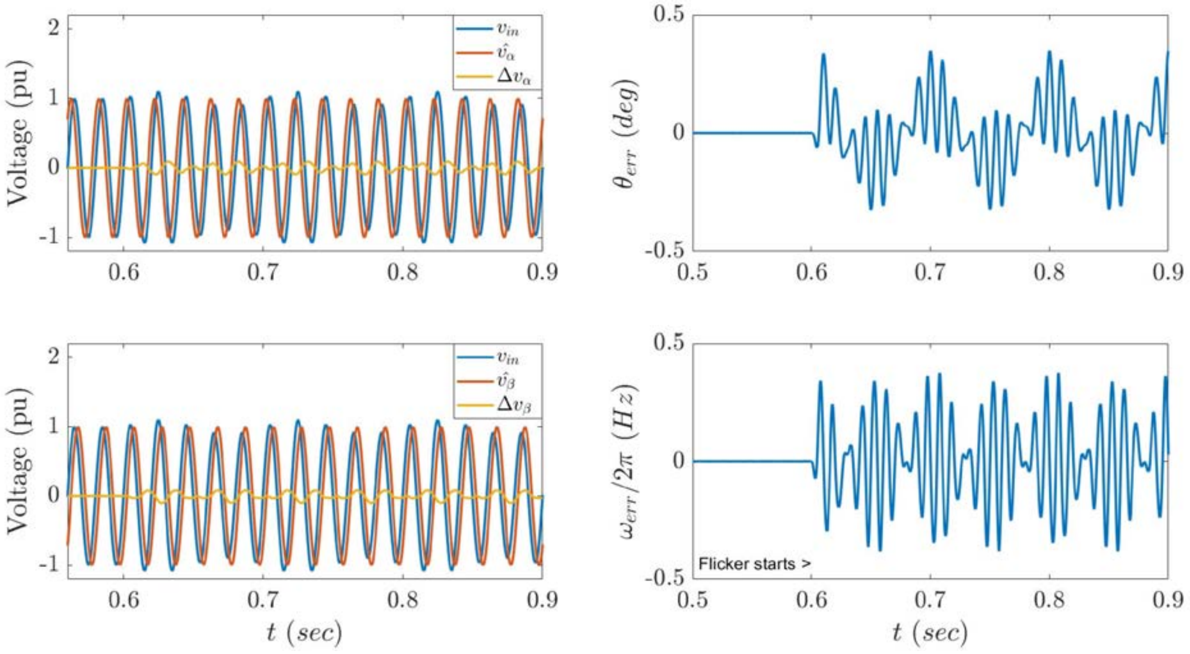


Fig. 29: *Simulation results under the voltage flicker.*

regulated to almost zero. This confirms that the method is robust against a potential DC offset due to quantization errors, roundoff errors, measurement offsets, or temporary grid faults. Fig. 25 shows the simulation results. In the presence of DC offset, the phase error and estimated frequency yield similar dynamic responses to the experimental results.

F. Voltage Sag

Fig. 26(a)–(b) show the compensated phase-lead voltage $\hat{v}_\alpha$ and the compensated phase-lag voltage $\hat{v}_\beta$ during the occurrence of a 70% voltage sag. After compensating, their magnitudes remain at the same value as the nominal grid voltage. In Fig. 26(c), the estimated frequency varies in a narrow range of ±2 Hz and the phase error overshoots slightly by as much as 1.2°. The method can estimate the magnitude and phase of the grid voltage accurately and responds quickly in 2 cycles. Though a steady-state phase error of 0.2° persists during the occurrence of voltage sag, it may result from roundoff errors in the algorithm of the magnitude estimation. Fig. 27 shows the simulation results. Once a step up/down occurs in voltage sag, the phase error and estimated frequency overshoot by nearly 1.5° and 1.2 Hz, respectively. Their dynamic responses are approximately comparable to the results obtained from the experiment.

G. Voltage Flicker

The amplitude of the grid voltage varies sinusoidally in the range of 90–110% at a flickering frequency of 10 Hz. As can be observed from Fig. 28(a)–(b), the method can estimate the magnitude of the grid voltage correctly and generate the compensation voltages Δv_α and Δv_β rapidly at the instant voltage flicker starts. As a result, the magnitudes of the compensated voltages $\hat{v}_\alpha$ and $\hat{v}_\beta$ remain constant at the same level as the nominal grid voltage. According to Fig. 28(c), after the flicker starts, the frequency and phase errors vary within a range of between 0.5 Hz and 0.5°. The results confirm that the method has satisfactory immunity against voltage flicker. Fig. 29 shows the simulation results. After the voltage flicker begins, the phase and frequency errors oscillate at twice the grid frequency. It can be observed that their amplitudes are modulated sinusoidally at a flickering frequency of 10 Hz. Their amplitudes vary by almost 0.5° and 0.5 Hz peak to peak, respectively. The experimental results agree with the simulation results

6. CONCLUSION

The analysis and small signal model of the proposed phase lead-lag synchronous reference frame PLL with frequency variation compensation are discussed in this paper. The design guidelines and an example of the phase-lead and phase-lag tuned filters and the PI controller are detailed. The design example yields a phase margin of nearly 45°, settling time of 2.75 cycles under the 45° step phase jump, and attenuation of -15 dB at twice the nominal frequency. The algorithm is implemented on a rapid prototyping MicroLabBox and programmed in a dSPACE Real-Time Interface for Simulink®. The method is tested under seven different voltage conditions, generated by a programmable AC source. The experimental results are compared with the simulation results and positively validate that the algorithm is robust under many adverse power quality events such as distorted harmonic voltage, phase jump, frequency variation, DC offset, voltage flicker, and voltage sag.

7. APPENDIX

A small signal model is derived as follows:
Let the grid voltage be expressed in a sinusoidal function as,

$$v_i = \left|V_i\right| \cos(\omega_i t + \phi_i)$$

The time-responses of the phase-lead compensated voltage and the phase-lag compensated voltages are expressed as,

$$\begin{aligned}\hat{v}_\alpha(t) &= \left|V_i\right| \left|G_\alpha(j\omega_i)\right| \cos\left(\omega_i t + \phi_i + \angle G_\alpha(j\omega_i)\right) + A_\alpha \cos\left(\omega_{n\alpha}\sqrt{1-\left(\frac{1}{2Q_\alpha}\right)^2}\, t + \varphi_\alpha\right) e^{-t/\tau_\alpha} \\ &+ \left|V_s\right| \cos\left(\hat{\omega}_i t + \phi_i + \frac{\pi}{4}\right) - \left|\hat{V}_i\right| \left|G_\alpha(j\hat{\omega}_i)\right| \cos\left(\hat{\omega}_i t + \phi_i + \angle G_\alpha(j\hat{\omega}_i)\right)\end{aligned}$$

$$\begin{aligned}\hat{v}_\beta(t) &= \left|V_i\right| \left|G_\beta(j\omega_i)\right| \cos\left(\omega_i t + \phi_i + \angle G_\beta(j\omega_i)\right) + A_\beta \sin\left(\omega_{n\beta}\sqrt{1-\left(\frac{1}{2Q_\beta}\right)^2}\, t + \varphi_\beta\right) e^{-t/\tau_\beta} \\ &+ \left|V_s\right| \cos\left(\hat{\omega}_i t + \phi_i - \frac{\pi}{4}\right) - \left|\hat{V}_i\right| \left|G_\beta(j\hat{\omega}_i)\right| \cos\left(\hat{\omega}_i t + \phi_i + \angle G_\beta(j\hat{\omega}_i)\right)\end{aligned}$$

where Δ_α and Δ_β denote the phase-lead compensation voltage and the phase-lag compensation voltage respectively. Applying the Park transformation (31), the quadrature-phase voltage v_q is expressed as,

Term A

$$\begin{aligned}v_q(t) = &-\left|V_s\right| \cos\left(\hat{\omega}_i t + \phi_i + \frac{\pi}{4}\right) \sin\left(\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}\right) \\ &+ \left|V_s\right| \cos\left(\hat{\omega}_i t + \phi_i - \frac{\pi}{4}\right) \cos\left(\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}\right)\end{aligned}$$

Term B

$$\begin{aligned}&+ \left|\hat{V}_i\right| \left|G_\alpha(j\hat{\omega}_i)\right| \cos\left(\hat{\omega}_i t + \phi_i + \angle G_\alpha(j\hat{\omega}_i)\right) \sin\left(\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}\right) \\ &- \left|\hat{V}_i\right| \left|G_\beta(j\hat{\omega}_i)\right| \cos\left(\hat{\omega}_i t + \phi_i + \angle G_\beta(j\hat{\omega}_i)\right) \cos\left(\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}\right)\end{aligned}$$

Term C

$$\begin{aligned}&- \left|V_i\right| \left|G_\alpha(j\omega_i)\right| \cos\left(\omega_i t + \phi_i + \angle G_\alpha(j\omega_i)\right) \sin\left(\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}\right) \\ &+ \left|V_i\right| \left|G_\beta(j\omega_i)\right| \cos\left(\omega_i t + \phi_i + \angle G_\beta(j\omega_i)\right) \sin\left(\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}\right)\end{aligned}$$

Term D

$$\begin{aligned}&- A_\alpha \cos\left(\omega_{n\alpha}\sqrt{1-\left(\frac{1}{2Q_\alpha}\right)^2}\, t + \varphi_\alpha\right) e^{-t/\tau_\alpha} \sin\left(\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}\right) \\ &+ A_\beta \cos\left(\omega_{n\beta}\sqrt{1-\left(\frac{1}{2Q_\beta}\right)^2}\, t + \varphi_\beta\right) e^{-t/\tau_\beta} \sin\left(\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}\right)\end{aligned}$$

Term A can be simplified by

$$\begin{aligned}A = &-\frac{\left|V_s\right|}{2}\left\{\sin\left((\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}) + (\hat{\omega}_i t + \phi_i + \frac{\pi}{4})\right) + \sin\left((\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}) - (\hat{\omega}_i t + \phi_i + \frac{\pi}{4})\right)\right\} \\ &+ \frac{\left|V_s\right|}{2}\left\{\cos\left((\hat{\omega}_i t + \phi_i - \frac{\pi}{4}) + (\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4})\right) + \cos\left((\hat{\omega}_i t + \phi_i - \frac{\pi}{4}) - (\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4})\right)\right\} \\ A = &-\frac{\left|V_s\right|}{2}\left\{\sin\left(2\hat{\omega}_i t + \phi_i + \hat{\phi}_i + \frac{\pi}{2}\right) + \sin\left(\hat{\phi}_i - \phi_i\right)\right\} + \frac{\left|V_s\right|}{2}\left\{\cos\left(2\hat{\omega}_i t + \phi_i + \hat{\phi}_i\right) + \cos\left(\phi_i - \hat{\phi}_i - \frac{\pi}{2}\right)\right\} \\ A = &\left|V_s\right| \sin\left(\phi_i - \hat{\phi}_i\right)\end{aligned}$$

Term B can be simplified by

$$\begin{aligned}
B = {} & \frac{\left|\hat{V}_i\right| \left|G_\alpha(j\hat{\omega}_i)\right|}{2} \left\{ \sin\left((\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}) + (\hat{\omega}_i t + \phi_i + \angle G_\alpha(j\hat{\omega}_i)) \right) \right. \\
& \left. + \sin\left((\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}) - (\hat{\omega}_i t + \phi_i + \angle G_\alpha(j\hat{\omega}_i)) \right) \right\} \\
& - \frac{\left|\hat{V}_i\right| \left|G_\beta(j\hat{\omega}_i)\right|}{2} \left\{ \cos\left((\hat{\omega}_i t + \phi_i + \angle G_\alpha(j\hat{\omega}_i)) + (\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}) \right) \right. \\
& \left. + \cos\left((\hat{\omega}_i t + \phi_i + \angle G_\beta(j\hat{\omega}_i)) - (\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}) \right) \right\} \\
B = {} & \frac{\left|\hat{V}_i\right| \left|G_\alpha(j\hat{\omega}_i)\right|}{2} \left\{ \sin\left(2\hat{\omega}_i t + \phi_i + \hat{\phi}_i + \angle G_\alpha(j\hat{\omega}_i) + \frac{\pi}{4}) \right) + \sin\left(\hat{\phi}_i - \phi_i - \angle G_\alpha(j\hat{\omega}_i) + \frac{\pi}{4} \right) \right\} \\
& - \frac{\left|\hat{V}_i\right| \left|G_\beta(j\hat{\omega}_i)\right|}{2} \left\{ \cos\left(2\hat{\omega}_i t + \phi_i + \hat{\phi}_i + \angle G_\beta(j\hat{\omega}_i) + \frac{\pi}{4}) \right) + \cos\left(\phi_i - \hat{\phi}_i + \angle G_\beta(j\hat{\omega}_i) - \frac{\pi}{4} \right) \right\}
\end{aligned}$$

Term C can be simplified by

$$\begin{aligned}
C = {} & -\frac{\left|V_i\right| \left|G_\alpha(j\omega_i)\right|}{2} \left\{ \sin\left((\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}) + (\omega_i t + \phi_i + \angle G_\alpha(j\omega_i)) \right) \right. \\
& \left. + \sin\left((\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}) - (\omega_i t + \phi_i + \angle G_\alpha(j\omega_i)) \right) \right\} \\
& + \frac{\left|V_i\right| \left|G_\beta(j\omega_i)\right|}{2} \left\{ \cos\left((\omega_i t + \phi_i + \angle G_\alpha(j\omega_i)) + (\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}) \right) \right. \\
& \left. + \cos\left((\omega_i t + \phi_i + \angle G_\beta(j\omega_i)) - (\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4}) \right) \right\} \\
C = {} & -\frac{\left|V_i\right| \left|G_\alpha(j\omega_i)\right|}{2} \left\{ \sin\left((\hat{\omega}_i + \omega_i)t + \phi_i + \hat{\phi}_i + \angle G_\alpha(j\omega_i) + \frac{\pi}{4}) \right) + \sin\left((\hat{\omega}_i - \omega_i)t + \hat{\phi}_i - \phi_i - \angle G_\alpha(j\omega_i) + \frac{\pi}{4} \right) \right\} \\
& + \frac{\left|V_i\right| \left|G_\beta(j\omega_i)\right|}{2} \left\{ \cos\left((\hat{\omega}_i + \omega_i)t + \phi_i + \hat{\phi}_i + \angle G_\beta(j\omega_i) + \frac{\pi}{4}) \right) + \cos\left((\omega_i - \hat{\omega}_i)t + \phi_i - \hat{\phi}_i + \angle G_\beta(j\omega_i) - \frac{\pi}{4} \right) \right\}
\end{aligned} \tag{64}$$

Under a quasi-frequency locked state, it is assumed that

$$\begin{aligned}
\left|V_s\right| &\approx \left|\hat{V}_i\right| \\
\omega_i &\approx \hat{\omega}_i
\end{aligned}$$

Applying Taylor's series approximation as follows:

$$\begin{aligned}
\sin(\phi_i - \hat{\phi}_i) &\approx \phi_i - \hat{\phi} \\
\cos(\phi_i - \hat{\phi}) &\approx 1
\end{aligned}$$

The sum of terms B and C approximately equals zero. Excluding the exponential terms, the quadrature-phase voltage v_q is linearized and expressed as,

$$\begin{aligned}
v_q(t) = \left|V_s\right| & (\sin(\phi_i - \hat{\phi}) - e^{-t/\tau_\alpha} \left(A_\alpha \cos\left(\omega_{n\alpha} \sqrt{1 - \left(\frac{1}{2Q_\alpha}\right)^2} t + \varphi_\alpha \right) \sin\left(\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4} \right) \right) \\
& + e^{-t/\tau_\beta} \left(A_\beta \sin\left(\omega_{n\beta} \sqrt{1 - \left(\frac{1}{2Q_\beta}\right)^2} t + \varphi_\beta \right) \cos\left(\hat{\omega}_i t + \hat{\phi}_i + \frac{\pi}{4} \right) \right)
\end{aligned}$$

REFERENCES

[1] C. jeraputra, J. Pongpaiboon, T.Singhavilai, and S. Tiptipakorn, “A Phase Lead-Lag Synchronous Reference Frame PLL for Grid Synchronization of a Single-Phase Inverter,” *ECTI Transactions on Electrical Engineering, Electronics, and Communication*, vol. 20, no. 1, pp. 123–132, Feb. 2022.

[2] *Voltage Characteristics of Electricity Supplied by Public Distribution Systems*, Eur. Std. EN 50160, 2008.

[3] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, “Dynamics Assessment of Advanced Single-Phase PLL Structures,” *IEEE Transactions on Industrial Electronics*, vol. 60, no. 6, pp. 2167-2177, Jun. 2013.

[4] S. Preitl and R.-E. Precup, “On the Algorithmic Design of a Class of Control Systems based on Providing the Symmetry of Open-Loop Bode Plots,” *Buletinul Stiintific al U.P.T., Trans. Automatic. Control Computer. Science.*, vol. 41(55), no. 1/2, pp. 47–55, Dec. 1996.

[5] K. Shu and E. Sanchez-Sinencio, *CMOS PLL Synthesizers—Analysis and Design.* New York, USA: Springer-Verlag, 2005.