A Symmetrical Cross-Connected T-Type Multilevel Inverter With Reduce Device Count

Vishal Rathore[1†], **Dhananjay Kumar**[2], and **Prateek Mundra**[3], Non-members

ABSTRACT

This paper presents a symmetrical, cross-connected T-type (CT-type) multilevel inverter (MLI) configuration with reduced device count (RDC). It comprises eight power switches, two DC sources, and four capacitors with self-voltage balancing. The generalized topology is formed by two CT-type basic modules connected by two power switches. These topologies operate using DC sources and capacitors having the same or different voltage levels, which can be extended by cascading the modules to attain a higher voltage level suitable for high-power applications. Therefore, the proposed CT-Type MLI is a good choice for renewable energy applications that require a lower input voltage source magnitude to attain high voltage levels. This paper uses the Matlab/Simulink platform to simulate the proposed CT-type topology using the level-shifted pulse width modulation (LS-PWM) technique. Further, a laboratory prototype is developed to test and validate the feasibility and effectiveness of the proposed MLI. Finally, a comparative analysis of the number of DC sources, capacitors, power switches, drivers, and total standing voltage (TSV) is presented against similar recent topologies.

Keywords: Multilevel Inverter, Total Harmonic Distortion, Pulse Width Modulation, Reduced Device Count, CT-type, Total Standing Voltage

1. INTRODUCTION

Multilevel inverters (MLIs) have played a significant role in various applications for medium and high voltage/power ratings. Applications of MLIs in large areas are dominated by power electronics devices like electric vehicles, wind turbines, active power filters, grid-connected PV systems, induction motor control, etc., because of their ability to synthesize high-voltage outputs [1–5]. It can generate various output voltage levels by incorporating multiple capacitors, power semiconductor switches, DC supplies, and diodes. Technically, MLIs are sound in delivering high efficiency, modularity, low THD, high voltage levels, etc. MLIs are broadly classified into three types: flying capacitors (FC), cascaded H-bridges (CHB), and neutral point capacitors (NPC). Cascaded H-bridge (CHB) has gained more interest among researchers among these technologies as it overcomes the drawbacks of the other two, i.e., high switching losses, unbalanced DC voltage, and the use of more capacitors. Some recently developed and traditional MLI topologies presented in [6, 7] have been briefly reviewed for this work.

Multiple DC source-based CHBs are more appealing than single DC MLIs because of their higher reliability and modularity. Moreover, symmetric CHB has less complex control than asymmetric configurations, significantly increasing voltage levels with a reduced device count [8, 9]. On the other hand, the count of isolated DC voltage sources required in CHB is significantly higher. Previously, MLIs were limited by needing more DC sources and semiconductor switches. Over the last few years, extensive research has been conducted on improving MLI configuration in every feasible way. In [10–11], MLIs with switched-DC, switched-diode, and switched-capacitor configurations have been proposed. In [12], an asymmetric switched-DCMLI having fewer components than traditional circuitry has been presented. The proposed topologies in [13] and [14] are cost-effective and perform better with a switched DC source. Even with a reduced device count, these configurations can provide both negative and positive voltage polarity. Besides that, significantly higher voltage levels can be obtained by connecting multiple fundamental units in series. In the presence of an integrated H-bridge, optimized structures in [15, 16] revealed that 15 levels could be generated using 16 interrupter numbers and 7 DC sources in the basic unit. Voltage levels using different DC sources can be generated by having lower switching stress by modifying the sources. [17, 18] presented and validated the symmetrical and asymmetrical topologies using various pulse width modulation (PWM) techniques. [19–21] investigated switched DC-based topologies that can replace traditional MLIs. Two switches connected by a DC link to generate the required voltage level are proposed in [22]. A negative voltage level was created by incorporating an H-bridge into the initial design. This MLI modification was improved in [23], which added two capacitors to get more levels out of each module.

Conventional MLIs can be combined to produce

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[1]The authors is with Department of Electrical Engineering, BITS Bhopal, M.P, India-462045,

[2]The author is with Department of Industrial Research Design and Development, Aartech Solonics Ltd. Mandideep, M.P, India-462046,

[3]The author is with Department of Electrical Engineering, GHRCEM, Pune, India-412207,

[†]Corresponding author: vishalrathore01@gmail.com

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multiple voltage levels in a hybrid form. Some hybrid topologies proposed in [24, 25] are classified as symmetrical MLIs. Because of the unequal DC input voltage, symmetric MLIs generate high voltage levels with a reduced device count (RDC). An unconventional asymmetrical topology is presented in [26] by utilizing power switches to demonstrate higher voltage levels, reducing stress on semiconductor switches. Also, a modified H-bridge topology proposed in [27, 28] has unequal voltage DC supplies. Therefore, different bridges in symmetrical MLIs operate at different voltages.

Consequently, switches associated with the high-voltage bridge must be capable of withstanding high voltage. However, the primary design objective of MLIs may be compromised because this method uses low-rating switches for high-power applications, even though it can significantly increase voltage levels. This disadvantage affects asymmetrical MLIs that use the voltage balancing method. Furthermore, the asymmetrical MLIs proposed in [29, 30] are composed of self-balancing bridges with equal DC-link voltages and are primarily designed in a symmetrical configuration. So, no self-balancing circuit is required, making inverter control simpler.

The proposed MLI is intended to increase the output voltage level while ensuring the smart setup of semiconductor switches. The economical design also ensures that the number of power devices is minimal. This paper introduces symmetrical CT-type MLI configurations. In a symmetrical configuration, there are two DC voltage supplies and four capacitors of the same rating, allowing it to produce four negatives, four positives, and one zero for nine different voltage levels. The proposed topology comprises CT-type modules so that negative voltage levels can be generated without the additional support of an H-bridge. Only 2 DC sources, 4 capacitors, and 8 switches were used.

This paper has the following structure: Section 2 discusses the circuit and the workings of the proposed CT-Type MLI. In addition, this section also provides symmetric configuration and modes of operation, as well as module extension with output voltage level generation. Section 3 presents the modulation and control techniques, followed by the simulation results for the proposed CT-Type MLI. Hardware implementation and the experimental results are presented in Section 4. The proposed MLI's power loss and efficiency are discussed thoroughly in Section 5, followed by a detailed comparative analysis of the recent topologies with the proposed CT-Type topology presented in Section 6. Finally, Section 7 contains the conclusion of the paper.

2. PROPOSED BASIC TOPOLOGY

2.1 Circuit configuration and its operation

Fig. 1 illustrates a schematic diagram of a basic CT-type multilevel inverter. It consists of 1 DC source, 2 capacitors, 2 unidirectional switches, and 1 bidirectional switch. The DC supply's bidirectional switches prevent short-circuit currents by facilitating blockage of both

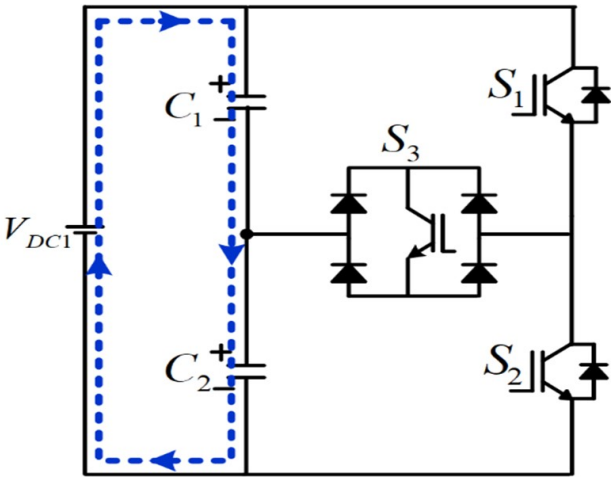


***Fig. 1**: Basic cell of single-phase CT-type multilevel inverter.*

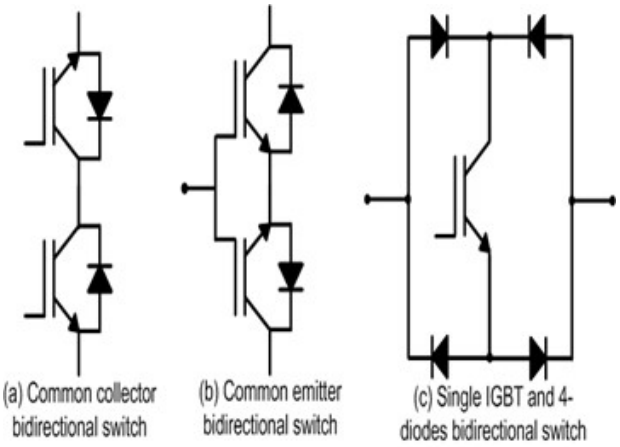


***Fig. 2**: Various arrangements for bidirectional switches.*

current polarities. Moreover, the proposed CT-Type topology inherently achieves self-voltage balance in DC-link capacitors. This module has generated the three-level output voltage. Various arrangements for bidirectional switches have been shown in Fig. 2.

Fig. 3 illustrates the generalized structure of the proposed single-phase CT-Type MLI module. The two basic modules are connected, L and R, with two power switches. Unidirectional switches S1 and S2 are connected between the L and R modules and vice versa. The load is connected between both modules (L and R). This arrangement can produce multiple voltage levels despite having a reduced power device count. Higher voltage levels are expected to have significantly lower total harmonic distortion (THD) and a lower switching frequency.

2.2 Determination of Capacitance

The capacitor starts charging when connected in series with the load and discharges when connected in parallel across the voltage source [7]. The capacitor's charging-discharging behavior in the proposed CT-type

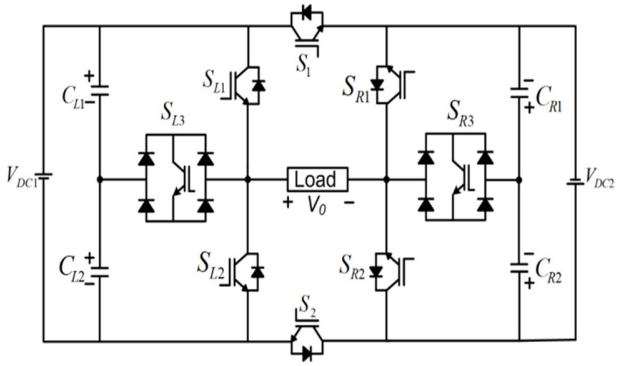


***Fig. 3**: Generalized single-phase CT-Type MLI module.*

MLI significantly impacts output voltage levels. Therefore, it is critical to identify the appropriate value of the capacitor, and the operating frequency and the load current determine the capacitance value. The capacitor's largest voltage ripple occurs during the discharging phase, as described in [1].

Consequently, the capacitance value is calculated using the worst case of the capacitor's discharge duration. The voltage ripple must be within a specific range to be considered acceptable. When the ripple voltage is kept to a minimum, it reduces losses, thereby improving the efficiency of the proposed topology. In Fig. 3, it can be seen that the DC input voltage source is connected in series with both capacitors. As a result, the identical current flows through them during charging so that the same charge accumulates on them. Therefore,

$$I_{C1} = I_{C2} \quad \Rightarrow Q_{C1} = Q_{C2} \quad \Rightarrow C_1.V_{C1} = C_2 V_{C2} \tag{1}$$

When identical capacitance values are used, Eq.(1) achieves

$$\begin{cases} C_1 V_{C1} = C_2 V_{C2} \\ V_{C1} = V_{C2} \end{cases} \quad \Rightarrow \quad C_1 = C_2 \tag{2}$$

As a result, Eq. (2) provides identical values for the capacitances C_1 and C_2 , i.e., $C_1 = C_2$. Two significant factors must be considered when calculating an appropriate capacitance value: (*i*) the amplitude of the load current and its phase difference with the load voltage; and (*ii*) the time of the capacitors' discharging while keeping voltage ripples in an acceptable range.

Each capacitor's maximum charge drawn is as follows:

$$\Delta Q_C = \int_{t_S}^{t_f} I_{Load} \sin\left(2\pi f_0 t\right) dt \tag{3}$$

where I_{Load} and f_0 indicate the load current amplitude and fundamental output frequency, respectively, in this equation.

Furthermore, the period is the biggest discharging interval for each capacitor, demonstrating the worst possible state. Finally, it should be noticed that the capacitance values of capacitors C_1 and C_2 are identical, and the equivalent capacitance of the circuit (C_{eq}) while supplying the load is given by:

$$C_{eq}. \geq \frac{\Delta Q_C}{K.V_{eq}} \tag{4}$$

where K is the maximum permissible voltage ripple, the exact value of both capacitors can be calculated using the same values of C_{eq} and equations mentioned above.

From the preceding equations, the amplitude of the load current is critical in determining the optimal value of capacitors C_1 and C_2. In this scenario, both capacitors are just in steady-state operation, and the load is supposed to be a purely resistive load, so the output current is given by the equation below:

$$I_L(t) = \begin{Bmatrix} \frac{V_{dc}}{R_L} & for \quad t_1 \leq t \leq t_2 \\ \frac{2V_{dc}}{R_L} & for \quad t_2 \leq t \leq t_3 \\ \frac{3V_{dc}}{R_L} & for \quad t_3 \leq t \leq \frac{T}{4} \end{Bmatrix} \tag{5}$$

However, if the load is supposed to be a resistive-inductive (R-L) load, the amplitude of the load current is given as:

$$I_L(t) = I_{\max} \sin\left(\omega t - \alpha\right) dt \tag{6}$$

The optimum value of capacitors in the proposed CT-type topology can be obtained by solving Eqs. (3)–(6). The appropriate capacitor ranges under RL and pure resistive loads are obtained from Eq. (7).

$$C_1 = C_2 \geq \frac{2\int_{t_3}^{T_{/4}} I_L(t)dt}{K.V_{eq}} \tag{7}$$

The circuit parameters of the proposed CT-type topology are $R = 20\Omega$ & 40Ω, $L = 20$mH & 40mH, $k = 0.05$, $f_{ref} = 50$Hz, and the series connection of both capacitors' value of equivalent capacitance is $C_1 = C_2 \geq 1780\mu F$.

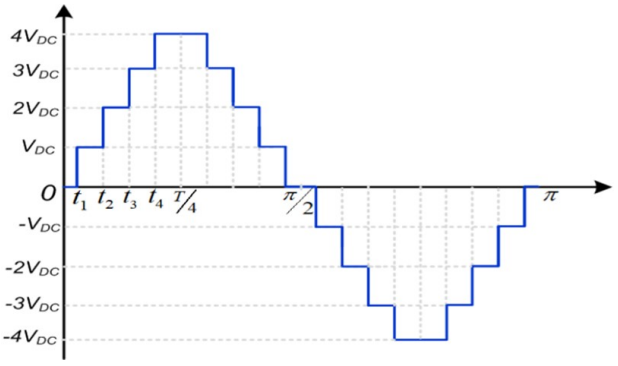
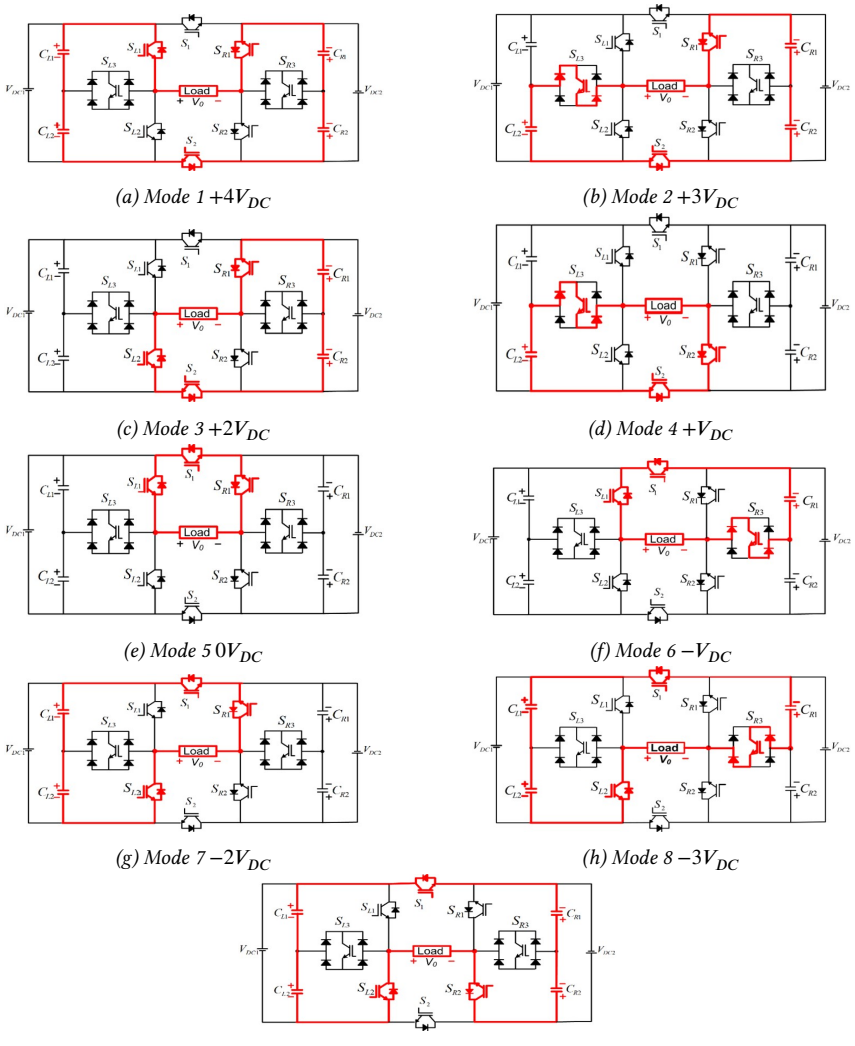


***Fig. 4**: 9-level voltage waveform of the proposed symmetrical CT-Type topology .*

***Table 1**: Switching modes for the proposed symmetric configuration.*

S_{L1}	1	0	0	0	1	1	0	0	0
S_{L2}	0	0	1	0	0	0	1	1	1
S_{L3}	0	1	0	1	0	0	0	0	0
S_1	0	0	0	0	1	1	1	1	1
S_2	1	1	1	1	0	0	0	0	0
S_{R1}	1	1	1	0	1	0	1	0	0
S_{R2}	0	0	0	1	0	0	0	0	1
S_{R3}	0	0	0	0	0	1	0	1	0
O/P voltage	+4E	+3E	+2E	+E	0	-E	-2E	-3E	-4E
C_{L1}	Dis charge	-	-	-	-	-	Charge	Charge	Charge
C_{L2}	Discharge	Discharge	-	Discharge	-	-	Charge	Charge	Charge
C_{R1}	Discharge	Discharge	Discharge	-	-	Charge	-	Charge	Charge
C_{R2}	Discharge	Discharge	Discharge	-	-	-	-	-	Charge



(a) Mode 1 $+4V_{DC}$ *(b) Mode 2 $+3V_{DC}$*

(c) Mode 3 $+2V_{DC}$ *(d) Mode 4 $+V_{DC}$*

(e) Mode 5 $0V_{DC}$ *(f) Mode 6 $-V_{DC}$*

(g) Mode 7 $-2V_{DC}$ *(h) Mode 8 $-3V_{DC}$*

(i) Mode 9 $-4V_{DC}$

***Fig. 5**: Switching mode and active current paths.*

It implies that we must pick at least two identical capacitors $1780\mu F$ for the inverter with the aforementioned parameters, load, and 5% capacitor voltage tolerance (ripple). So, the nearest commonly available capacitance value $2200\mu F$ is chosen for both model and experimental validation in Sections 3 and 4.

2.3 Generalized Symmetric CT-Type MLI structure

The proposed CT-type MLI includes eight switches, four capacitors, and two DC supplies with the same magnitudes of DC sources for symmetric operation. This can create a nine-step output voltage. The topology's primary premise is to provide diverse pathways for current from various DC sources. The DC sources of both modules (L and R) are connected in this manner, resulting in negative voltage levels having no support from any H-bridge circuit. Fig. 4 illustrates the 9-level voltage waveform of the proposed symmetrical CT-Type topology.

Switching modes for symmetric configuration are presented in Table 1. Fig. 5 shows switching modes and active current paths (red line) for a symmetrical configuration. The adjacent semiconductor switches ($S_{L1}, S_{L2}, S_{R1}, S_{R2}$), and the power switches (S_1 and S_2), are unidirectional. Both modules include bidirectional switches (SL3 and SR3) in the center. As previously stated, DC sources (V_{DC1} and V_{DC2}) have the same magnitude in symmetric operation ($V_{C1L} = V_{C2L} = V_{C1R} = V_{C2R} = E/2$).

The switching configuration of CT-type MLI has been set so that the positive poles of DC sources are not linked to the anode side of diodes to enhance current conduction. The CT-type MLI also uses the same switching components for each voltage level. As a result, the proposed configuration is self-balancing.

The switching process clearly shows that switch pairs (S_{L1}, S_{L2}), (S_1, S_2), and ($S_{R1}, S_{R2)}$ can never be turned on at the same time. Therefore, the proposed topology has to switch redundancy at the same voltage levels, which improves reliability.

2.4 Voltage stress calculations

Table 1 shows the proposed topology's total standing voltage (TSV) calculation. The maximum voltage standing capacity of switches is determined in the off state, and the sum of these voltages is used to calculate the TSV of the proposed topology. TSV is calculated using the standing voltage across S1 as an example. VBB = −3E or VBB = −4E is used to compute S1's maximum voltage standing capability. S1 is switched off in both states, and DC sources in module L deliver a standing voltage to S1. This calculation can be expressed as follows:

$V_{S1} = E + E = 2E, V_{S2} = E + E = 2E$

$V_{S5} = E + E + E = 4E, V_{S4} = E + E = 2E$

$V_{S6} = E + E + E = 4E, V_{S7} = E$, and $V_{S8} = E$

$TSV = V_{S1} + V_{S2} + V_{S3} + V_{S4} + V_{S5} + V_{S6} + V_{S7} + V_{S8} = 18E$.

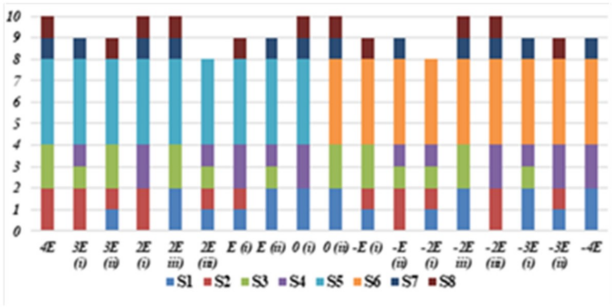


***Fig. 6**: TSV of switches in a symmetrical configuration.*

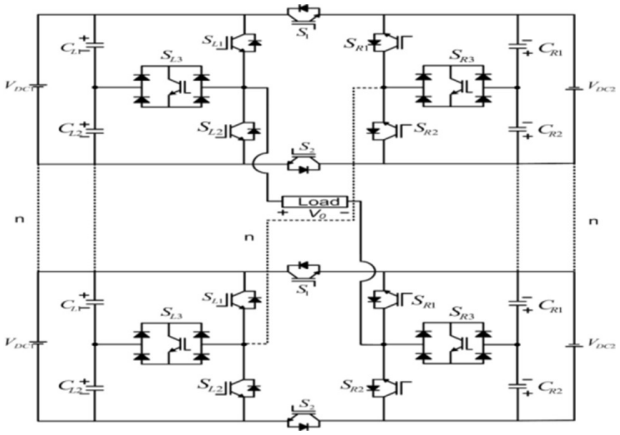


***Fig. 7**: Extension of proposed CT-type topology for N_{level}.*

The TSV calculation clearly shows that particular groups of switches have the same amount of standing voltage but at numerous levels. The TSV of switches in the symmetric configuration is illustrated in Fig. 6.

2.5 Module Extension

With some changes, the proposed CT-type module could potentially produce a higher output voltage. Consequently, CT-type modules are excellent for applications requiring high output voltage levels, like PV grid-connected systems. Therefore, the proposed CT-type topology can be extended for higher voltage levels. For example, the extension of the proposed CT-type topology for the N-level is shown in Fig. 7.

Depending on the application, the modifications might be done in a symmetric arrangement. After modification, the topology can produce 17 levels, as tabulated in Table 2.

3. SIMULATION STUDY

3.1 Modulation and Control Method of MLI

Various modulation techniques are used for MLIs, including high switching frequency techniques (i.e., multi-carrier pulse width modulation and space-vector pulse width modulation) and low switching frequency techniques (i.e., active harmonic elimination, selective harmonic elimination, and nearest level control). With appropriate modification, the proposed CT-type topology

***Table 2**: Switching modes for the proposed symmetric configuration.*

Unit 2 \ Unit 1	4	3	2	1	0	-1	-2	-3	-4
4	8	7	6	5	4	3	2	1	0
3	7	6	5	4	3	2	1	0	-1
2	6	5	4	3	2	1	0	-1	-2
1	5	4	3	2	1	0	-1	-2	-3
0	4	3	2	1	0	-1	-2	-3	-4
-1	3	2	1	0	-1	-2	-3	-4	-5
-2	2	1	0	-1	-2	-3	-4	-5	-6
-3	1	0	-1	-2	-3	-4	-5	-6	-7
-4	0	-1	-2	-3	-4	-5	-6	-7	-8

***Table 3**: Simulation Parameters.*

Parameters	Ratings
Rated DC voltage	$V_{DC1} = 24\text{V} \& V_{DC2} = 24\text{V}$
Capacitors	$C_1 C_2 = 2200\mu\text{F}$
Modulation index	$m_a = 0.85$
Load value	$R = 20\Omega, L = 20\text{mH}$
Modulating wave frequency	$f_m = 50\text{Hz}$
Switching frequency	$f_s = 3150\text{Hz}$

can be modified using any of these techniques. The level-shift pulse width modulation is adopted in this work. The triangular carrier signals are being compared to the sinusoidal reference signal in the LS-PWM technique. Gate pulses are generated for switching devices at various voltage levels. The peak value of the waveform is V_{ref}, peak and modulation index (MI) will be obtained using Eq. (8).

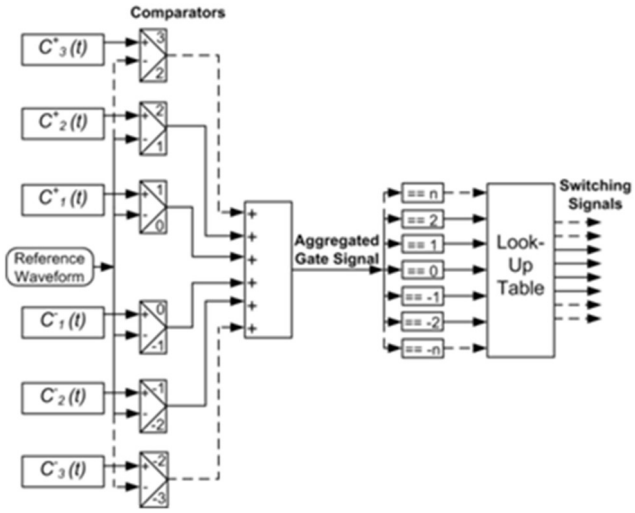
$$MI = \frac{V_{ref.peak}}{5V_{car}} \tag{8}$$

The proposed circuit employs the phase opposition disposition (POD) approach to create gate pulses. Fig. 8(a) shows the schematic diagram of the control technique, and Fig. 8(b) shows the time domain waveform of LS-PWM.

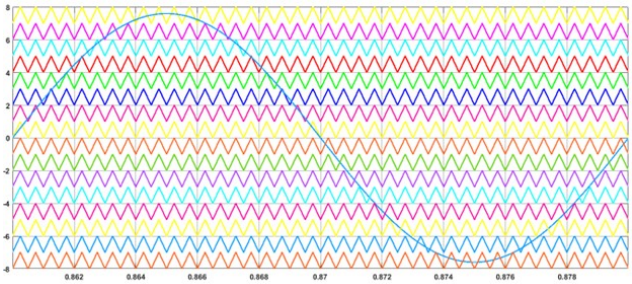
Due to the switching redundancy of particular voltage levels, a specific switching state is chosen to reduce the number of the switching transition of the IGBT device from higher to lower voltage levels. The location of high-frequency carriers determines the PWM signals generated for switches S_1 to S_7.

3.2 Simulation Results

In this sub-section, MATLAB/Simulink software is used to implement the proposed CT-type MLI with LSPWM modulation. Simulation parameters for the proposed CT-type topology are tabulated in Table 3. The input source $V_{DC1} = V_{DC2} = 24V$ is applied to generate



(a)



(b)

***Fig. 8**: Schematic diagram of (a) control technique (b) LS-PWM waveform.*

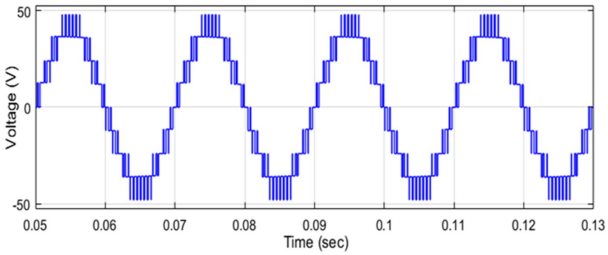


***Fig. 9**: Output voltage of proposed CT-type topology.*

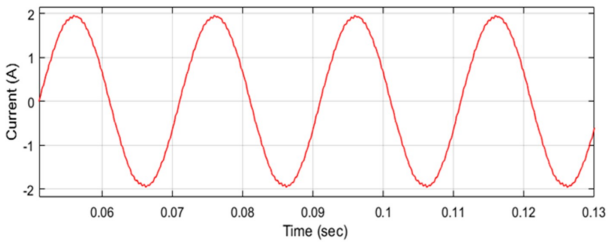


***Fig. 10**: Load current of proposed CT-type topology.*

the output voltage. Fig. 9 and 10 show the output voltage and load current, respectively.

Fig. 9 shows the 9-level output voltage waveform of the proposed CT-type topology. Correspondingly, the

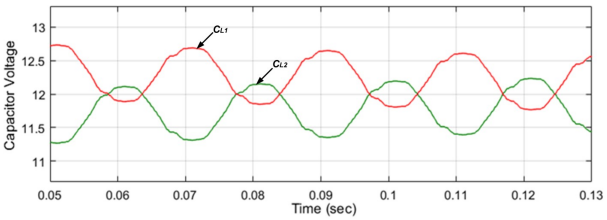


***Fig. 11**: Voltage across capacitors (C_{L1} and C_{L2}.*

***Table 4**: Parameters of Experimental Setup.*

Components	Ratings
Capacitor (LGU2A222MELA)	\$2200\mu \text{F}
DC Source (lead acid battery)	28 Ah
Driver circuit (TLP250(F))	10-35 V
Output voltage frequency	50Hz
Switching frequency	3150 Hz
IGBT switch (GW30NC120HD)	1200V, 30A
Digital storage oscilloscope (DL-750E)	6-channel
Controller board (dSPACE-1104)	-
Single-phase power analyzer (Fluke)	-
Load (RL Load)	$R = 40\Omega, L = 40$mH $R = 20\Omega, L = 20$mH

proposed CT-type topology load current waveform is shown in Fig. 10. The output voltage of the topology reaches its peak value of $V_{BB} = 48V$ at 9 levels of voltage. Fig. 11 illustrates the voltage across capacitors (C_{L1} and C_{L2}).

4. EXPERIMENTAL SETUP RESULTS

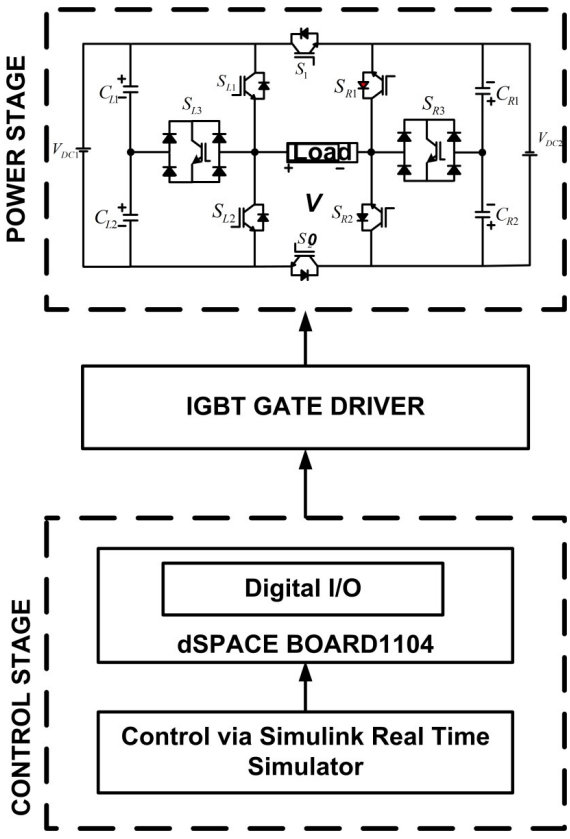
A laboratory prototype setup has been developed with power switch modules, gate drivers, and isolated power supplies to validate the proposed CT-type topology. Fig. 12 (a) and (b) show a block diagram and snapshot of the experimental setup. The values of various components and parameters are listed in Table 4. The simulated gate pulses and control method is implemented on an experimental setup using the dSPACE-1104 controller.

The prototype is created utilizing four equal DC supplies in symmetric operation, with $V_{C1L} = V_{C2L} = V_{C1R} = V_{C2R} = 12V$, bringing the total DC-link voltage of the inverter to 48 V.

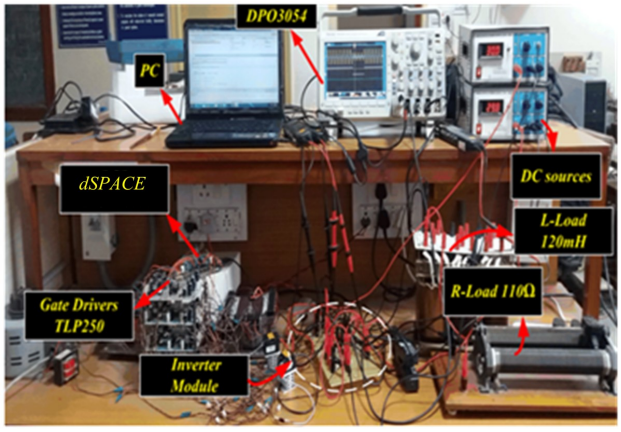
In steady-state and dynamic load conditions, experimental results of capacitor voltage, output voltage, and load current are illustrated in Figs. 13(a) and 13(b). Figs. 14(a) and 14(b) show 7.2% of voltage THD and 1.3% of current THD.

5. CALCULATION OF LOSSES AND EFFICIENCY

Mainly, two types of losses, switching and conduction losses, have been associated with power switches in the proposed CT-type topology. The conduction losses (P_C) occur because of the current flow in switches while they are in the ON state. The corresponding load current in the switch flows through the IGBT and anti-parallel diode in



(a)

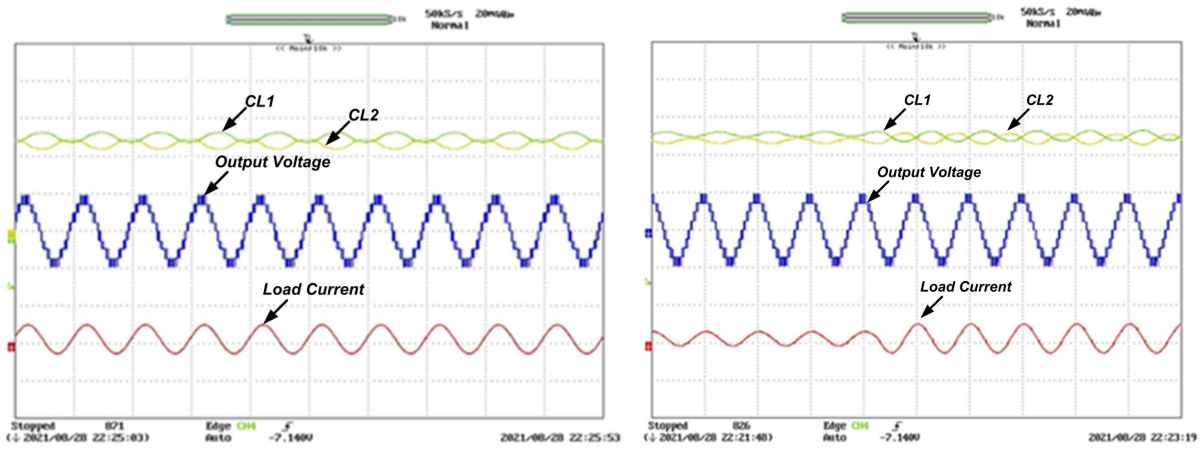


(b)

***Fig. 12**: Experimental setup (a) block diagram (b) snapshot of the test rig.*

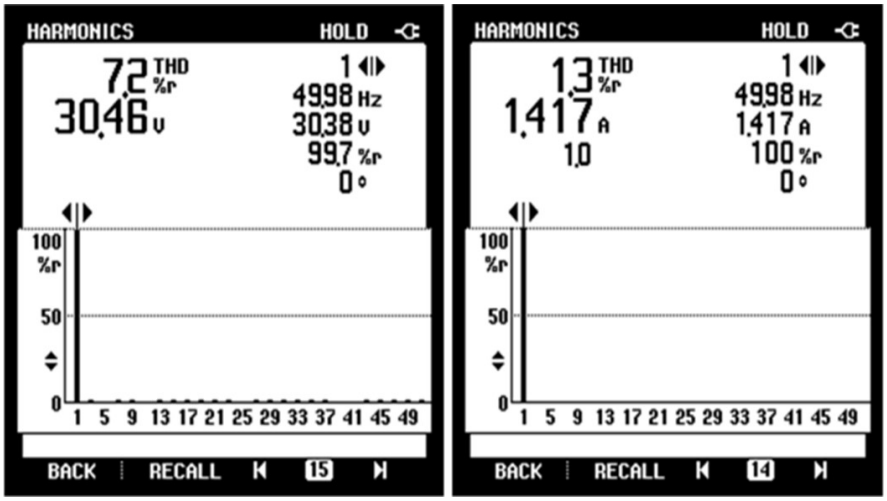
the MLI. Consequently, P_C will be calculated as the sum of the conduction losses in the IGBT ($P_{C,IGBT}$) and anti-parallel diode ($P_{C,D}$). $P_{C,IGBT}$ and $P_{C,D}$ are estimated as follows:

$$P_{C,IGBT} = n_{IGBT}(t). \left[\frac{1}{2\prod}\int_0^{2\Pi}\left[V_{ON,IGBT}I + R_{ON,IGBT}I^{\beta+1}d(\omega t)\right]\right] \quad (9)$$



(a) (b)

***Fig. 13**: (a) Experimental results with load ($R = 20\Omega$, $L = 20mH$) showing: capacitors voltage (C_{L1} and C_{L2}); output voltage and load current (b) Experimental results with transition in load ($R = 40\Omega$, $L = 40mH$) to ($R = 20\Omega$, $L = 20mH$) showing : capacitors voltage of (C_{L1} and C_{L2}) ; output voltage and load current.*



(a) (b)

***Fig. 14**: Experimental results with load (R= 20Ω, L= 20 mH) showing : (a) Output voltage THD (b) Output current THD.*

***Table 5**: Switching modes for the proposed symmetric configuration.*

Topologies	Capacitors and DC supplies	Diodes	Power switches	Driver circuit	TSV	Total components	CF/Level		
							α =0.5	α =1	α =1.5
Flying capacitor MLI	8	16	16	16	16	40	5.31	6.23	7.10
Cascaded H-bridge MLI	4	16	16	16	16	36	4.87	5.78	6.65
Diode Clamp MLI	8	24	16	16	16	48	6.21	7.12	8.01
[32]	6	14	14	14	36	34	5.76	7.76	9.78
[33]	4	12	12	12	18	28	4.12	5.10	6.12

$$P_{C,Diode} = n_{Diode}(t). \left[\frac{1}{2\prod}\int_{0}^{2\Pi}[V_{ON,Diode} + R_{ON,Diode}I^2 d(\omega t)\right] \tag{10}$$

$$P_C = P_{C,IGBT} + P_{C,Diode} \tag{11}$$

where $n_d(t)$ and $n_{IGBT}(t)$ are the numbers of the anti-parallel diode and on-state IGBTs in the current path, $V_{ON,D}$ and $V_{ON,IGBT}$ are the voltage drops of the anti-parallel diode and on-state IGBT, respectively. $R_{ON,D}$ and $R_{ON,IGBT}$ are the resistances of the anti-parallel diode and the on-state IGBT, respectively. β is the constant related to the specification of IGBT at different levels of output voltage and output current, which is assumed to be sinusoidal.

The sum of conduction losses in switches and diodes gives us the proposed CT-type inverter's total conduction losses ($P_{conduction}$). Inverter switching losses (P_{switch}) are estimated using the power consumed by switching devices in turn-off and turn-on states. Losses are evaluated in the same way for different switches. Eqs. (12) and (13) can be used to calculate the devices' turn-on (E_{on}) and turn-off (E_{off}) energy losses, respectively.

$$\begin{aligned} E_{on,T} &= \int_{0}^{ton} v(t)i(t)dt \\ &= \int_{0}^{ton}\left[\left(\frac{V_{sw}t}{t_{off}}\right)\left(-\frac{I_1(t-t_{on})}{t_{on}}\right)\right]dt \\ &= \frac{1}{6}V_{SW}I_1 t_{on} \end{aligned} \tag{12}$$

$$\begin{aligned} E_{off,T} &= \int_{0}^{toff} v(t)i(t)dt \\ &= \int_{0}^{toff}\left[\left(\frac{V_{sw}t}{t_{off}}\right)\left(-\frac{I_2(t-t_{off})}{t_{off}}\right)\right]dt \\ &= \frac{1}{6}V_{SW}I_2 t_{off} \end{aligned} \tag{13}$$

Here, I denotes the current through IGBT devices during the conduction stage, and V_{SW} denotes the voltage drop of the IGBT switches. So, the switching loss of the inverter can be computed using Eqs. (14) and (15),

$$P_S = \frac{1}{T}\left(N_{on}E_{on} + N_{off}E_{off}\right) \tag{14}$$

$$P_{loss} = P_{C,IGBT} + P_{C,Diode} + P_S \tag{15}$$

N_{off} and N_{on} denote the number of times switches are turned off and on in the 't' period. So, the sum of switching and conduction losses gives the total loss of a CT-type hybrid MLI. Hence, the efficiency can be calculated from Eq. (16),

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \tag{16}$$

The efficiency of the symmetric CT-type MLI is compared to the nine-level symmetric CHB inverter to demonstrate the superiority of the suggested circuitry. Both inverters are made using identical configurations. Therefore, the comparison is valid. Both inverters employed ABB 5SNG IGBT devices with the following parameters: $V_{IGBT} = 2.4V$, $R_{IGBT} = 0.052\Omega$, $V_{Diode} = 2V$, and $R_{Diode} = 0.1\Omega$. By applying a total voltage (DC-link) of $1300V$ and a single-phase RL load (20Ω–20mH) at the output, the power loss of both CT-type and CHB is calculated. Consequently, the MLIs can deliver 3.5 kW of output power (0.97 W/s). The overall losses of the CT-type module are calculated at 10.37 mW/s using this arrangement and (1–6). Instead, the CHB inverter's overall losses are 16.39 mW/s. Thus, the proposed MLI has a 98.94% efficiency, whereas the CHB has a 98.34% efficiency when operated for one second. The calculation mentioned above demonstrates the superiority of CT-type modules over CHB inverters. It is important to note that the proposed inverter's losses may rise slightly with time if it is used for a longer period, as the MLI has a total loss of 15.98 mW. On the other hand, the inverter's loss reached a constant state after this time and did not cause any further loss. As a result, the inverter's overall efficiency is 98.30%.

5.1 Voltage Ripples of Capacitors

The proposed MLI's switching capacitors supply voltage and current to load simultaneously. The critical drivers of voltage levels are the input voltage Vin, the output current I_o, and voltage ripples across capacitors, which are inescapable. The voltage ripples are different for unalike capacitors since the discharge times are different and the output current fluctuates over time.

When switch Q_i is turned on, capacitor $C_i (i = 1, 2, ..., n)$ begins to discharge and stops when Q_i is switched off. As a result, the voltage ripple V_i across the capacitor can be represented as Eq. (17).

$$\Delta V_i = \frac{1}{C_i}\int_{t_{i\_1}}^{t_{i\_2}} i_o(t)dt \tag{17}$$

The start and finish times of the discharge duration are t_{i_1} and t_{i_2}. For various modulation schemes, their values differ.

The SHE method considers the capacitor's discharging period to be half the fundamental frequency, or from the ζ_{i+1} to $\pi - \zeta_{i+1}$, where ζ_{i+1} is the conducting angle for switch Q_i. Hence, voltage ripple is calculated as Eq. (18),

$$\Delta V_i^{'} = \frac{1}{2\pi f_S C_i} \int_{\theta_{i+1}}^{\pi-\theta_{i+1}} i_o d(\omega t) dt \tag{18}$$

where f_S is the fundamental frequency and ω is the corresponding angular frequency. Because the output current of a purely resistive load is the staircase waveform, the charge amount ΔQ_i flows out of the capacitor C_i while the discharging period can be approximated as Eq. (19).

$$\Delta Q_i \approx \frac{V_{in}}{2\pi f_S R} \sum_{a=1}^{n} \left(\pi - 2\theta_{\alpha+1}\right)(\alpha+1) \tag{19}$$

Voltage ripple is further given in Eq. (20)

$$\Delta V_i^{'} \approx \frac{V_{in}}{2\pi f_S C_i} \sum_{a=1}^{n} \left(\pi - 2\theta_{\alpha+1}\right)(\alpha+1) \tag{20}$$

As shown in Eqs. (18) and (20), voltage ripple (ΔV) is inversely proportional to the capacitance and proportionate to the output current. This means that the higher the switching capacitance value, the greater the load capacity. Therefore, capacitor values should be determined by design requirements for minimum voltage ripples and maximum output current.

6. COMPARISON ASSESSMENTS

A comparison of numerous topologies with characteristics analogous to the proposed topology has been given in this section. The proposed CT-Type MLI topology is compared with standard topologies, such as diode clamped, FC-MLIs, CHB, and topologies in [33–36]. It is observed that CT-Type MLI provides significantly higher-level output as compared to other topologies with a reduced number of switches. It indicates that, compared to other topologies, the total number of components required to produce a given number of levels is significantly lower in the proposed topology; this can be seen in Table 5. For example, the FC-MLI, CHB-MLI, diode-clamped, and topologies given in [31, 32] need 40, 36, 48, 28, and 34 components to provide 9-level output, compared to the 22 components required for symmetric CT-Type MLI. While employing CT-Type MLI, we must use switches with higher reverse blocking capacity since total standing voltage (TSV) is significantly higher than in traditional topologies.

• Cost-effectiveness—Cost factor (CF) for proposed CT-Type MLI is obtained using Eq. (21),

$$CF = \frac{[N_{dc} + N_s + N_{dio} + N_{cap} + \alpha\,(TSV)] * nV_{dc}}{N_{levels}} \tag{21}$$

where N_{dio} is the total number of diodes, N_S is the number of switches, N_{cap} is the capacitor count, N_{DC} is the number of DC supplies, α is the weight coefficient, and TSV is the total standing voltage.

7. CONCLUSION

This paper presents a generalized single-phase CT-type reduced device count MLI topology. Also, the operating principles, control design, and TSV are explained in detail. The proposed CT-Type topology inherently achieves self-voltage balance in DC-link capacitors. The main benefit of this topology is its capability to generate negative voltage levels without using a modified H-bridge. The proposed topology can be used for higher output voltage waveforms without putting additional stress on the power switches. Therefore, this CT-Type MLI is suitable for renewable energy systems and high-voltage or power applications. Simulations and experimental results of the proposed CT-Type MLI at different load conditions are presented to show the effectiveness of the topology. Several other recently developed MLI topologies are compared to prove the superiority of the proposed CT-type topology. The proposed CT-Type is superior to the other recently developed MLI topologies in terms of the number of DC sources, capacitors, power switches, and drivers, thereby making the entire system simpler and less expensive. Hence, the proposed topology's performance in various operational situations is satisfactory.

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Vishal Rathore received his B.E. degree in Electrical and Electronics Engineering from Laxmi Narayan College of Technology (LNCT), Bhopal, India, in 2007, M.Tech. in Electrical Drives form MANIT Bhopal in 2012 and Ph.D. from NIT Jamshedpur, Jharkhand, India. Currently, he is working as an Assistant Professor at BITS Bhopal, MP, India. His fields of interest include Multilevel inverters based multiphase drives, Application of multiphase machine in electric vehicles, Real-time controllers for power electronics based drives systems, and usage of power electronics in transit systems.

Dhananjay Kumar received his BE degree from Lakshmi Narain College of Technology, Bhopal, Madhya Pradesh, India in 2014, the M.Tech (Electrical Drives) degree from Maulana Azad National Institute of Technology, Bhopal, India in 2017, and the Ph.D degree from Department of Electrical Engineering, Maulana Azad National Institute of Technology, Bhopal, India in 2022. Currently, he is working as a Senior Technologist in Department of Industrial Research Design and Development (IRDD), Aartech Solonics Ltd., Mandideep, India. His fields of interest are multilevel inverters, power electronics for renewable energy, and energy storage system.

Prateek Mundra received his B.E. degree in Electrical and Electronics Engineering from Lakshmi Narain College of Technology (LNCT), Bhopal, India, in 2014. He received M.Tech. (Power System) from MANIT, Bhopal, India. Currently, he is pursuing Ph.D. from Maulana Azad National Institute of Technology, Bhopal, India. His fields of interest include Renewable energy economics, renewable energy forecasting, power system stability etc.