Minimal Realization Plus Current Output CC-based Biquad Circuit

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ABSTRACT

This paper presents a minimal design of a biquad circuit using only one plus current output type-II current conveyor (CCII), one differential voltage current conveyor (DVCC) and grounded passive components. The circuit enables the implementation of all 5 basic filter types: low-pass (LP), band-pass (BP), high-pass (HP), band-stop (BS) and all-pass (AP) by selecting and adding input and output currents with no component matching constraints. Moreover, the circuit parameters ω_0 and Q can be set simply by adjusting the circuit components. The proposed biquad circuit performance has very low sensitivity to circuit components due to its simple structure and a small number of devices (2 active and 4 grounded passive components). This allows the circuit to work at high frequencies. Non-ideal and parasitic effects are investigated and discussed. The performance of the proposed topology was evaluated through PSPICE simulator using the 0.18 μm CMOS technology from the Taiwan Semiconductor Manufacturing Company (TSMC).

Keywords: Biquad Filter, Current Conveyors, Analog Signal Processing

1. INTRODUCTION

Today, active circuits have been widely researched and used in a wide variety of applications. In particular, the high-performance characteristics current conveyor (CC) [1] circuits, such as reduced DC power supply requirements, reduced power consumptions, high precision, high current driving capability, high bandwidth, electronic tunability and high accuracy, are available. They have been developed to many variants such as Current Voltage Conveyor (CVC) [2], Inverting CCIIs [3], Differential-Voltage Current Conveyor [4], etc. With their efficiency, therefore, they are applied in various fields such as sinusoidal oscillator [5], Variable-gain Amplifier [6], Generalized Function Generator [7] or even Nonlinear Applications such as Precision Rectifiers [8], Multiplier/Divider [9].

High performance active filters have recently received much attention because current-mode filters have many advantages compared with their voltage-mode counterpart [10-12]. The reason why current-mode circuits often performs differently from voltage-mode circuits is that current-mode circuits often use less loop gain and are less complex in terms of certain performance parameters such as propagation delay, dynamic range, and bandwidth. The characteristics of a current mode circuit make it not so vulnerable to the current demands of IC design trends, such as continuously decreased size, lower DC supply voltages and low power consumption [13-14]. Therefore, some active devices that could be exploited in both low voltage and low power have drawn a lot of attention, such as type-II current conveyor (CCII) [15], differential voltage current conveyor (DVCC) [16], differential difference current conveyor (DDCC) [17] and etc.

For biquad filter, the name of this circuit was first used by J. Tow in 1968 [18] and later by L.C. Thomas in 1971 [19]. The name derives from the fact that the transfer function is a quadratic function in both the numerator and the denominator. Hence, the transfer function is a biquadratic function. Recently, there have been many alternative designs for biquad circuit [20-24]. A general class of current amplifier-based biquadratic filter circuits [20] uses the principle of adjacent networks to design a single-amplifier quadratic (SAB) filter circuit, however it requires several passive devices.

Fully differential current conveyor (FDCCII) has been used to design the biquad circuit [22, 25]. This device provides differential difference input voltages and differential output currents into a single circuit. The proposed circuit of [22] can realize all the five filter functions but it uses two capacitors along with 3 resistors. Although [25] has been improved to use fewer resistors, due to the complexity of the circuit resulting in the need for a large supply voltage for operation.

For tuneable biquad filter, a type of transconductance circuits is commonly used. [23] uses the current follower transconductance amplifier (CFTA) and [24] uses a voltage differencing transconductance amplifier (VDTA) to alter the filter properties. However, transconductance devices often have a limited operating range and easily cause a signal distortion. Tuneable current mode universal biquad filters have also been proposed by [21], using

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three active devices (multiple-output current conveyor, MOCC) and lots of passive devices.

For the VLSI implementation point of view, the simple structures and minimum number of active and passive components are important to reduce the power consumption, noise, space, and cost. The proposed current mode biquad circuit design uses two active devices, one plus current output type-II current conveyor (CCII+) [26-27] and one differential voltage current conveyor (DVCC) [4, 28]. The plus current output type-II current conveyor (CCII+) has a simpler circuit configuration than the minus current output circuit. Furthermore, it has a wide operating range and low power consumption compared to the minus current output current conveyor [26]. Both of them have a simple internal structure, which is able to operate at low voltages and retain low power consumption at high-speed operation. The proposed circuit requires 4 grounded passive components without requiring passive component matching constraints. It is very suitable for IC technology [29]. The circuit enables all 5 basic filter types, low-pass (LP), band-pass (BP), high-pass (HP), band-stop (BS) and all-pass (AP) implementing by selecting and adding the input and output currents with no component matching constraints. The circuit has the orthogonal adjusting capability for circuit parameters ω_0 and Q, which is required for an application. The proposed circuit use low supply voltage as ±0.6V which comparable to the circuit proposed by [30] using 1.2V differential difference transconductance amplifier as active device but less component count.

In the section 2 the active devices used in the designed filter are discussed. In the section 3 the block diagram and transfer functions of the proposed circuit are demonstrated. Section 4, the non-ideal analysis of these two active devices is used to see their impact on the operation of the circuit. Section 5, the parasitic effect of low-pass (LP) and band-pass (BP) is analysed. Next the simulation results of the proposed biquad circuit using PSPICE by using the 0.18 mm TSMC's CMOS technology are shown and then the conclusion.

2. PLUS CURRENT OUTPUT CURRENT CONVEYOR (CCII+) AND DIFFERENTIAL VOLTAGE CURRENT CONVEYOR (DVCC)

The dual plus current output second generation current conveyor (CCII+) and the multiple plus current output differential voltage current conveyor (DVCC) are symbolically shown in Fig. 1(a) and (b), respectively.

2.1 CCII+

A current conveyor is an abstraction for a three-terminal designated X, Y, and Z, an analogue electronic device. The potential at X equals whatever voltage is applied to Y and no current flows through terminal Y. As its name a current conveyor, any current out of terminal X is reflected at terminal Z. If the current flowing out of X resulted in the same direction of current flowing out of Z,

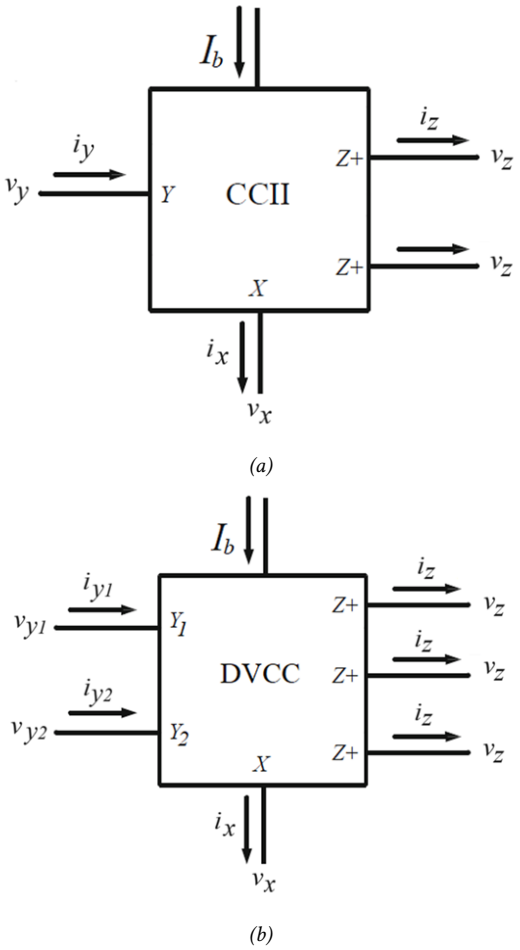


***Fig. 1**: (a) plus current output CCII+ [26] (b) plus current output DVCC [4,28].*

it is called plus current output current conveyor circuit, CCII+. The CCII+ is characterized by

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad (1)$$

The current conveyor can be implemented in many forms. Fig. 2(a) shows CMOS CCII+ with Class AB configuration [27]. M1 to M4 act as Voltage followers which lead v_x equal to v_y. The bias current (I_b) sets the operating points of M1-M4 through current mirrors M6-M7 and M11-M12, which forces i_y equal to 0. The current mirrors (M8 to M10) and (M13 to M15) cause i_z equal to i_x.

2.2 DVCC

A differential voltage current conveyor (DVCC) [26] is a powerful analogue building block, especially for applications demanding differential or floating inputs like impedance converter circuits and current mode instrumentation amplifiers. It can be implemented by MOS transistor shown in Fig. 2(b). The DVCC is

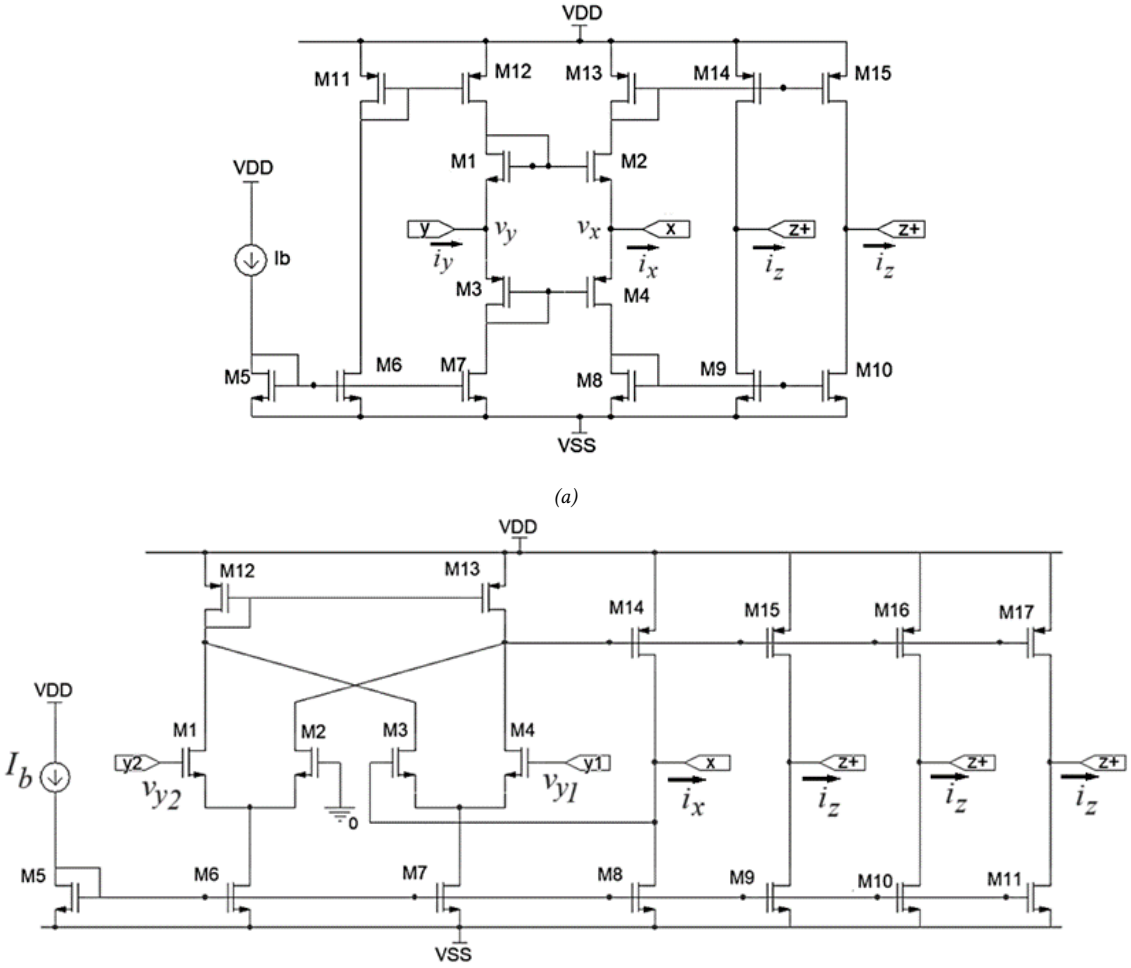


***Fig. 2**: (a) plus current output CCII+ (b) plus current output DVCC [26].*

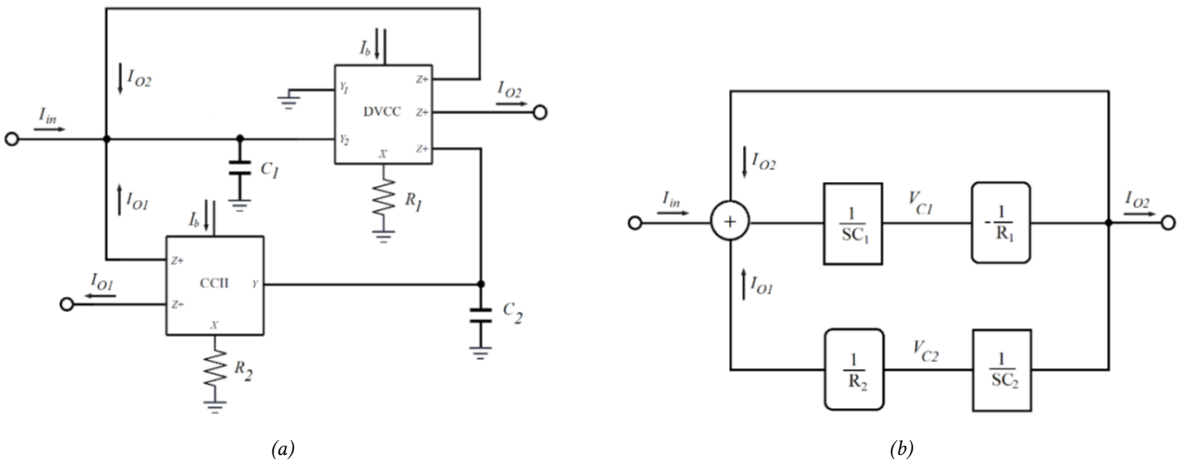


***Fig. 3**: (a) proposed circuit (b) equivalent block diagram.*

characterized by

$$\begin{bmatrix} i_{y1} \\ i_{y2} \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{y1} \\ v_{y2} \\ i_x \\ v_z \end{bmatrix} \quad (2)$$

The two differential stages composed of M1-M2 and M3- M4 and a current mirror M12-M13, which provide a relation of the v_x to be a differential voltage of v_{y1} and v_{y2}.

The M8 to M11 and M14 to M17 will duplicate i_x to

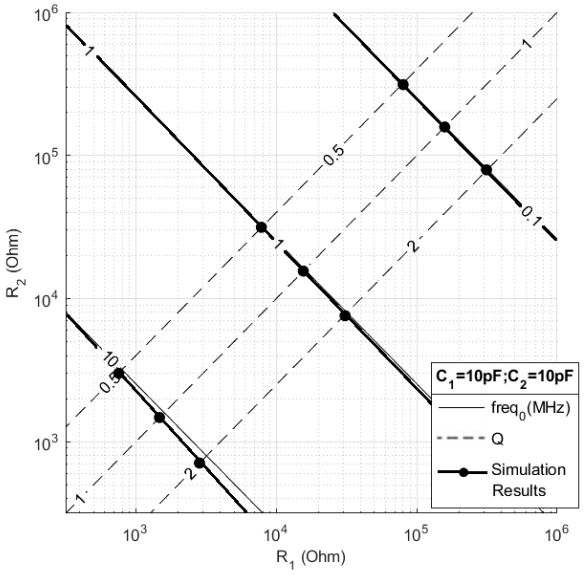


Fig. 4: R_1 and R_2 values when given $C_1 = C_2 = 10\ pF$.

multiple i_z for using in the biquad circuit, which will be mentioned in the next section.

3. THE PROPOSED PLUS CURRENT OUTPUT CURRENT CONVEYOR BIQUAD CIRCUIT

The transfer function of biquad circuit is a quadratic function in both the numerator and the denominator, then $T(s)$

$$T(s) = \frac{a_2 S^2 + a_1 S + a_0}{S^2 + b_1 S + b_0} = \frac{a_2\left(S^2 + \left(\frac{\omega_Z}{Q_Z}\right)S + \omega_Z^2\right)}{S^2 + \left(\frac{\omega_P}{Q_P}\right)S + \omega_P^2} \quad (3)$$

Hence, the low-pass ($a_2 = a_1 = 0$), high-pass ($a_1 = a_0 = 0$), band-pass ($a_2 = a_0 = 0$), band-stop ($a_1 = 0$) or all-pass responses can be performed. The proposed biquad circuit is comprised of one CCII+, one DVCC and 4 grounded components operating in current mode as shown in Fig. 3(a). Its equivalent circuit is shown in Fig. 3(b) that can be easily transformed into transfer functions:

$$T_{BP}(s) = \frac{I_{02}}{I_{in}} = -\frac{sR_2C_2}{s^2R_1R_2C_1C_2 + sR_2C_2 + 1} \quad (4a)$$

$$T_{LP}(s) = \frac{I_{01}}{I_{in}} = -\frac{1}{s^2R_1R_2C_1C_2 + sR_2C_2 + 1} \quad (4b)$$

***Table 1**: Component Sensitivity.*

Component	ω_0	Q
R_1	-0.5	0.5
R_2	-0.5	0.5
C_1	-0.5	0.5
C_2	-0.5	0.5

Therefore, a biquad filter parameter can be demonstrated as

$$\omega_0 = \sqrt{\frac{1}{R_1R_2C_1C_2}} \quad (5a)$$

$$\frac{\omega_0}{Q} = \frac{1}{R_1C_1} \quad (5b)$$

$$Q = \sqrt{\frac{R_1C_1}{R_2C_2}} \quad (5c)$$

Table 1 shows the sensitivity with respect to the circuit components.

From (5a) and (5b), the parameters ω_0 and ω_0/Q are orthogonally adjustable. For the fix-valued capacitors C_1 and C_2, and the specified value of ω_0 and Q, the resistors R_1 and R_2 can be calculated as,

$$R_1 = \frac{Q}{C_1\omega_0} \quad (6a)$$

$$R_2 = \frac{1}{C_2\omega_0 Q} \quad (6b)$$

Although the parameters ω_0 and Q are interactive, the filter parameter control can be non-interactively obtained as follows: for the fix-valued capacitors, ω_0 can be tuned arbitrarily without disturbing Q while simultaneously changing R_1 and R_2 and keeping the ratio R_1/R_2 constant. The parameter Q can also be adjusted without disturbing ω_0 by simultaneously changing R_1 and R_2 and keeping the product R_1R_2 constant. The tunable grounded resistors can be used for R_1 and R_2 for electronically set the ω_0 and Q [31-33].

Fig. 4 shows examples of R_1 and R_2 values when $f_0 = \omega_0/2\pi$ = 0.1, 1, 10, 100 MHz and when Q = 0.5, 1, and 2 when given $C_1 = C_2$ = 10pF.

The High-Pass (HP), Band-Stop (BS) and All-Pass (AP) filter can be achieved by the current manipulation by selection and addition of the circuit currents (I_{01} and I_{02}) with the duplicated I_{in} which can be generated from a current copier circuit [34]. The corresponded circuit transfer functions are

$$T_{HP}(s) = \frac{I_{in}(s) + I_{01}(s) + I_{02}(s)}{I_{in}(s)} = \frac{s^2R_1R_2C_1C_2}{s^2R_1R_2C_1C_2 + sR_2C_2 + 1} \quad (7a)$$

$$T_{BS}(s) = \frac{I_{in}(s) + I_{02}(s)}{I_{in}(s)} = \frac{s^2 R_1 R_2 C_1 C_2 + 1}{s^2 R_1 R_2 C_1 C_2 + s R_2 C_2 + 1} \quad (7b)$$

$$T_{AP}(s) = T_{BP}(s) + T_{BS}(s) = \frac{s^2 R_1 R_2 C_1 C_2 - s R_2 C_2 + 1}{s^2 R_1 R_2 C_1 C_2 + s R_2 C_2 + 1} \quad (7c)$$

As shown in equations above, it can be deduced that all active and passive and sensitivities of this circuit are very low.

4. NON-IDEALITY ANALYSIS

In this section, we discuss the effect of non-idealities of the CCII+ and DVCC on the biquadratic characteristic. the DVCC non-idealities can be characterized by

$$\begin{bmatrix} i_{y1} \\ i_{y2} \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{y1} \\ v_{y2} \\ i_x \\ v_z \end{bmatrix} \quad (8)$$

where R_{x1}, a_1 and b_{1i} (i = 1, 2) are intrinsic resistance at the x-terminal, current gain and voltage gain, respectively. As well as, The CCII+ considering the non-idealities is characterized by

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta_2 & R_{x2} & 0 \\ 0 & \alpha_2 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad (9)$$

The current gains (a_i ; i = 1, 2) and voltage gains (b_i ; i = 1 and 2) can be expressed by using current-tracking error $e_c << 1$ and voltage-tracking error $e_{vi} << 1$ [28] as

$$\alpha_i = 1 - \varepsilon_{ci} \text{ and } \beta_i = 1 - \varepsilon_{vi} \quad (10)$$

Using equations (8) and (9), the biquad circuit transfer functions are derived under the conditions where $a_1 = a_2 = a$ and $b_{11} = b_{12} = b_2 = b$ as

$$T_{BP}(s) = \frac{I_{02}}{I_{in}} = -\frac{\alpha\beta s R'_2 C_2}{s^2 R'_1 R'_2 C_1 C_2 + \alpha\beta s R'_2 C_2 + \alpha^2\beta^2} \quad (11a)$$

$$T_{LP}(s) = \frac{I_{01}}{I_{in}} = -\frac{\alpha^2\beta^2}{s^2 R'_1 R'_2 C_1 C_2 + \alpha\beta s R'_2 C_2 + \alpha^2\beta^2} \quad (11b)$$

$$T_{HP}(s) = \frac{I_{in}(s) + I_{01}(s) + I_{02}(s)}{I_{in}(s)} = \frac{s^2 R'_1 R'_2 C_1 C_2}{s^2 R'_1 R'_2 C_1 C_2 + \alpha\beta s R'_2 C_2 + \alpha^2\beta^2} \quad (11c)$$

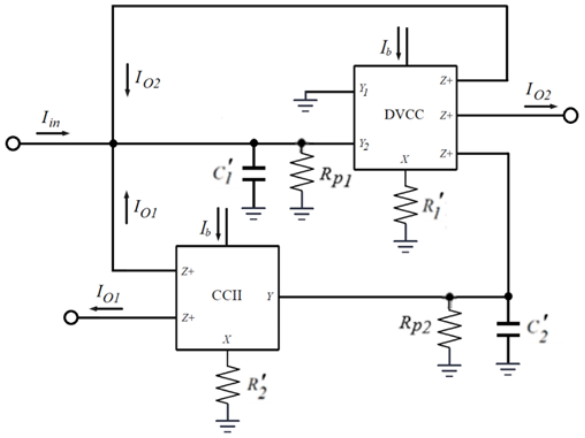


***Fig. 5**: Time responses simulation results of proposed circuit ($f_0 = 1MHz$ and $Q = 1$) when apply input signal at frequency (a) 0.1 MHz, (b) 1 MHz and (c) 10 MHz.*

$$T_{BS}(s) = \frac{I_{in}(s) + I_{02}(s)}{I_{in}(s)} = \frac{s^2 R'_1 R'_2 C_1 C_2 + \alpha^2\beta^2}{s^2 R'_1 R'_2 C_1 C_2 + \alpha\beta s R'_2 C_2 + \alpha^2\beta^2} \quad (11d)$$

and,

$$T_{AP}(s) = T_{BP}(s) + T_{BS}(s) = \frac{s^2 R_1 R_2 C_1 C_2 - s R_2 C_2 + 1}{s^2 R_1 R_2 C_1 C_2 + s R_2 C_2 + 1} \quad (11e)$$

where,

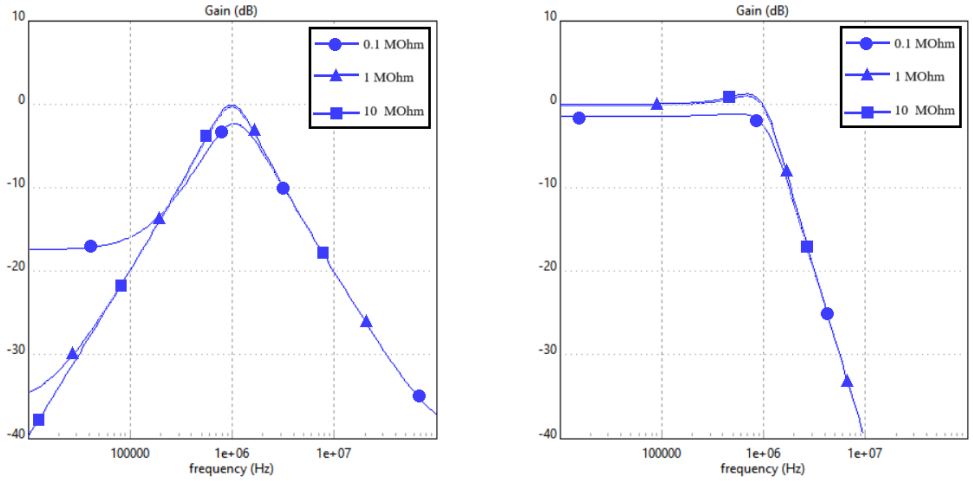
$$R'_1 = R_1 + R_{x1} \text{ and } R'_2 = R_2 + R_{x2} \quad (12)$$

The circuit parameter ω_0 and Q become

$$\omega_0 = \frac{\alpha\beta}{\sqrt{R'_1 R'_2 C_1 C_2}} \quad (13)$$

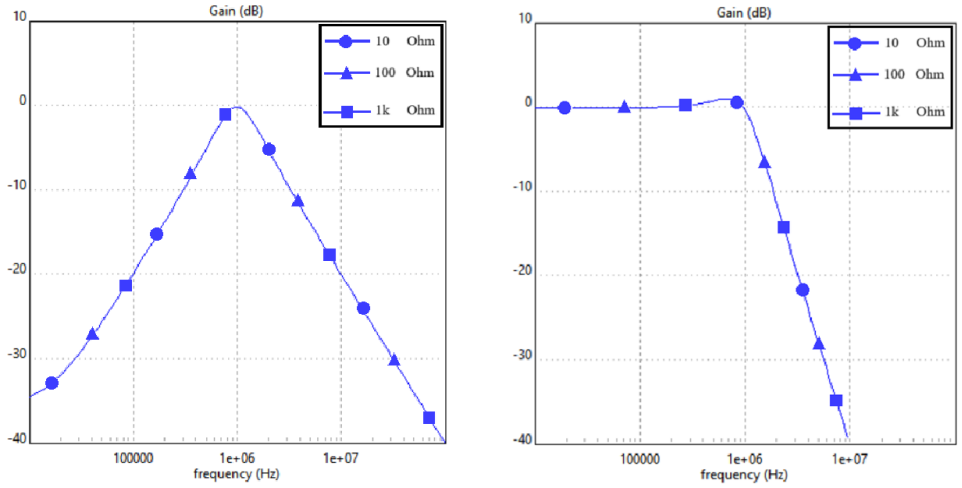
$$Q = \sqrt{\frac{R'_1 C_1}{R'_2 C_2}} \quad (14)$$

Equations (13) and (14) demonstrate that deviations from ideal circuit characteristics arise due to non-ideal factors associated with the x-terminal resistance (R_x), current gains (α), and voltage gains (β). It is noteworthy that equation (13) reveals the potential for mitigating the influence of non-idealities on the circuit parameter ω_o through the introduction of pre-distortion via the resistor R'_i. Furthermore, the x-terminal resistances R_{x1} and R_{x2} can be precisely adjusted by manipulating the bias currents of the CCII+ and DVCC components. This underscores the significance of pre-tuning these bias currents as a viable means to effectively diminish the impact of non-idealities.



(a) *(b)*

***Fig. 6**: Parasitic effect of parasitic resistance ($R_{p1} = R_{p2}$) 0.1, 1, and 10 MOhm (a) Band pass and (b) Low pass.*



(a) *(b)*

***Fig. 7**: Parasitic effect of parasitic resistance ($R_{px1} = R_{px2}$) 10, 100, and 1 kOhm (a) Band pass and (b) Low pass.*

5. PARASITIC EFFECT

Parasitic impedances of the proposed circuit are shown in Figure 5. The parasitic elements in components are in the internal circuit, the parasitic resistance of the component leads and the parasitic capacitance of the component packaging. The real DVCC and CCII have parasitic resistors and capacitors at terminal Y and Z to the ground and a serial resistor at the input terminal X. Considering the DVCC and CCII parasitic impedances, the transfer functions of the Low-pass and Band-pass the of proposed circuit are obtained and given in (15a) and (15b) for non-ideal case, respectively.

R_{p1} is the parallel parasitic resistance of the input impedance of Y_2 terminal of DVCC and the total effective output impedance of the two-output current mirrors of DVCC and CCII at Z+ terminal.

R_{p2} is the parallel parasitic resistance of the the input impedance of Y terminal of CCII and the total effective output impedance of the two-output current mirrors of DVCC at Z+ terminal.

R_1' is the series resistance of R_1 and the parasitic resistance of DVCC at X terminal (R_{px1}).

R_2' is the series resistance of R_2 and the parasitic resistance of CCII at X terminal (R_{px2}).

C_1' is the parallel capacitance of C_1, the input capacitance of Y_2 terminal of DVCC and the total effective output capacitance of the two-output current mirrors of DVCC and CCII at Z+ terminal.

C_2' is the parallel capacitance of C_2, the input capacitance of Y terminal of CCII and the total effective output capacitance of the two-output current mirrors of DVCC at terminal Z+.

At the X terminals parasitic series resistances decrease effective resistances, while at the Z and Y terminals parasitic parallel capacitances increase effective capacitances. In effects of parasitic impedance case, natural frequency

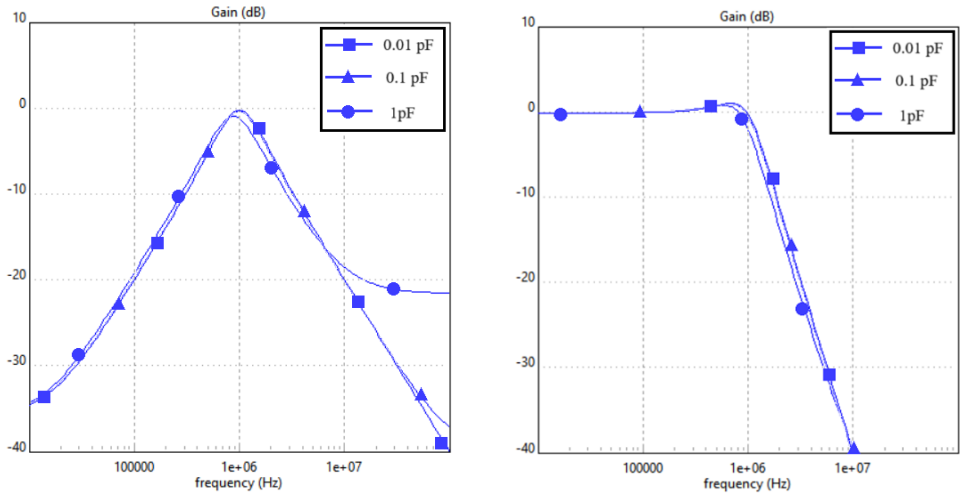


***Fig. 8**: Parasitic effect of parasitic capacitance for each terminal of DVCC and CCII 0.01, 0.1, and 1 pF (a) Band pass and (b) Low pass.*

$$T_{LP}(s) = \frac{I_{01}}{I_{in}} = -\frac{1}{s^2(C_1'C_2'R_1'R_2') + s\left(C_2'R_2'(1+\frac{R_1'}{R_{p1}}) + C_1'R_1'R_2'\frac{1}{R_{p2}}\right) + \left(\frac{R_2'}{R_{p2}} + \frac{R_1'R_2'}{R_{p1}\ R_{p2}} + 1\right)} \tag{15a}$$

$$T_{BP}(s) = \frac{I_{02}}{I_{in}} = -\frac{s\left(C_2'R_2'\right) + \frac{R_2'}{R_{p2}}}{s^2(C_1'C_2'R_1'R_2') + s\left(C_2'R_2'(1+\frac{R_1'}{R_{p1}}) + C_1'R_1'R_2'\frac{1}{R_{p2}}\right) + \left(\frac{R_2'}{R_{p2}} + \frac{R_1'R_2'}{R_{p1}\ R_{p2}} + 1\right)} \tag{15b}$$

$$\omega_0' = \left(\frac{1}{\sqrt{C_1'C_2'}}\right)\left(\sqrt{\frac{1}{R_1'R_2'} + \frac{1}{R_1'R_{p2}} + \frac{1}{R_{p1}\ R_{p2}}}\right) \tag{16a}$$

and,

$$Q' = \left(\frac{\sqrt{C_1'C_2'}}{\frac{C_1'}{R_{p2}} + C_2'\left(\frac{1}{R_1'} + \frac{1}{R_{p1}}\right)}\right)\left(\sqrt{\frac{1}{R_1'R_2'} + \frac{1}{R_1'R_{p2}} + \frac{1}{R_{p1}\ R_{p2}}}\right) \tag{16b}$$

(ω_0') and quality factor (Q') of the proposed circuit are found as (16).

From (16), it can be easily observed that the circuit parameter, the natural frequency (ω_0') and quality factor (Q') changes depend on values of parasitic impedances. Fig. 6x-8x show the calculation results of the parasitic effect for the Band-pass (BP) and Low-Pass (LP). The nominal parasitic resistances (R_{p1}, R_{p2}), (R_{px1}, R_{px2}) and parasitic capacitance of each terminal are assumed to equal to 1 MOhm, 100 Ohm and 0.1pF, respectively. Fig. 6, 7 and 8 are calculation results of parasitic effect when alter (R_{p1}, R_{p2}), (R_{px1}, R_{px2}) and parasitic capacitances, respectively. The effect of parasitic resistance of DVCC and CCII at X terminal have less impact on circuit parameter (ω_0' and Q') due to their small resistance when compare with R_1 and R_2.

***Table 2**: Component Sensitivity.*

Mos transistors	W/L (µm)
Plus current output CCII+ (Fig. 2a)	
M1-M4	15/0.18
M5-M15	5/0.35
Plus current output DVCC (Fig. 2b)	
M1-M4	15/0.18
M5-M17	5/0.35

6. SIMULATION RESULTS

The proposed circuit performance was evaluated through PSPICE simulator using the 0.18 ⊠m CMOS technology from Taiwan Semiconductor Manufacturing

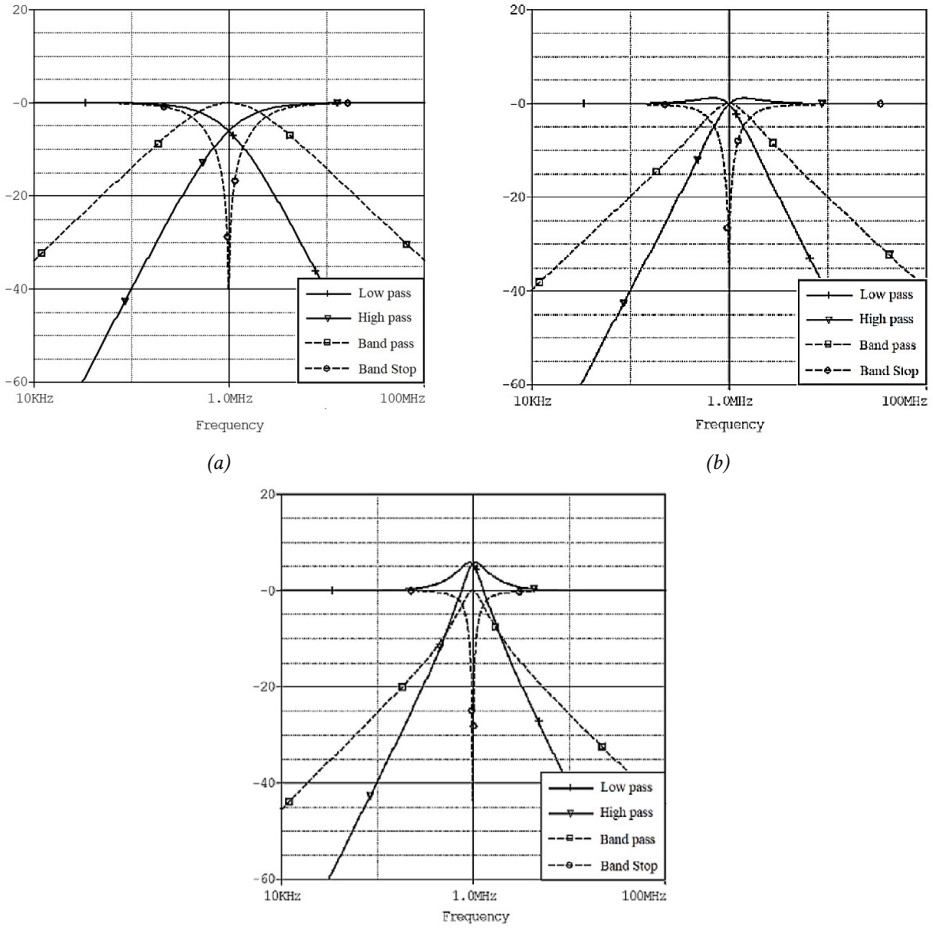


***Fig. 9**: Simulation results of proposed biquad circuit (f_0 = 1MHz) LP, HP, BP, BS (a) Q = 0.5, (b) Q = 1, (c) Q =2.*

***Table 3**: The set R_1 and R_2.*

Q	0.5	1	2
R_1	7.96k	15.92k	31.8k
R_2	31.8k	15.92k	7.96k

(f_0 = 1MHz and $C_1 = C_2$ = 10pF)

***Table 4**: Comparison with other current-mode biquad filter.*

Reference	No. of active component	No. of passive component	Supply Voltage	All five-filter function realized
[10]	2	2	-	No
[11]	4	2	-	YES
[16]	2	5	±1.5	YES
[21]	3	3	±1.5	YES
[22]	1	5	±1.25	YES
[23]	1	3	±3	No
[24]	1	3	±1	YES
[25]	1	4	±1.65	YES
[26]	3	4	±1.2	YES
[28]	2	4	±1.5	YES
[30]	5	2	1.2	YES
Proposed	2	4	±0.6	YES

Company (TSMC). The aspect rations (W/L) of CCII+ and DVCC in Fig. 2 (a) and (b), respectively, are shown in table 2. DC supply is set to VDD = -VSS = 0.6V when bias current (I_b) is set to 10 μA.

For simulating the filter circuit, I_{in} is set the amplitude to 1 μA; f_0 = 1 MHz. When given $C_1 = C_2$ = 10 pF, equation (6) can be used to obtain R_1 and R_2 as shown in Table 3. The results of the simulation of Low-pass (LP), High-pass (HP), Band-pass (BP) and Band-stop (BS) filter are shown in Fig. 9 (a), (b) and (c) when Q = 0.5, 1 and 2, respectively. For All-pass (AP) filter, the simulation results are shown in Fig. 10 (a), (b) and (c) when Q = 0.5, 1 and 2. The power dissipation was 0.16 mW.

Fig. 11 is the time response simulation result of Low-pass (LP), High-pass (HP), Band-pass (BP), Band-stop (BS) and All-pass (AP) filter which is set to operate at f_0 = 1MHz and Q = 1 by given $C_1 = C_2$ = 10pF and $R_1 = R_2$ = 15.92 kOhm. Fig. 11 (a), (b) and (c) is the time response when applied the input current signal at 0.1, 1 and 10 MHz, respectively.

Furthermore, a Monte-Carlo analysis was conducted to assess the tolerance variations of passive components. The simulation involved subjecting the BP output to a Gaussian deviation of 1% in components C_1, C_2 (both set

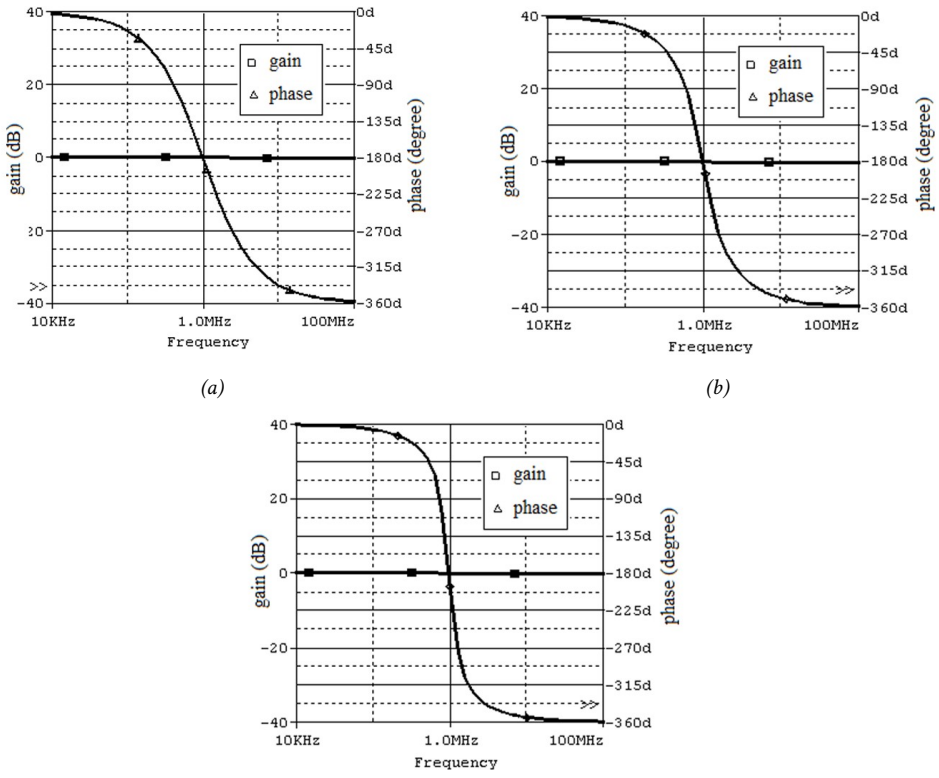


***Fig. 10**: Simulation results of proposed biquad circuit (f_0 = 1MHz) AP (a) Q = 0.5, (b) Q = 1, (c) Q =2.*

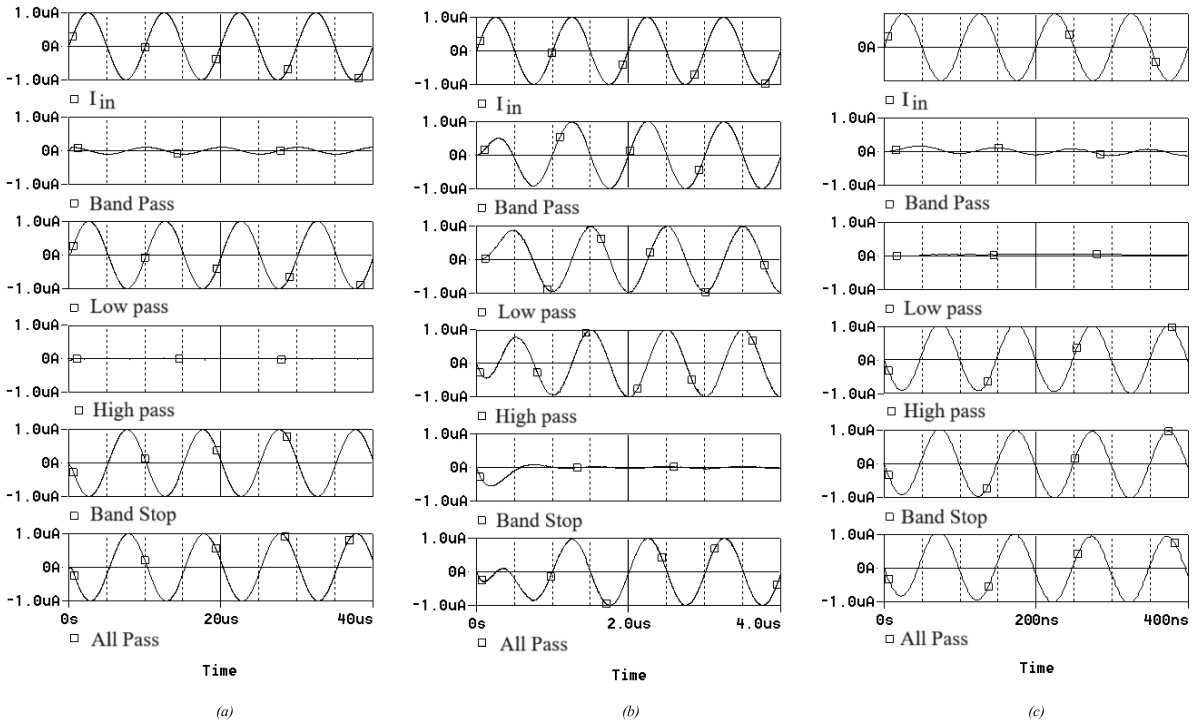


***Fig. 11**: Time response simulation results of proposed circuit (f_0 = 1 MHz and Q = 1) when applying input signal at frequency (a) 0.1MHz, (b) 1MHz and (c) 10MHz.*

at 10pF), and R_1, R_2 (both set at 15.92kΩ), with the circuit configured for f_0 = 1MHz and Q = 1. This simulation was executed iteratively in 100 runs. As depicted in Figures 12(a) and 12(b), the resulting histograms illustrate

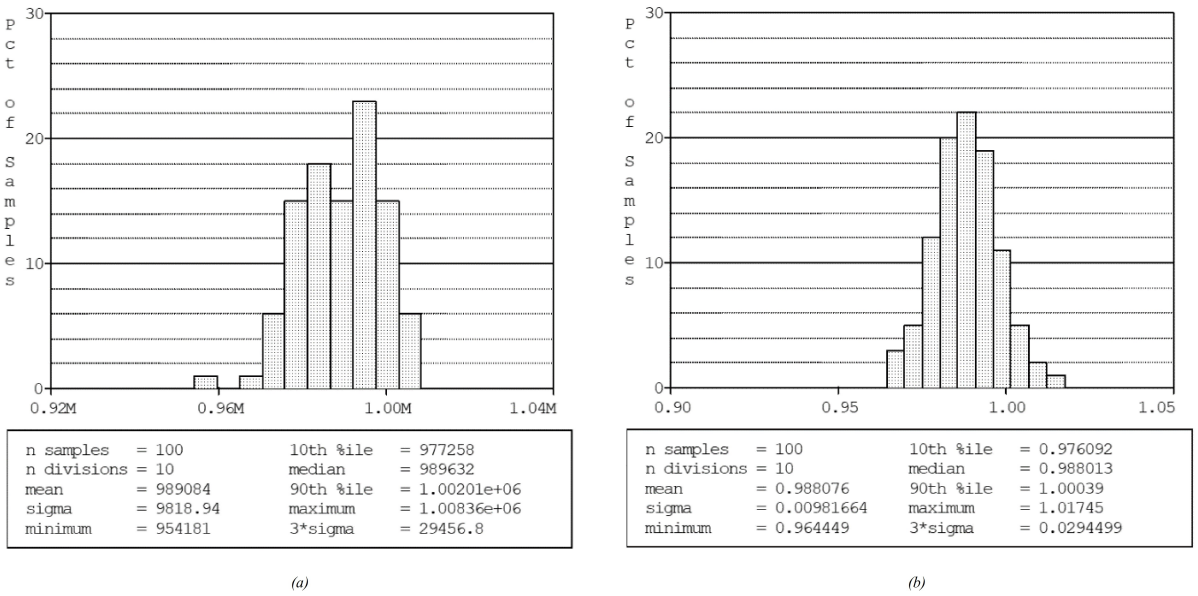


***Fig. 12**: Monte-Carlo analysis results of proposed circuit (a) f_0, (b) Q.*

the distributions of f_0 and Q, respectively. These plots reveal that the simulated standard deviation and mean values for f_0 are 9.818KHz and 0.989MHz, respectively, while for Q, they are 0.988 and 0.009, respectively. These findings indicate that variations in component values do not significantly impact the circuit's overall performance.

7. CONCLUSION

In this paper, a current mode biquad filter circuit is introduced. It composes of differential voltage current conveyor (DVCC) and the plus current output type-II current conveyor (CCII+), which have a simpler circuit configuration. Therefore, the circuit requires low supply voltage. The comparison with other current-mode biquad filter design is shown in Table 4. The proposed circuit offers several appealing characteristics, including the capability to realize all five essential functions, eliminating the need for component-matching requirements. It leverages the plus current output current conveyor approach to reduce power consumption and extend its suitability for wide-band applications. Additionally, the design utilizes all grounded passive components, making it highly suitable for integrated circuit (IC) implementation. Furthermore, the circuit provides orthogonal tunability for both ω_0 and Q parameters while demonstrating low-sensitivity performance. These advantageous attributes are substantiated by the simulation results and the outcomes of Monte-Carlo Analysis.

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