A New Single-Source Switched-Capacitor Based Seven-Level Boost Inverter Topology with Reduced Part Count and Voltage Stress

Kasinath Jena[1], **Dhananjay Kumar**[2†], **Gangadhar Dhal**[3], **Pradeep Kumar Sahu**[3], and **Lipika Nanda**[3], Non-members

ABSTRACT

The use of multi-level inverters is a widespread and effective solution for solar power plants, wind farms, and other types of renewable energy sources. A novel switched-capacitor multi gain inverter topology (SCMGIT) is proposed in this paper. The research presents a SCMGIT that, with a single dc source, can produce seven distinct voltage levels at a voltage-boosting of three times the original input. The proposed SCMGIT exhibits several noteworthy characteristics, including self-balancing capacitor voltages, fewer switches with decreased voltage stress, and bipolar voltage generation without the usage of a backend H-bridge. A thorough comparison with other SC inverter has been performed in the article to highlight the benefits of the suggested SCMGIT. An analysis of the proposed SCMGIT has been investigated, and verified by simulation and experimental testing with a low prototype.

Keywords: Boosting Factor, Cost Function, MBV, Multilevel Inverter, TSV

1. INTRODUCTION

Multilevel inverters (MLIs) are commonly utilized in industrial and residential applications due to their unique qualities, which include the ability to provide a virtually sinusoidal output voltage waveform, greater power control capabilities, increased efficiency, and reduced filter size needs.[1].

There have been several advancements made to the multi-level inverter throughout the many decades since its inception. MLIs offer a number of advantages over traditional two-level inverters, including lower peak-inverse-voltage (PIV) of the power switches and diode, improved waveform, lower dv/dt stresses on the power switches and load, and so on. Neutral Point Clamped (NPC) converters, Flying Capacitor (FC) converters, and cascaded H-bridge (CHB) converters are three examples of the prominent multilevel topologies utilized in industrial applications [2]. These inverters have various restrictions, including unity gain, the requirement of many active and passive components, capacitors voltage balancing, etc. Simultaneously, the structural and control complexity of multilevel inverters increases.

In recent years, a new form of MLIs based on switched capacitor technology (SCT) has been presented as a solution to this problem [4-20]. The advantages of SCT include a gain larger than one, suitability for sources with the low input voltage, self-balancing of capacitor voltage, and so on.

Existing topologies in the literature [3–4] all have one essential feature in common; they are made up of two stages. The first stage, typically a switched-capacitor dc-dc converter, is used to generate positive voltage levels, while the second stage, typically an H-bridge, is used to regulate the output voltage's polarity. Second-stage power switches in these topologies are often subjected to voltage stress at or near the maximum level, which is a significant inconvenience. The series/parallel SCMLI described in [4] is capable of producing 2n+3 levels of ac output voltage, with each level equal to the dc input voltage. where n is the number of SC cells and each level is equivalent to the dc input voltage. And the voltages of all capacitors in this SCMLI are automatically balanced without the usage of additional balancing circuits and control algorithms. Additionally, the triple gain SC configuration advocated in [5-6] results in high voltage stress across the H-bridge switches, restricting its usage to high voltage applications.

Only one input source, one T-type converter, and many H-bridges are needed for the proposed symmetric hybrid MLI [7]. However, the proposed topology minimizes the total number of parts, which boosts performance and reduces costs.

Single-stage topologies alleviate the disadvantages of two-stage topologies [8-19]. The single-stage topologies are more convenient since they do not necessitate the usage of an H-bridge to generate polarity. To create the architecture seen in [8] three H-bridges are cascaded with two bidirectional switches. Though they have the

Manuscript received on October 11, 2023; revised on March 1, 2024; accepted on March 25, 2024. This paper was recommended by Associate Editor Chainarin Ekkaravarodome.

[1]The author is with Department of Electrical and Electronic Engineering, ARKA JAIN University, Jamshedpur-831001, India.

[2]The author is with Department of Electrical Engineering, Government Engineering College Siwan, Bihar-841226, India.

[3]The authors are with School of Electrical Engineering, KIIT University, Bhubaneswar, Odisha-751024, India.

[†]Corresponding author: dhananjaymanit23@gmail.com

Digital Object Identifier: 10.37936/ecti-eec.2024222.251240

benefit of CHB, they need a total of sixteen switches A reduced device count seven-level ANPC described in [8] that is capable of voltage-boosting by 1.5 times its normal amount [9]. In order to supply a seven-level voltage with a three-fold gain, the topology [10] makes use of a larger number of switching components. A 13-level design was also proposed in [11], which uses fewer components and offers the benefits of lower voltage stress and a 6X gain. There is no H-bridge in the self-balanced MLI proposed in [12], but the concept is quite similar to that of series/parallel SC MLI. The increased number of switches is the main disadvantage of this design. Although the SC topology [13] has a low number of switching components, the TSV per unit is relatively high. The low-voltage stress on the switches in the topologies presented in [14-15] make them more suited to high-voltage applications, but it requires larger switching components. The design described in [16] employs sixteen switches to achieve seven voltage levels by guaranteeing that no switch operates at a voltage greater than the dc source voltage. Topology presented in [17] is more suitable for high voltage applications because of low-voltage stresses on the switches; however, they are designed with higher switching components with lower gain. Although a generalized SC design offers the advantages of reduced voltage stresses and leakage current described in [18], it involves a substantial number of switching counts. The SCMLI described in [19] has a three-boosting factor and employs reduced devices to achieve seven output voltage levels. However, it puts greater stress on the switching components, i.e., equal to the peak load voltage. In [20], a SC inverter design is proposed that is both efficient and economical, utilizing minimum switches to achieve triple-gain.

The advantages of the proposed SCMGT are as follows:

1. The proposed architecture has a voltage gain of 1:3.
2. The proposed architecture operates from single DC source
3. Even at low modulation indices, all capacitors are self-balanced.
4. PIVs for all power switches are significantly lower than the load voltage
5. the number of components used per level has decreased
6. Automatic polarity reversal without a need of a back H-bridge.
7. It has the capability of producing 7L output voltage using 12 switches.

Following this section, the rest of the article is organized in the following manner. Section II describes the circuit, operating concept and the self-balancing mechanism of capacitor voltage. Section III details the modulation scheme. Section IV provides the details of the SCMGIT loss evaluation. Comparison with the state-of-art SC topologies provided in Section V. The proposed SCMGIT utility and practicality are evaluated using MATLAB/Simulink and experimentation, as stated in Section VI. The final section VII contains the conclusion part.

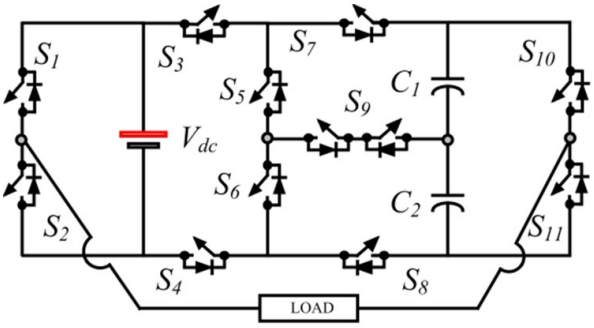

***Fig. 1**: Proposed seven-level SCMGT.*

2. PROPOSED SCMGIT

2.1 Circuit Description

Fig. 1 depicts a schematic design of the proposed SCMGIT. The SCMGIT comprises two capacitors, eleven switches, and a single unit DC supply. This SCI topology incorporates the concept of switched capacitors, which can be charged and discharged while tied to the DC voltage source. The proposed architecture is capable of producing a peak voltage amplitude of $3V_{dc}$, which is a noteworthy characteristic of the research. Out of the twelve switches, eight ($S_1 \sim S_5$, S_7, S_9,) have a voltage rating of V_{dc}, and four (S_6, S_8, S_{10}, S_{11}) have a voltage rating of $2Vdc$. Switch S_9 is a bidirectional. Additionally, three sets of switches (S_1S_2, S_7S_8, S_{10} S_{11}) have been connected in complementary mode; as a result, it required just eight driver units.$v_0$represent the load voltage. The red line indicates the charging path of the capacitor, while the black line indicates the current path.

2.2 Working principle

Fig. 2 depicts an analysis of the proposed SCMGIT demonstrating the various output voltage level. Each voltage level's switching sequence is shown in Table I. to yield the proposed seven-level output voltage The power switches are labeled with the numbers "1" and "-" to indicate there on and off states, respectively. Capacitor charging/discharging and idle states are denoted by Δ/∇ and "-" respectively. The following modes describe the operation of each voltage level in greater detail:

Mode 1: $vo = 0$
This level can be reached by short-circuiting the switches S_1-S_4-S_5-S_{11} *(or* S_1-S_3-S_7-S_{10}*)* simultaneously. Capacitor C_1 *(or* C_2*)* is charged to Vdcin this mode. Fig. 2(a-b) depicts the analogous circuit for this level.

Mode 2: $vo = \pm 1Vdc$
The output voltage$vo = +1Vdc$ can be reached by switching S_2-S_3-S_7-S_{10} simultaneously. Subsequently, capacitor C_1 is charged to Vdc through the switches S_4-

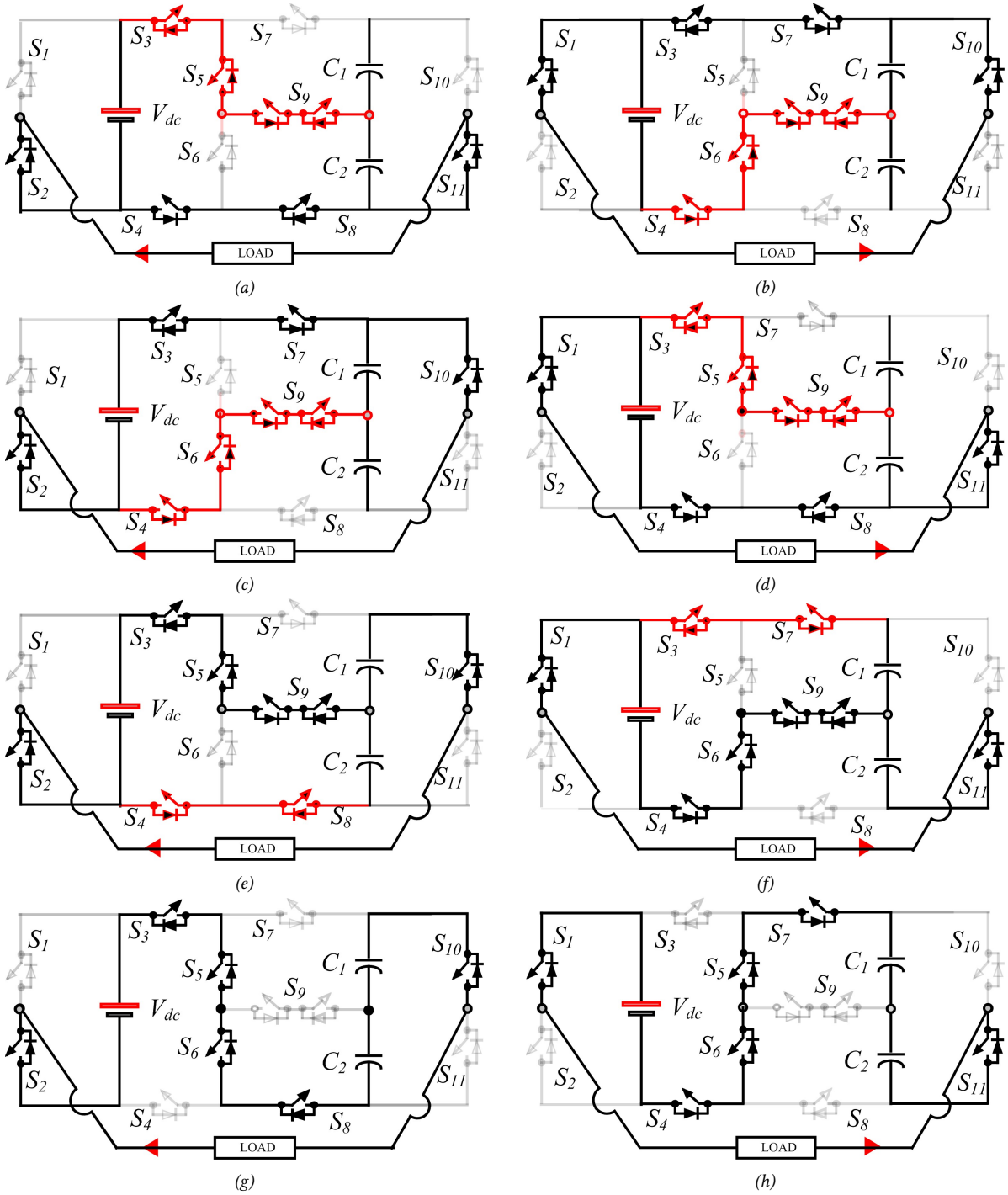

***Fig. 2**: Illustration of an equivalent circuit at various voltage levels (a) $vo = 0$, (b) $vo = 0$, (c) $vo = +1Vdc$ (d) $vo = -1Vdc$, (e) $vo = +2Vdc$, (f) $vo = -2Vdc$, (g) $vo = +3Vdc$, (h) $vo = -3Vdc$.*

S_6-S_9. Fig. 2(c) depicts the analogous circuit for this level. Similarly, the output voltage $vo = -1Vdc$ can be reached by switching S_1-S_4-S_8-S_{11} simultaneously. Capacitor C_2 gets charged to Vdc through the switches S_3-S_5-S_9. Fig. 2(d) depicts the analogous circuit for this level.

Mode 3: vo=$\pm 2Vdc$

To obtain this output voltage vo=$+2Vdc$ capacitor C_1 is drained in conjunction with Vdcthrough the switches S_2-S_3-S_5-S_9 -S_{10}.Capacitor C_2 gets charged to Vdc through the switches S_4-S_8. Fig. 2(e) depicts the analogous circuit for this level. Similarly, capacitor C_2 is drained in conjunction with Vdc through the switches S_1-S_4-S_6-S_9 -S_{11} to gets output voltage vo=$-2Vdc$. Capacitor C_1 gets charged to Vdc through the switches S_3-S_7. Fig. 2(f) depicts the analogous circuit for this level.

Mode 4: vo=$\pm 3Vdc$

***Table 1**: Switching Combination.*

Mode	v_0	C_1	C_2	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}
1	0	Δ	-	-	1	1	1	1	-	-	1	1	-	1
	0	-	Δ	1	-	1	1	-	1	1	-	1	1	-
2	$+V_{dc}$	Δ	-	-	1	1	1	-	1	-	-	1	1	-
	$-V_{dc}$	--	Δ	1	-	1	1	1	-	-	1	1	-	1
3	$+2V_{dc}$	∇	Δ	-	1	1	1	1	-	-	1	1	1	-
	$-2V_{dc}$	Δ	∇	1		1	1		1	1	-	1	-	1
4	$+3V_{dc}$	∇	∇	-	1	1		1	1		1	-	1	-
	$-3V_{dc}$	∇	∇	1	-	-	1	1	1	1	-	-	-	1

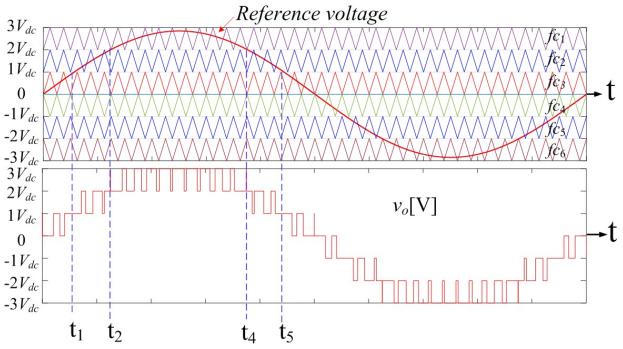

***Fig. 3**: Staircase output voltage.*

To obtain this output voltage vo=+3Vdc capacitors C_1 and C_2 are drained in conjunction with Vdc through the switches S_2-S_3-S_5-S_6-S_8-S_{10}. Fig. 2(g) depicts the analogous circuit for this level. Similarly, capacitors C_1 and C_2 are discharged in series with Vdc via the switches S_1-S_4-S_5-S_6-S_7-S_{11} to obtain an output voltage of vo=−3Vdc. A similar circuit at this level is depicted in Fig. 2(h).

2.3 Self-balancing and optimization technique of capacitors

In the proposed SCMGIT topology, the series-parallel action of all capacitors ensures that they are all self-balanced. The capacitors C_1 and C_2 are charged in parallel and discharged in series simultaneously in a single cycle, as illustrated in Fig. 2(a)-(h) and Table I. There are multiple charging times for each capacitor throughout an output voltage cycle, and the voltages of both capacitors can dynamically maintain the source voltage $Vdc$with some ripples. This function enables the voltages of the two capacitors to be balanced automatically.

The operating states indicated in Table I have been simplified into a single output voltage cycle, as illustrated in Fig. 3. The discharging time instant is denoted by t_1, t_2, t_3. In the positive half cycle, C_1 is responsible for the double voltage 2Vdc in the interval from t_2 to t_3 whereas C_2, C_3 are responsible for the triple voltage 3Vdc in the interval from t_2 to$\pi - t_3$. This same type of analysis is used for the negative half-cycle. The discharge time of capacitors is calculated as [10].

$$t_2 = \frac{\sin^{-1}(1/2)}{2\pi f} \tag{1}$$

$$t_3 = \frac{\sin^{-1}(2/3)}{2\pi f} \tag{2}$$

The discharge quantity of capacitors can be computed as

$$\Delta Q_{C1} = \int_{t_2}^{t_3} i_l \sin(2\pi f t)dt \tag{3}$$

$$\Delta Q_{C2} = \int_{t_3}^{\pi - t_3} i_l \sin(2\pi f t)dt \tag{4}$$

Thus, the optimum capacitance is computed as:

$$C_i \geq \frac{\Delta Q_{Ci}}{\Delta V_{Ci}} \tag{5}$$

where ΔV_C is the capacitor's voltage ripples. For a pure resistive(R) load, the voltage ripples between the two capacitors are indicated by the expressions (6) and (7)

$$\Delta V_{C1} = \frac{Vdc}{2\pi f RC_1}\left[3\pi - 2t_2 - 4t_3\right] \tag{6}$$

Similarly, for ΔV_{c2}

$$\Delta V_{C2} = \frac{Vdc}{2\pi f RC_2}\left[3\pi - 2t_2 - 4t_3\right] \tag{7}$$

Equations (7) and (8) imply that the two capacitors' voltage ripple is the same.

***Table 2**: Comparison with State-of-Art 7-Level SC Topologies.*

Ref.	N_{sw}	N_d	N_c	N_{dri}	$TSV + PIV_{pu}$	MBV/Gain	Gain	$F_{c/l}$	*CF*/Gain	
									$\alpha = 0.5$	$\alpha = 1.5$
[4]	10	-	3	10	6	1	3	3.28	3.71	4.57
[6]	8	2	2	8	6	1	3	2.85	3.28	4.14
[7]	9	1	2	8	6.66	0.66	1.5	2.85	3.33	4.28
[8]	16	-	2	14	5.33	0.33	3	4.57	4.94	5.71
[9]	8	2	4	8	6.66	0.66	1.5	3.14	3.61	4.57
[12]	14	2	2	14	5.33	1	3	4.57	4.95	5.71
[13]	10	4	2	10	8	1	3	3.71	4.28	5.42
[14]	12	-	2	11	5.33	0.66	3	3.57	3.95	4.71
[15]	10	-	4	8	6.66	0.33	1.5	3.14	3.61	4.57
[16]	16	-	2	14	5.33	0.33	3	4.57	4.94	5.71
[17]	10	-	3	8	5.3	0.66	1.5	3	3.37	4.13
[18]	13	-	3	13	5.7	0.66	3	4.12	4.55	5.37
[19]	9	2	3	9	5.66	1	3	3.28	3.69	4.49
[P]	12	-	2	8	5.3	0.66	3	3.14	3.52	4.27

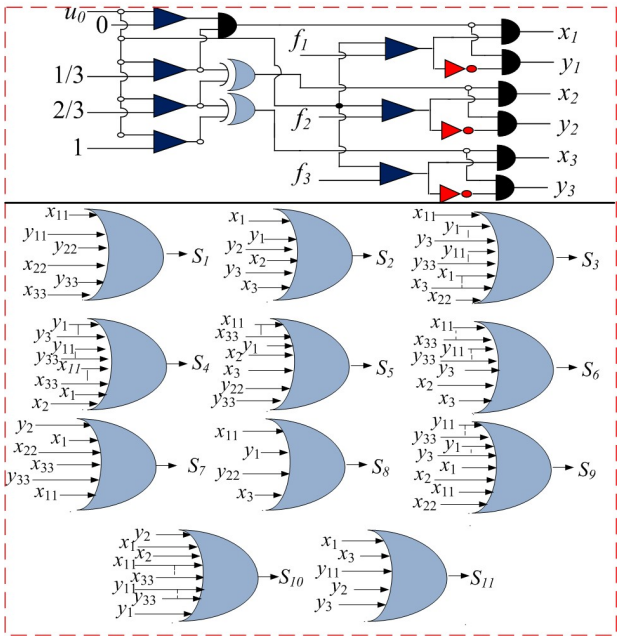

***Fig. 4**: Proposed 7-level Modulation scheme.*

3. MODULATION SCHEME

As seen in Fig. 4, the proposed 7-level SCMGIT is controlled using a logic-based PWM approach in which six triangular carrier signals are compared to a sinusoidal 50Hz reference signal to generate the pulses required by the proposed SCI's switches.

The triangular carriersf_1, f_2, and f_3 are triangular carriers for the positive half-cycle of the output voltage and f_4, f_5 and $f_6$are triangular carriers for the negative half-cycle of the output voltage, which continuously compared with the modulating signal u_0 to generates the switching pulses. The switching pulses developed by the logical OR operation is show in Fig. 4.

4. COMPARATIVE ANALYSIS

In order to obtain an assessment of the topology's overall characteristics, an analysis of selected topologies has been conducted. Because of this, a thorough evaluation of several elements of SCMGIT topologies has been conducted, including the maximum voltage stress, the needed number of components, voltage gain, total standing voltage (TSV), and overall cost. Further, the total number of components can be expressed in part counts per level, as specified by [9].

$$F_{c/l} = \frac{N_{sw} + N_d + N_c + N_{dri}}{N_l} \tag{8}$$

TSV_{pu} defined by the equation (10)

$$TSV\,pu = \frac{\sum TSV}{v\,\max} \tag{9}$$

where $v_{\max}$ Peak value of the load voltage

Cost function defined by the equation (11) [19]

$$CF = \frac{N_{sw} + N_d + N_{dri} + \alpha TSV_{pu}}{N_l} \tag{10}$$

Table 2 presents a comparison of the parameters being used with the currently available seven level inverters. The architecture that is described in [4][6] makes use of fewer components than the suggested one, as shown in Table II; nevertheless, the negative polarity is

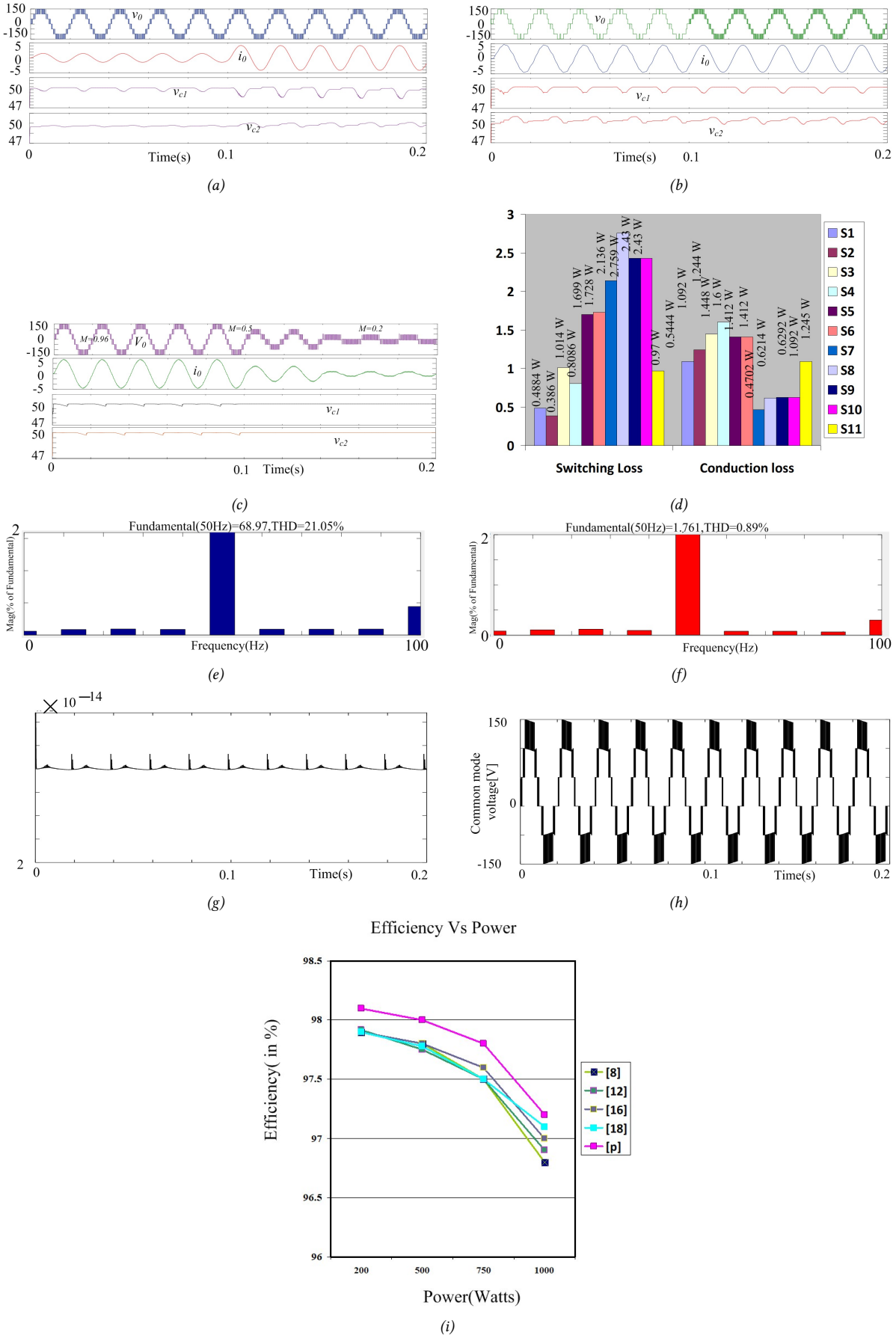

***Fig. 5**: Simulation results (a) step change load (b) change in switching frequency (c) change in modulation index (d) loss distribution graph (e) voltage THD (f) current THD (g)leakage current (h) common mode voltage (i) efficiency Vs Power.*

***Table 3**: Simulation and Experimental Parameters Rating.*

Parameters	Specifications
Input voltage (V_{dc})	50V
Switching frequency (f_r)	200 Hz, 2 kHz
Load	50 Ω,120 mH,30Ω50 mH
Fundamental frequency (f)	50 Hz
Capacitance ($C_1 = C_2$)	470
Modulation Index	0.95, 0.5, and 0.2
Power switches	MOSFET (IRF640)

generated at the backside of the circuit via an H-bridge. Counting the number of $F_{c/l}$, the work [6-7][9][15][17] uses the fewest switches but the greater number of diodes are in [6-7][9]. Additionally, the suggested topology does not incorporate any diode. There are two capacitors for the proposed one, however there are three capacitors employed in the works [4][17][18]and four capacitors in [9] [15]. On the other hand, the total switches' voltage, also known as *TSV*, is virtually identical across [8],[12],[14], [16-17] inverters and more in rest the topologies. Therefore, the proposed topology is more efficient than the inverters reported in [4], [6-7][9][13][15][18][19]. With the exception of [6-7][17], the *CF* factor of the suggested approach is lower in comparison to all of the other recommended topologies. Therefore, the proposed topology lends itself more favorably to the development of a 7-level SCMGIT.

5. LOSS ANALYSIS

The suggested topology comprises three forms of losses: switching losses, conduction losses, and capacitor losses.

5.1 Switching losses

The transitions of the switching states produce switching losses. This loss is assessed as [10].

The loss of power during power on

$$P_{sw,i,ton} = \frac{1}{6}\left(f_{sw} V_{sw,i} I_{on,i} t_{on}\right) \tag{11}$$

The loss of power during power off

$$P_{sw,i,toff} = \frac{1}{6}\left(f_{sw} V_{sw,i} I_{off,i} t_{off}\right) \tag{12}$$

where, V_{sw} denote the blocking voltage and I_{0n} denote the current flowing through the switches following their activation.

The times t_{on} and t_{off} represent the switch's on and off states.

As a result, the total switching losses$\left(P_{sw}\right)$of the suggested topology can be estimated as follows:

$$P_{sw} = \sum_{n=1}^{7}\sum_{i=1}^{12}\left(P_{sw,i,ton} + P_{sw,i,toff}\right) \tag{13}$$

5.2 Conduction losses

Conduction losses occur whenever the switching components (switches or diodes) are in the conduction path to communicate their unique voltage level [10].

$$P_{c,sw} = V_{on,sw} I_{sw,avg} + I^2 s_{w,rms} R_{on,sw} \tag{14}$$

$$Pc,d = V_{on,d} I_{d,avg} + I^2{}_{d,rms} R_{on,d} \tag{15}$$

where, $V_{on,sw}, V_{on,d}$: on-state voltage of switches and diodes, $I_{d,rms}, I_{d,avg}$: rms and average currents through the diodes, $I_{sw,rms}.I_{sw,avg}$: Average and rms currents through the switches, $R_{on,sw}, and\, R_{on,d}$: on state resistance of switches and diodes

Thus, aggregating these losses yields total conduction losses.

5.3 Capacitor ripple losses

The power lost due to voltage ripple is defined by [10]

$$P_{rip} = \frac{f}{2}\left(C_i \Delta^2{}_{C,i}\right) \tag{16}$$

Hence, inverter efficiency($\%\eta$) is expressed as follows:

$$\%\eta = \frac{Output}{Input} \times 100 \tag{17}$$

6. RESULTS AND DISCUSSIONS

6.1 Simulation Outcomes

For the purpose of verifying the proposed topology and modulation technique, simulations have been performed on a common platform consisting of MATLAB and PLECS. Table III contains the simulation parameters for the proposed SCMGIT.

Fig. 5(a) illustrates the output voltage and current waveforms under transient situations for RL loads. Despite the step-change in load, both the capacitors automatically maintained their self-balancing values around 50V. As expected, the suggested SCMGT maintains a constant output voltage. This result shows, the inverter appeared to be reliable under changing load conditions.

Fig. 5(b) illustrating the output voltage and current when the switching frequency is altered from 200Hz to 2 kHz. This result proves the proposed SCMGIT can respond to different modulation frequencies correctly. Fig.5(c) shows a change in modulation wave amplitude changes the output voltage. The output voltage drops from 7 to 5 level and 5 to 2 level as the Modulation index decreases from 0.95 to 0.5 and 0.5 to 0.2. Therefore, the inverter high dynamic performance is quickly revealed.

PLECS software has been used to define the steady-state efficiency of proposed SCMGIT. To investigate the power losses, the datasheet of IRFP460 MOSFETs has been imported. Fig. 5(d) shows the power loss distribution for a purely resistive load. The proposed SCMGIT achieves an overall efficiency of 98.05 percent. Fig 5(e-f) displays the results of the THD study for

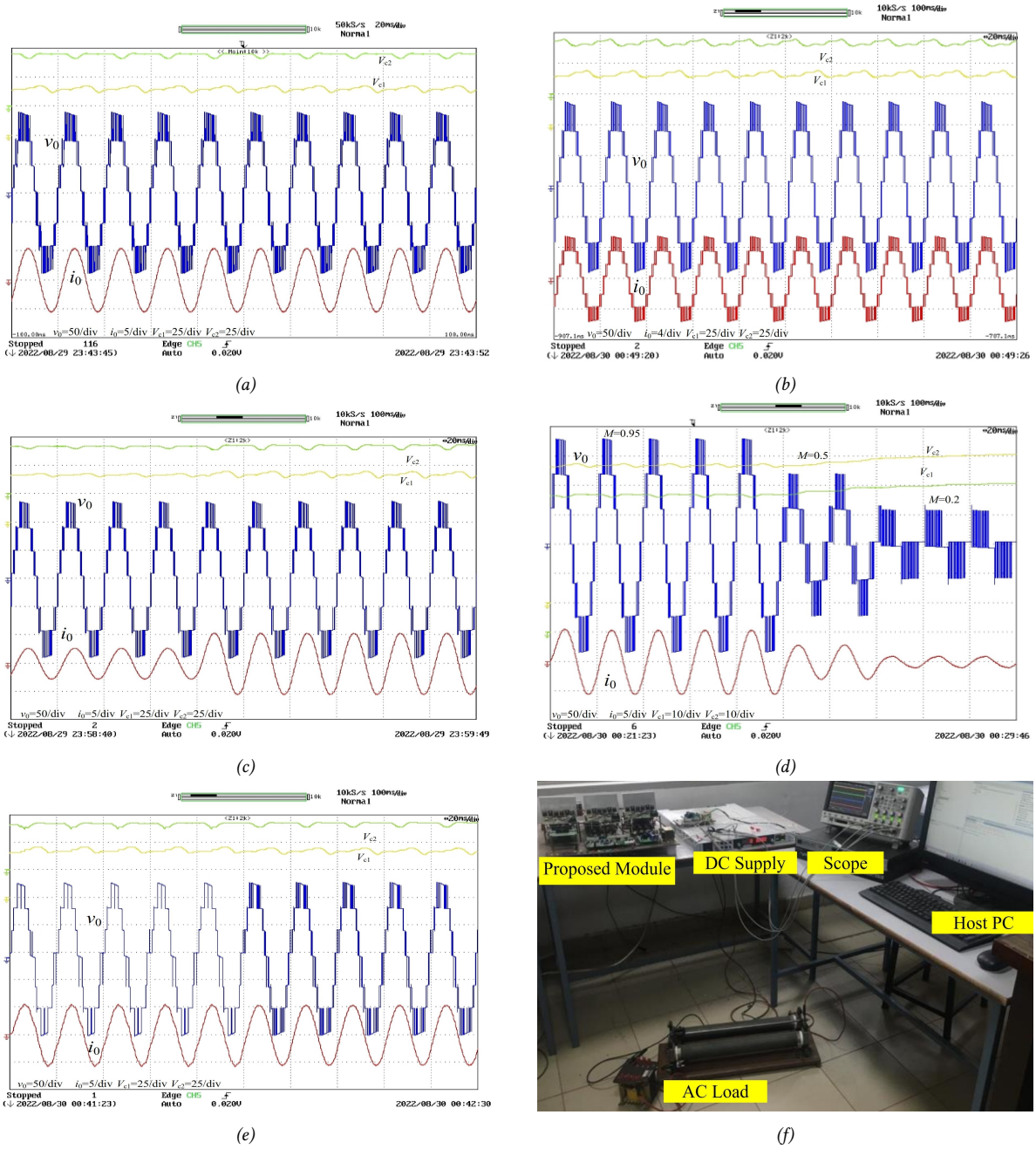

***Fig. 6**: Analysis for (a) RL-load (b) R-load (c) step change load (d) step change modulation index (e) step change switching frequency (f) Experimental prototype module.*

the suggested topology. Figure 5(g-h) also displays the common mode voltage and leakage current. The proposed architecture has little leakage current because it is not transformer less. Fig 5(i) shows a comparison of efficiency under different loads. It has been proven from the analysis that the recommended one is superior regardless of the other one when the load varies.

6.2 Experimental Outcomes

The proposed SCMGIT has been developed as a laboratory prototype in order to confirm the simulation outcomes. The experimental study's parameters are listed in Table III. Validation of the proposed SCMGIT has been performed in both transient and steady-state conditions.

The experiment has been initially conducted in a steady state with RL and R- load. With a 50V dc input source, the proposed SCMGIT generates a seven level, with the highest voltage level being 150V, showing that the proposed topology has a threefold voltage boosting gain. Additionally, the voltage over both capacitors is balanced to keep their voltage at 50V as illustrated in Fig.6(a-b).

Furthermore, the proposed SCMGIT have been carried

out with a resistive-inductive step change load. This fact implies that the capacitor's voltage ripples grow when the load decreases, and the staircase waveform of 7-level remains unchanged, as displayed in Fig.6(c).

Fig. 6(d) shows the range of modulation index (MI) function variations for the proposed 7L SCMGIT, which ranges from 0.95 to 0.5 and 0.5 to 0.2. In response to a reduction in the modulation index from 0.95 to 0.5 and then from 0.5 to 0.2, the levels dropped from 7 to 5 and 3 to 2 correspondingly. There are seven, five, and three stages where the peak voltage drops from 150V to 100V and then to 50V, respectively.

Fig. 6(e) depicts the voltage and current at the output when the switching frequency is varied from 200 Hz to 2 kHz. This study demonstrates that the proposed SCMGIT accurately responds to a wide range of modulation frequencies. The experimental prototype module is depicted in Fig. 6(f).

6.3 Practical Applications

As evident from both simulation and experimental outcomes concerning the suggested design, a 9-level waveform is produced with a voltage gain thrice that of the input voltage, considering potential applications for the recommended topology,various options have emerged from a comprehensive exploration of the literature on *SCMLIs*.

(a) High-Frequency A.C. Distribution:

The high-frequency alternating current (HFAC) power distribution system (PDS) has become increasingly popular due to its advantages in diverse applications, including telecommunication, spaceflight, and computer systems [23]. HFAC PDS offers reduced power conversion stages, smaller transformer sizes, and compact filters. Notably, this technology finds new applications in microgrids, buildings, and electric vehicles [24]. However, challenges with capacitor voltage imbalances limit the feasibility of standard MLIs with more than five levels [25]. To address this, SCMLIs are increasingly preferred for HFAC applications [26], eliminating the need for complex solutions and additional boost converters at low voltage sites.

(b) Photovoltaic (PV) Power Generation and Electric Vehicle (EV) Traction Systems:

Generating power from renewable sources like *PV* systems has limitations due to relatively low available power. To overcome this, voltage boosting is typically achieved through methods such as cascading PV modules, implementing dc-dc boost inverters, or using step-up transformers. Unfortunately, these techniques have drawbacks, including increased component count, costs, size, and power losses [26]. Nevertheless, the utilisation of SCMLIs provides benefits such as enhanced voltage amplification, automatic balancing of capacitors, precise waveforms for compliance with the power grid, and decreased need for filtering [27].

7. CONCLUSION

This paper proposed a new SCMGIT that incorporates the switched-capacitor concept. It enables the creation of seven distinct voltage levels, the highest of which is three times the dc source voltage. A comprehensive comparison with the 7-level SC topologies demonstrates the proposed SCMGIT relevance. Reduce voltage stress, voltage gain, cost function, and the part count per level reveal the proposed SCMGIT benefits. Additionally, with a single stage of power transfer, high efficiency is achieved. The simulation and experimental results confirm the theoretical investigation and indicate the suggested SCMGIT ability to dynamically working and loading circumstances without impacting the capacitors voltage.

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Kasinath Jena received his B.E. degree in Electrical Engineering from Fakir Mohan University, India, in 2002 and M. Tech degree from Centurion University, Bhubaneswar, India in 1915, India. He received the Ph.D. degree from the KIIT University Bhubaneswar, India in 2022. Currently Working as an Assistant professor in ARKA JAIN University, Jharkhand. His current research interests include, Multilevel Inverters and DC-DC converters, DC microgrid, Electric vehicles.

Dhananjay Kumar received his B.E. degree in Electrical and Electronics Engineering from the Lakshmi Narain College of Technology (LNCT), Bhopal, India; and his M.Tech. degree in Electrical Drives from the Maulana Azad National Institute of Technology (MANIT), Bhopal, India, in 2017, Completed his Ph.D degree from MANIT Bhopal, India, in 2022. Working as assistant professor in Government Engineering College Siwan, Bihar. His current research interests include multilevel inverters and DC-DC converters.

Gangadhar Dhal received the bachelor's degree and Masters degree in electrical engineering from BPTU in 2015 & 2017 respectively, and he is pursuing the Ph.D from KIIT, University India. He is currently working as an Professor in the Department of Electrical Engineering, Bhadrak Institute of Engineering and Technology, Bhadrak, India. His current research interest includes Multilevel Inverters and DC-DC converters, Electric vehicles.

Pradeep Kumar Sahu is working as an associate professor in the School of Electrical Sciences, KIIT University, Bhubaneswar. He received a Ph.D. degree from the National Institute of Technology, Rourkela in 2015. His research interests are grid-connected PV systems, electric vehicles, power quality, advanced power electronics converters, and soft-computing.

Lipika Nanda is presently working as Assistant Professor (II) in School of Electrical Engineering, KIIT University, an Institute of Eminence. Prof. Nanda had completed my Ph.D. in the area of Hardware Realization on Multilevel Inverter in the year of 2019. Her working areas are Power Electronics, Electrical Drives, Solar Photovoltaics and Renewable Energy Sources.