Performance Analysis of Distance-Based Wireless Transceiver Placement for Wireless NoCs with Deterministic Routing

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ABSTRACT

This research analyzes the impact of wireless transceiver subnet clustering on a hundred-core mesh-structured WiNoC architecture. The study aims to examine the effects of distance-based wireless transceiver placements on transmission delay, network throughput, and energy consumption in a mesh Wireless NoC architecture with a hundred cores, particularly under the X-Y, West-First, Negative-First, and North-Last routing strategies. This research investigates the impact of positioning radio subnets at the farthest, farther, nearest, and closest positions within an architecture featuring four wireless transceivers. The Noxim simulator was used to simulate the analyzed wireless transceiver placements on the hundred-core mesh-structured WiNoC designs, with the objective of validating the results. The architecture with the wireless transceiver positioned at the midway proximity (nearer and further) delivers the best performance, as evidenced by the lowest latencies for all evaluated deterministic routing algorithms, corresponding to the simulation outcomes.

Keywords: Distance-based Optimization, Wireless Transceiver, Optimal Placement, Wireless Network-on-Chip, Deterministic Routing Algorithm

1. INTRODUCTION

In the preceeding years, there has been a growing importance in the utilization of on-chip interconnect topologies as a means of communication for chip multiprocessors. This trend is supported by various studies, including those conducted in [1–3]. Recent advancements in semiconductor technology have enabled the successful integration of integrated circuits incorporating even more processing components into a chip multi processor architecture. Furthermore, several integrated chip project using Network-on-Chip (NoC) technology, comprising of many processing cores, have been developed and utilized in various prototypes such as SCORPIO [4], MIT RAW [5], Xeon Phi [6] and Intel TILERA [2].

The issue of wire delay poses a notable obstacle for on-chip network systems, for the most part in the context of extensive on-chip interconnects, due to its potential to significantly affect the overall performance of the network. The standard wired Network-on-Chip (NoC) infrastructure is facing constraints due to the growing number of computing cores, as it heavily depends on multiple hop far reaching communication. Consequently, this leads to an architectural design that uses a greater amount of power and has elevated latency. Therefore, in order to tackle the issues related to significant propagation delay and multiple-hop long-distance communication between processing cores, Wireless NoCs introduce flexibility in communication by enabling direct links between distant nodes, thus potentially reducing hop count and latency.

The challenge posed by wire delay is importance in chip-based network architecture, especially while addressing expansive on-chip communication systems, as it can significantly affect the entire network capabilities and performance [7, 8]. As quantity of processing cores continues to grow, the traditional wired NoC architecture faces limitations due to its dependence on long-distance multi-hop communication. Consequently, this results in an architecture that use more power and demonstrates increased latency. Therefore, to tackle challenges related to elevated latency in signal propagation and long-distance multi-hop communication between processing cores, computer architects and researchers have introduced the design of Wireless NoC (WiNoC) interconnect as a viable solution [9, 10].

This approach requires the integration of one-hop wireless transmission to allow far reaching communication among processor cores, as referenced in multiple studies [11–16] for its efficacy and scalability. The WiNoC setup incorporates integrated transceivers, facilitating an immediate wireless channel for the transfer of packets over long distances on the chip, as supported by several research findings [12, 17, 18]. The effectiveness of the WiNoC framework is significantly influenced by several importance network features, such as the arrangement of its topology, the management of data

Manuscript received on November 8, 2023; revised on March 5, 2024; accepted on March 29, 2024. This paper was recommended by Associate Editor Nutapong Somjit.

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Digital Object Identifier: 10.37936/ecti-eec.2024222.251668

flow, and routing mechanisms, with various studies highlighting their critical impact [19–21].

Mrunalini et al. [22] designed and simulated a fork-shaped, planar plasmonic nano-patch antenna employing graphene on an SiO2/Si substrate. This antenna can be integrated into transceivers operating at THz frequencies, with a range from 0.5 THz to 2.6 THz.Through simulations in the THz band, the proposed antenna's performance as the inter/intra-chip wireless link was examined by numerically obtaining its transmission coefficient signal characteristics between two on-chip antennas. These antennas act as a receiver and transmitter, enabling the THz communication in short-range between multi-core processors that integrated on the same substrate in the WiNoC. The results were achieved by the placement of antennas in a broadside orientation, allowing communication within intra-chip transmission coefficients that covering from -20 dB to -60 dB, whereas at the same time can sustain the bandwidths of up to 0.13–0.2 THz. Additionally, the study explored the impact of performance radiation of the presented antennas as the distance increased, alongside the reconfigurable nature of the graphene, which varies with chemical potentials from 0.1 eV to 0.5 eV. The investigated antenna achieved a radiation efficiency and maximum gain of 58% and 3.89 dB, respectively, at 1.83 THz when a chemical potential of 0.1 eV was implemented.

Ramesh et al. [23] proposed a novel neural mapping model with a reinforcement learning approach called NeurMap3D to design application-specific 3D NoC-based integrated circuit. Furthermore, the neural congestion-aware Through-Silicon via placement and application mapping) approach is presented, which not only addresses application mapping but also incorporates TSVs placement and load balance across the TSVs for the specific application. Additionally, to decrease the CPU execution time for the NCTPAM algorithm, a partial model parameter update mechanism is integrated into the design. Experimental results indicate improved performance in terms of minimizing communication cost, load balancing across TSVs and energy consumption, highlighting the potential of our approach to enhance the efficiency of these synthesized network architectures.

Gulzari et al. [24] conducted a comparative analysis of 2D mesh topologies with additional communication links for on-chip networks, emphasizing their systematic and scalable design structures. The investigation delves into understanding the implications of integrating extra communication pathways on the efficiency and effectiveness of on-chip mesh network designs, aiming to uncover their role in enhancing or potentially hindering the performance metrics of these architectures. The comparative analysis delves into a detailed evaluation of several critical aspects. It assesses performance attributes, which may include metrics such as speed, reliability, and efficiency, to understand how different systems or components operate under various conditions. This comprehensive approach ensures a thorough understanding of the systems' overall performance and practicality. Among the mesh topologies compared, the link design of the d-Torus topology was found to achieve high performance, albeit at the cost of increased communication expenses. This study furnishes a detailed framework that assists designers in navigating the complex landscape of available topologies, guiding them towards the selection of the most fitting architecture for their unique design specifications. This tailored approach enhances the overall design process, leading to more effective and optimized outcomes.

Dehghani et al. [25] introduce a strategy for dynamic task mapping and scheduling that is both deadline-aware and energy-efficient, specifically designed for HWNoC-based multicore systems. Leveraging core utilization thresholds and the laxity times of tasks, this method aims to reduce communication energy consumption while ensuring the deadlines of real-time application tasks are met. This approach focuses on minimizing energy usage for communication by applying key utilization limits and the flexibility periods of tasks, all while guaranteeing that the deadlines for tasks in real-time applications are achieved. Cycle-accurate simulations were employed to assess the efficacy of this method against the other approaches, focusing on several performance metrics. These metrics included the energy used in communication, how often deadlines were missed, the delay in communication, and the additional time required for execution. The experimental findings validate that this strategy is highly competitive compared to other available methods.

Reddy et al. [26] introduced a methodology aimed at enhancing the efficiency of multiprocessor systems on chip by integrating adaptive routing utilizing the Bat algorithm. The architecture incorporates a 5-stage pipeline router that efficiently forward packets in an adaptive manner towards their intended destinations. Leveraging the Bat algorithm optimizes routing paths to ensure efficient packet transmission to their designated endpoints. Experimental evaluation encompassed various Network-on-Chip (NoC) configurations, including sizes of 6x6 and 8x8, employing multimedia benchmarks. These were compared against alternative algorithms and implemented on a Kintex-7 FPGA board. Simulation results demonstrate that the proposed algorithm significantly reduces latency and enhances throughput compared to traditional adaptive algorithms.

The primary challenge addressed in this study is to investigate and optimize the placement of wireless transceivers within a Wireless Network on Chip (NoC) architecture, particularly in systems employing deterministic routing algorithms. The study aims to determine how varying distances between transceivers, as well as their strategic positioning, can significantly influence key performance indicators such as latency, throughput, energy efficiency, and wireless utilization. This investigation is critical for advancing the design and efficiency of multicore and manycore systems, where

optimal wireless communication pathways are crucial for enhanced WiNoC performance

. The structure of the paper is as follows: beginning with Section 2, it includes an outline of the hundred core mesh-structured WiNoC network structure, the model of the wireless transceiver hub, and the deterministic routing mechanism. Section 3 offers a detailed account of the methodological framework used in the Noxim simulation setup. Following this, Section 4 engages in an examination of the experimental results and their analysis. Finally, Section 5 concludes the paper and suggests directions for future research.

2. MESH-STRUCTURED WIRELESS NOC WITH HUNDRED-CORE

2.1 Mesh-structured WiNoC Architecture

The WiNoC is a hybrid interconnection for Network-on-Chip systems which aims to alleviate the considerable latency related with the traditional wired communication. This is achieved by including both the wired and wireless links, resulting in the foundation of efficient wireless on-chip communications [11–16, 27–29].

Additionally, the emergence of integrated wireless transceiver [17, 30] and millimeter-wave CMOS-compatible antennas [31, 32] has highlighted the possibility of WiNoC as a viable alternative to traditional NoC designs [33]. The configuration of component interconnections in a WiNoC that has a substantial influence on both the performance of the system and the associated architectural expenses. Consequently, it is a crucial matter that must be taken into account during the design process.

The architectural design of a WiNoC infrastructure is affected by many aspects, such as the physical arrangement, interconnections between processor cores, the quantity of wireless channels, and the distribution of wireless transceivers throughout the WiNoC system [34–36]. The diagram shown in Figure 1 depicts a mesh-structured WiNoC topological design. It consists of a 10×10 grid layout with hundred cores and four wireless transceivers spread over the Mesh-structured WiNoC architecture. The integration of wireless transceivers into the Network-on-Chip (NoC) tiles facilitates direct connection between the processor cores that are spatially distant from each other, hence enabling wireless single-hop communication.

Transceivers hub are pivotal components in wireless communication systems, as they facilitate the transmission of data at high speeds and with high bandwidth [37–39]. Apart from requiring high bandwidth, an on-chip WiNoC network system with minimal energy consumption is highly desirable. Achieving this goal can be accomplished through the implementation of an effective radio transceiver design. Figure 2 presents a visual representation of the key components comprising the hub transceiver. The transmitting section of the wireless transceiver consists of a serialiser, an on-off keying (OOK) modulator, along with power amplifier. In

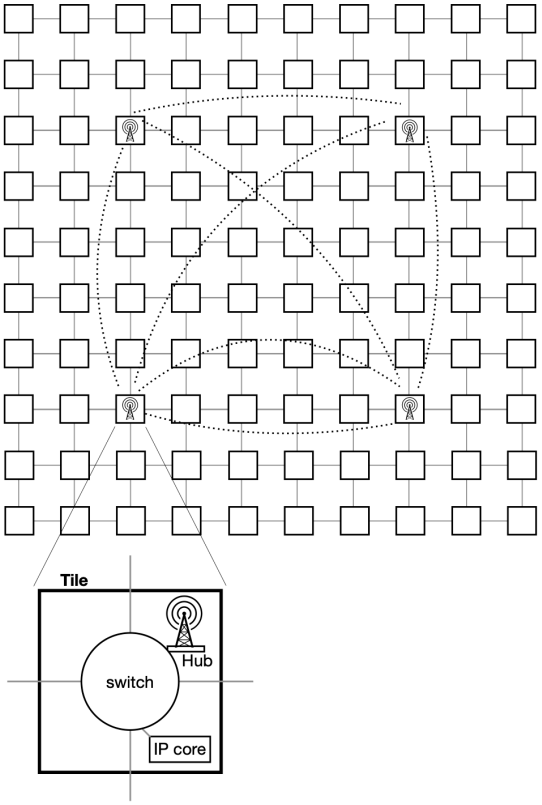


***Fig. 1**: Hundred cores mesh-structured Wireless NoC design with four wireless transceiver*

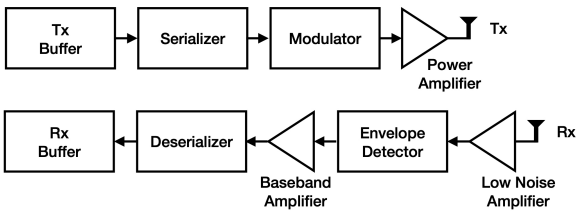


***Fig. 2**: A transceiver utilizing OOK modulation technique.*

contrast, the receiver section is comprised of low-noise amplifier (LNA), envelope detector, baseband-amplifier, and the demodulator-deserialiser.

2.2 Routing Algorithm with Deterministic Approach

In CMP applications where buffering resources are limited due to strict latency requirements, a deterministic routing approach is a preferred scheme [40-42]. This routing approach employs wormhole routing and breaks down packets into flow control units called flits. Each flit within a packet carries the necessary routing details in its header to navigate through the WiNoC network. Should there be network congestion causing a flit's header to be obstructed, all following flits are required to wait at their specific tile nodes until the congestion clears. The mesh-WiNoC topological structure is highly suitable

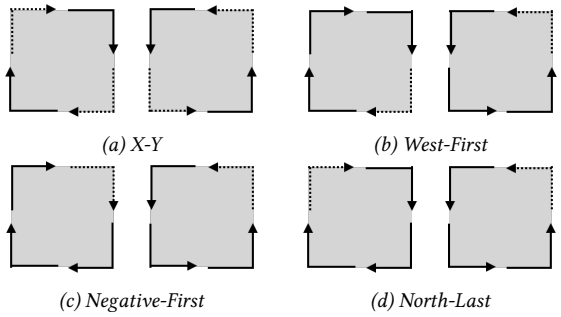


***Fig. 3**: The possible directions for turning in deterministic routings algorithm.*

***Table 1**: Noxim Experimental Setup*

Specification	Details
IP cores	100
Clock frequency	1 GHz
Technology	65 nm
Wireless transceiver	4
Emplacement	Furthest, Further Nearer, Nearest
Simulation Time	100, 000 (Cycles)
Wireless Data Rate	16 Gbps
Routing Algorithm	X-Y, West-First, Negative-First, North-Last

for the investigated deterministic routing approaches as it enables the establishment of the minimum distance feasible pathway between transmitting computing cores. Moreover, this technique eliminates the need for tables and ensures prevention of deadlock and live-lock issues throughout the chip network.

Figure 3 demonstrates the possible directions available in X-Y routing. The solid lines represent valid directions that can be taken, while the dashed lines indicate prohibited turns.

For instance, using the XY routing method, a packet can be initially routed in the X-orientation, followed by the Y-orientation, to arrived its intended processing core. The West-first routing algorithm prioritizes routing a packet in the west orientation first, if it is a effective orientation, while allowing for the selection of any shortest path if the west direction is not viable. In the negative-first routing scheme, if the destination of a data packet lies in any negative-axis direction (either vertical or horizontal) along with another orientation, the packet is initially directed in the direction of the negative-axis orientation and subsequently towards the other direction. Finally, the North-Last routing scheme required that when traffic is heading towards the north, the north direction should be chosen as the last option, while allowing for all possible shortest paths when traffic is headed south. However, for traffic going north, only a single path is permitted.

These routings represent the directional changes that data packets can make within the mesh network's grid structure. To manage and optimize the flow of data this algorithm plays a crucial role in controlling network traffic by classifying these turns into two distinct categories: allowed turns and prohibited turns. The classification is based on various factors, such as reducing congestion and avoiding deadlock situations in the network, ensuring efficient and reliable data transmission across the WiNoC system.

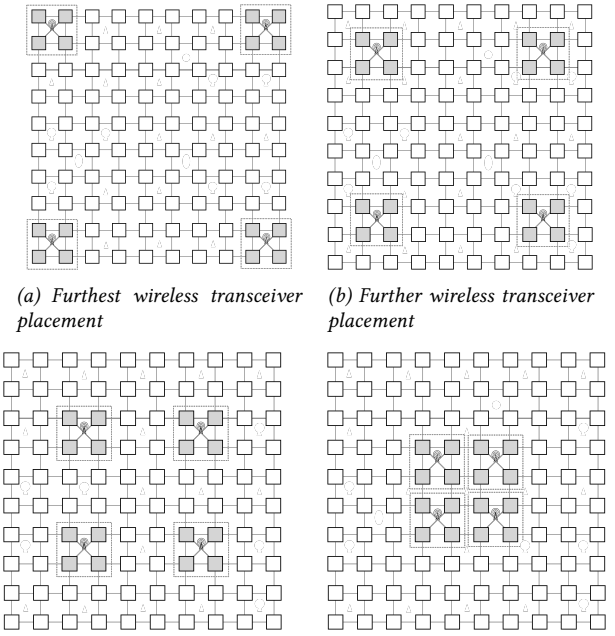
3. EXPERIMENTAL SIMULATION SETUP

The performance of the explored wireless transceiver emplacement based on distance has been evaluated on the hundred cores mesh-structured Wireless NoC topological structure employing the open source cycle-accurate network-on-chip simulator, Noxim [43]. By using a deterministic wormhole-based routing method, mesh-WiNoC topologies may provide wireless transmission through the Noxim simulator. In order to model various wireless transceiver placement designs into Wireless NoC infrastructure, Noxim was also built to provide placement configuration adaptation. Furthermore, Noxim provides an accurate representation of latency during crossbar arbitration and the process of selecting routing paths. This accuracy is achieved by incorporating actual data derived from the design of a router prototype. This approach enables a detailed representation of the router's behaviour under various operational conditions.

Table 1 displays the simulation setup parameters that were employed in this study. Four different wireless transceiver placement configurations such as furthest, farther, nearer, and nearest were used in the simulations, as shown in Figure 4. The use of various routing algorithms—X-Y, West-First, Negative-First, and North-Last—suggests a comprehensive study into the efficiency and effectiveness of different routing methodologies under the same network conditions. By employing multiple algorithms, the experiment can provide insights into which routing strategy performs best in a WiNoC environment with the given configuration.

The selection behind these routing offers several advantages, including deadlock avoidance, as it is specifically designed to prevent the formation of cyclic dependencies, which greatly enhances the reliability of the network. Additionally, this model boasts simplicity, as the routing decisions it requires are relatively straightforward to implement, particularly in hardware contexts. Furthermore, its deterministic nature contributes to predictable performance, ensuring a consistent and reliable operation within the network system.

Every simulation in the placement on Wireless NoC system was performed a total of 100,000 times to get a state that was stable. Random traffic distributions were used in the simulation, giving each tile core an equal chance of sending a packet of information to any other tile core.



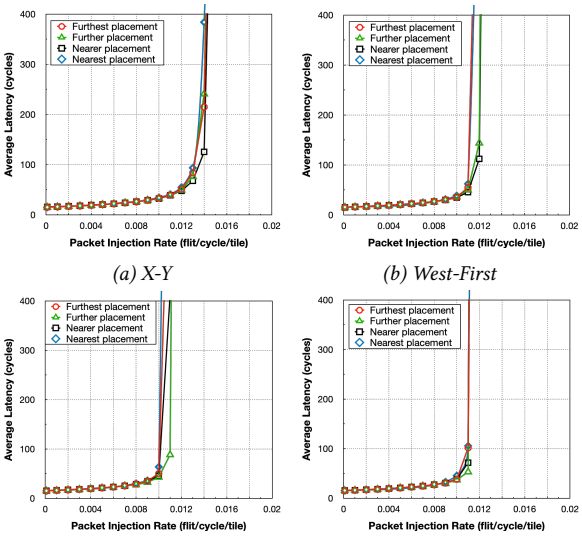
(a) Furthest wireless transceiver placement

(b) Further wireless transceiver placement

(c) Nearer wireless transceiver placement

(d) Nearest wireless transceiver placement

***Fig. 4**: Hundred cores mesh-structured WiNoC architecture with various distance proximity of wireless transceiver placements.*



(a) X-Y

(b) West-First

(c) Negative-First

(d) North-Last

***Fig. 5**: The effects of WiNoC latency for various wireless transceiver placement proximity under various deterministic routing algorithms.*

***Table 2**: Average latency at saturation load under various deterministic routing algorithms.*

	Average latency (cycles)			
	Furthest	Further	Nearer	Nearest
X-Y	84	76	68	93
W-F	55	50	46	62
N-F	50	43	45	64
N-L	102	53	72	106

4. RESULT AND ANALYSIS

This section evaluates the performance of a hundred cores mesh structured WiNoC with four wireless transceiver hub placements, taking random distribution workload into account. The effectiveness of the investigated system is evaluated using measurements of performance including network throughput and communication delay. These metrics are frequently employed for evaluating and illustrating the performance of the on-chip WiNoC system. In addition, the study was conducted on the wireless usage and energy consumption of several WiNoC designs with varied wireless transceiver positions according to the proximity of distance.

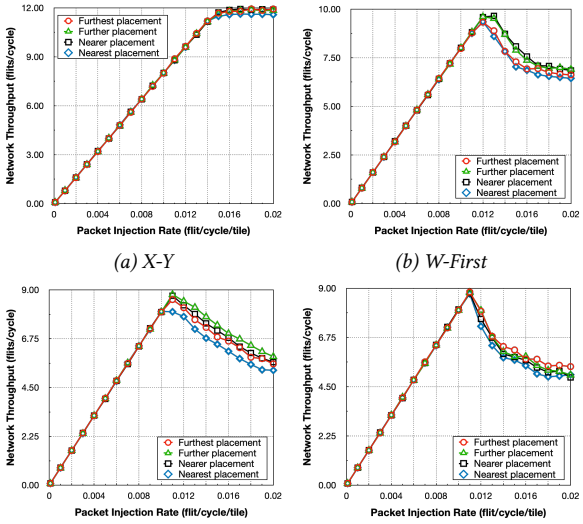
4.1 The Effect of WiNoC Communication Latency

Latency is the aggregate count of clock cycles necessary for a packet to traverse the WiNoC network, originating from its source and reaching its designated destination. Figure 5 illustrates the effect of latency on wireless transceiver placement, considering numerous routing algorithms, namely X-Y, West-First, Negative-First, and North-Last. Meanwhile, Table 2 summarizes the average latency at saturation PIR in cycles at the saturation load attained in this work for the furthest, further, nearer, and nearest placements under various routing algorithms.The graph illustrates the correlation between the injection packet load and the accompanying communication latency. The presented graphs exhibit a variety of delay values, each characterized by a distinct curvature.

The delay experiences a consistent increase as the packet injection rate (PIR) of the given load increases. Nevertheless, when subjected to greater loads, the latency experiences an apparent rise in the presence of PIR, indicating that the WiNoC system has established a state of saturation.In general, the wireless transceivers in all examined placements exhibit saturation at comparable points of PIR saturation: 0.013 (X-Y), 0.011 (West-First), 0.010 (Negative-First), and 0.011 (North-Last) flit/cycle/tile. However, the placement located in the middle demonstrates better results in terms of latency. Specifically, it requires 68 cycles for X-Y routing and 46 cycles for West-First routing. It is noteworthy that the placement at a greater distance exhibits the lowest delay, as evidenced by 43 cycles for Negative-First routing and 53 cycles for North-Last routing.

4.2 The Effect of the Throughput Saturation

The term network throughput is used to describe the speed at which data packets move across the WiNoC system. Moreover, throughput saturation defines the specific point where the network's capacity is fully utilized, aligning the throughput with the demands of the workload. At this saturation point, the WiNoC system becomes less effective in handling the transmission of the



(a) X-Y (b) W-First

(c) Negative-First (d) North-Last

***Fig. 6**: The effects of WiNoC network throughput for various wireless transceiver placement proximity under various deterministic routing algorithm.*

***Table 3**: Throughput at saturation load under various deterministic routing algorithms.*

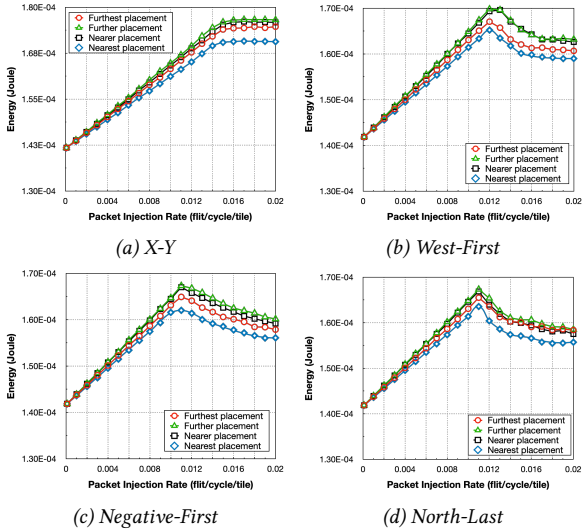
	Network throughput (flits/cycle)			
	Furthest	Further	Nearer	Nearest
X-Y	10.43	10.42	10.35	10.41
W-F	8.77	8.83	8.81	8.76
N-F	7.98	7.99	7.98	8.01
N-L	8.82	8.80	8.77	8.75

data packets it produces.

Figure 6 illustrates the impact of WiNoC throughput on diverse wireless transceiver placements, including several routing algorithms such as X-Y, West-First, Negative-First, and North-Last. Meanwhile, Table 3 summarises the WiNoC network throughput at PIR saturation in flits/cycle attained in this investigation for the furthest, further, nearer, and nearest placements under various routing algorithms. The figure shows how the throughput of the WiNoC system changes as the PIR (Packet Injection Rate) progressively increases. For closer placements of the wireless transceivers, the saturation throughput levels are 10.35 flits per cycle for the X-Y routing algorithm and 8.81 flits per cycle for the West-First routing algorithm. Additionally, for the farthest wireless transceiver placement, the saturated network throughput rates are 7.99 flits per cycle for the Negative-First routing algorithm and 8.80 flits per cycle for the North-Last routing algorithm.

4.3 The Effect of Energy Consumption

The quantity of electrical power used by the various elements and functioning that make up the WiNoC architectural network is indicative of its energy usage. Figure 7 illustrates how energy use in WiNoC is affected,



(a) X-Y (b) West-First

(c) Negative-First (d) North-Last

***Fig. 7**: The effects of energy utilization for various wireless transceiver placement proximity under various deterministic routing algorithm.*

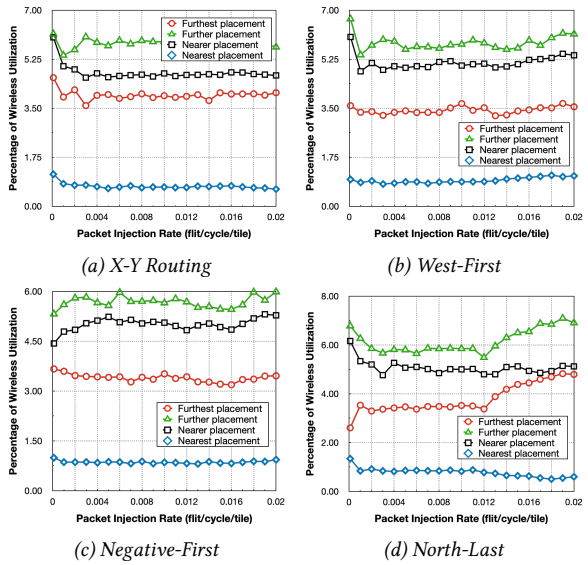
***Table 4**: Energy consumption at saturation load under various deterministic routing algorithms.*

	Energy consumption ($\times 10^{-4}$ Joule)			
	Furthest	Further	Nearer	Nearest
X-Y	1.70	1.72	1.71	1.67
W-F	1.65	1.67	1.67	1.63
N-F	1.63	1.65	1.64	1.62
N-L	1.65	1.67	1.67	1.64

highlighting how the positioning of wireless transceivers influences power consumption in conjunction with different routing algorithms. This information is derived from simulations run on Noxim. Meanwhile, Table 4 summarises the WiNoC energy consumption at the saturation load acquired in this investigation for the furthest, further, nearer, and nearest placements under various routing algorithms. Regarding energy usage, when the wireless transceiver is placed close to the source, it results in energy utilization values of 1.67×10^{-4} J for the X-Y routing strategy, and 1.77×10^{-4} J for the West-First routing approach. Moreover, for Negative-First and North-Last routing, the energy consumption is 1.65×10^{-4} J and 1.67×10^{-4} J accordingly, with the further placement of the wireless transceiver.

4.4 The Effect of the WiNoC Wireless Usage

The utilization of wireless elements within an on-chip network system is a measure of how effectively the wireless components, such as transceivers, are used to transmit data through the wireless channel.Achieving peak performance in WiNoC systems depends heavily on the effective management and use of these wireless elements, emphasizing the significance of their strategic implementation. In a WiNoC configuration, the percentage of wireless usage denotes the amount of



(a) X-Y Routing *(b) West-First*

(c) Negative-First *(d) North-Last*

***Fig. 8**: Wireless usage for various wireless transceiver placement proximity under different deterministic routing algorithms.*

***Table 5**: The percentage of wireless usage at load saturation under various deterministic routing algorithms.*

	Percentage of wireless usage (%)			
	Furthest	Further	Nearer	Nearest
X-Y	3.98	5.97	4.69	0.72
W-F	3.43	5.93	5.07	0.88
N-F	3.52	5.66	5.06	0.85
N-L	3.50	5.86	5.02	0.88

wireless capacity that is being utilized efficiently. Figure8 depicts the percentage of the total of wireless usage in a hundred-core mesh-structured WiNoC, showing the impact of various wireless transceiver placements on different routing algorithms.

Additionally, Table 5 provides a detailed account of the wireless utilisation percentages at saturation load for the WiNoC, which includes the results for the most distant, more distant, closer, and closest transceiver placements across numerous routing algorithms. In the scenario with optimal performance, the percentage of the total of wireless utilisation for nearer placement of the wireless transceiver is 4.69% and 5.07% for X-Y and West-First routing, respectively. Furthermore, 5.66% and 5.86% respectively for the Negative-First and North-Last routing algorithm for the case of further wireless transceiver placement.

5. CONCLUSION

The objective of this research was to explore the implications of the distance-based wireless transceiver placements specifically the furthest, further, nearer, and the nearest on the hundred cores mesh WiNoC architectural framework, using deterministic routing algorithms. The findings from the simulation suggest that positioning the wireless transceiver at an intermediate distance, either nearer or further, within the architecture results in the best performance and the least latency for deterministic the routing algorithms tested. Positioning the wireless transceiver closer offers optimal performance in both X-Y and West-First routing. On the other hand, the routing algorithms that show a preference for the further placement of the wireless transceiver include Negative-First and North-Last. Subsequent studies intend to delve into the assessment of network congestion under different traffic loads, and how transceiver placement and deterministic routing influence congestion levels. Furthermore, the study of adaptive routing using multiple wireless channels in the mesh Wireless NoC framework gains importance with an increased count of wireless transceivers, such as 8 and 16, to explore their impact.

ACKNOWLEDGEMENT

The authors gratefully acknowledge the support received from the Osaka Gas Foundation for Cultural Exchange (OGFICE) under grant number OGFICE INT/F02/OSAKA-IG/86193/2024. Additionally, we would like to thank the Faculty of Engineering at Universiti Malaysia Sarawak for their support with the Antenna Laboratory facilities.

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