Development of an On-Grid Low-Voltage Battery Energy Storage System with Balancing Dual-DC-Voltage Quasi Single-Stage Converter

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ABSTRACT

With low-voltage (LV) battery energy storage systems (BESSs), the quasi single-stage converters (QSSCs) are utilized to reduce power consumption in two-stage conversion systems. Despite a good waveform quality of applying multilevel converters, the unbalancing voltage problems is possible to be contributed, such as decrease in grid quality and complexity in pulse-width-modulation (PWM). In this paper, it is the main challenge to solve these problems for developing the on-grid LV BESS with the QSSC. Balancing voltage control is proposed to control the dc-dc converter. As a result, the dual dc voltages are equalized. The system waveform quality and power quality can be improved. The PWM stage is then symmetrical and simplified. For more simplicity, the two-inphase carrier-based PWM is applied. The continuous non-sinusoidal scheme is preferred to not only provide the full dc utilization, but also improve the grid waveform quality in addition to the improvement from the proposed control method. Besides, the powers are simply controlled using the basic of the current vector control and decoupling from the balancing voltage control, resulting in the grid-connected enhancement without affecting the waveform quality. A 10-kW-microgrid-scale BESS is employed to validate the feasibility of the proposed system and its superiority over conventional systems.

Keywords: On-Grid Battery Energy Storage System (BESS), Quasi Single-Stage Converter (QSSC), Balancing Voltage Control, Symmetrical Pulse-Width-Modulation (PWM), Current Vector Control

1. INTRODUCTION

Energy storage systems (ESSs) play an essential role in a "smart" and "green" grid to manage energy and enhance power quality due to a high expansion of renewable energy sources. It can be classified into four categories i.e., mechanical, electrochemical, electric charge, and magnetic field types [1]. The type of the electrochemical energy storage offers significant merits compared to the other types, such as large quantities for storing energy, high energy density, and fast response time, etc. Battery ESSs (BESSs) have become suitable for grid applications, due to the aforementioned benefits in a relatively small space. Moreover, the performance and lifetime of BESSs have improved and increased continuously with the ability of quicker and longer releasing energy, as well as more storing energy, while their cost has decreased. The BESSs have been therefore one important part of the consistent supplies to ensure the reliability and the stability of the utility grid [2-4].

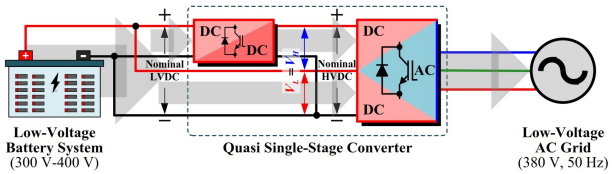

***Fig. 1**: An on-grid low-voltage (LV) battery energy storage system (BESS) with the proposed balancing dual-dc-voltage quasi single-stage converter (QSSC).*

The BESSs have been widely used in various grid-connected applications, especially for microgrids as behind-the-meter applications (small-scale power generating, ~1kW to ~10 MW, and low voltage, ~400 V). The particular functions are serviced for the end user to enhance customer experience [5,6], such as higher power quality, higher power reliability, retail electric energy time shift, etc. To comprehensively function these features, the configurations of the low-voltage (LV) on-grid BESSs are mainly divided into two conversion structures [7-12]: single-stage conversion systems and two-stage conversion systems. For the single-stage conversion systems, the BESS with the dc power and the grid with the ac power can be connected and flow their powers through only one-stage converter, which is herein called dc-ac converter. Such a one-step conversion not only provides less conversion power loss, but also simplifies the operation and control algorithms. However, the only problem of this system is the fact that the BESS is necessary to be operated in a high-voltage (HV) level for sufficiently synchronizing with the grid via the buck-type dc-ac converter. The two-stage conversion systems are employed to reduce the BESS-side voltage. The dc-dc conversion stage is inserted into the former conversion

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and employed to boost/step up the BESS LVDC level to the HVDC level for the dc-ac converter before. Even though this leads to a smaller BESS sizing, reducing weight, saving cost for investment and maintenance, and so on, the twice power conversion degrades the overall conversion efficiency. With the mentioned benefits and drawback of the two-stage conversion system, the quasi single-stage conversion systems were introduced [13-17] to improve the efficiency while being able to preserve the advantages.

The overview structure of the quasi single-stage conversion system is shown in Fig. 1. It is similar to that of the single-stage conversion by directly connecting the BESS terminal to the dc-ac converter. Meanwhile, it is also similar to that of the two-stage conversion by connecting the BESS terminal to the dc-dc converter for transferring the LVDC to the HVDC for the dc-ac converter. However, the different thing is that both of these connections are operated at the same time by using the extra dc-ac converter topology for the dc-ac conversion stage. To support the two dc-voltage connections, this extra dc-ac converter is structured by dual dc ports and here called 2dc-ac converter, where the one dc port is used to link the dc energy from the BESS, but the other one port is used to link the dc energy from the dc-dc converter. As a consequence, the dc-dc converter does not absorb all of the power. This leads to the efficiency improvement over the two-stage conversion while operating in a similar way with LV BESS. The connection structure between the dc-dc converter and the 2dc-ac converter for the quasi single-stage conversion system is entirely called the quasi single-stage converter (QSSC) (see Fig. 1).

With the QSSC, there are several 2dc-ac converter topologies that can be applied to the system. In the past works, the T-type converter is applied in [13-16] and the neutral-point-clamped converter is applied in [17]. It is noticed that the application with the multilevel converters is suitable for the quasi single-stage conversion systems. Although the systems have the intrinsic benefit of a high waveform quality by using the multilevel converters, the applying dual-dc-port connection of the multilevel converter with the two different dc derivations is possible to be an undesirable cause of the unbalancing dc voltage phenomenon. As is generally known, this results in a decrease in ac waveform quality and further grid power quality, harmonic loss, and finally a decrease in efficiency [18-20]. For the grid applications, the aforementioned negative results become one of the main problems in the grid-connected BESS with the QSSC, where there are no any existing works of literatures that have investigated and debated this problem as remarked in the following reviews. In [13], the single-phase QSSC has been proposed with the scalar closed-loop control for the grid-connected application. The pulse-width-modulation (PWM) stage is made more difficult by using up to four high-frequency carriers and is not able to provide full dc utilization performance due to its sinusoidal PWM-based feature. Moreover, this paper is unclear in terms of the unbalancing dual-dc-voltage issue. The single-phase QSSC with the sinusoidal PWM approach has been also presented in [14]. However, the unregulated dc-dc converter by means of the dc transformer is employed instead of the active dc-dc converter in order to simplify the control algorithms. As anticipated, the dual dc voltages cannot be controlled at all, leading to the plausibility of the unbalanced dual dc voltages of the 2dc-ac converter, where the problem statement was neglected. In [15], the three-phase QSSC for the three-phase grid-connected application has been presented with the voltage and power closed-loop controls based on the standard current vector control method [21-23]. One main focus is the modified space vector PWM (SVPWM) approach for modulating the 2dc-ac converter in the QSSC. Despite its 100% dc utilization, the modified SVPWM strategy is significantly more complicated in analysis, calculation, and implementation due to the unbalanced SVPWM diagram analyzed based on the possibility of dual-dc-voltage unbalancing. The identical system proposed in [15] is also performed in [16]. However, the two-inphase disposition carrier-based PWM (CBPWM) technique is applied in [16] with the non-sinusoidal PWM schemes. This is to avoid such complex PWM strategies of the CBPWM used in [13] and the SVPWM used in [15] while achieving full dc utilization. The CBPWM operation under the unbalanced dc voltages is also analyzed and implemented with the asymmetrical two carriers in amplitudes. Despite of this, the asymmetrical PWM scheme indeed produces the inferior waveform quality than the symmetrical PWM scheme in any case. Due to the regardless of the unbalancing dual-dc-voltage issue, the asymmetrical PWM scheme is run regularly. Then, the asymmetrical discontinuous PWM scheme is preferred to be applied. Although it can inherently reduce the switching loss, it reduces the waveform quality in addition to the reduced waveform quality obtained by using the asymmetrical PWM scheme. The model predictive power control is employed in [17]. It has to rely on the power information to make forecasts, where the additional observer circuit is required to update the data. This results in requirement of recognizing a proper model as well as costly installation. Again, these existing conventional studies are concerned on regulating a constant level of the HVDC, while the battery voltage is varied according to the BESS function. Because of this, the dual-dc-voltage balance is not able to be controlled, which may be why the voltage unbalancing problem is ignored for the QSSC system.

This paper presents the balancing dual-dc-voltage control method to figure out the unbalancing dual-dc-voltage issue in the QSSC for the on-grid LV BESS application, as shown in Fig. 1, where it is extended from [24] in terms of contribution, principle analysis, results and discussion, and evaluation. The main features and developments are summarized as follows.

1) Balancing dual-dc-voltage control method is proposed

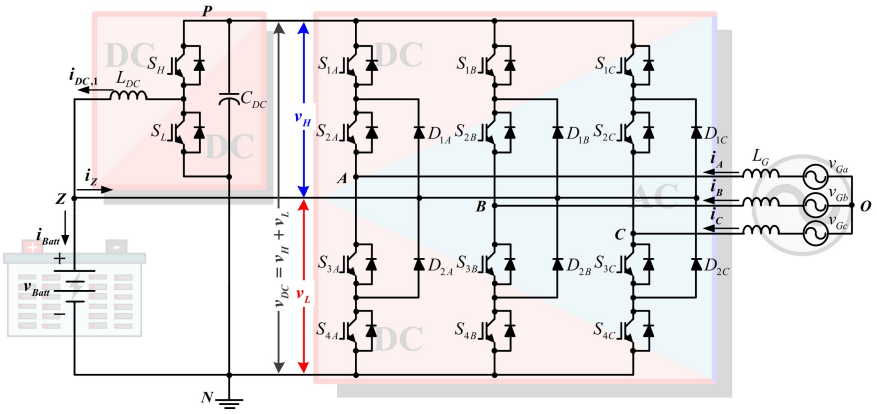

***Fig. 2**: Detailed power-circuit schematic of the BESS with the QSSC topology, consisting of the dc-dc converter and dual-dc port three-level NPC converter.*

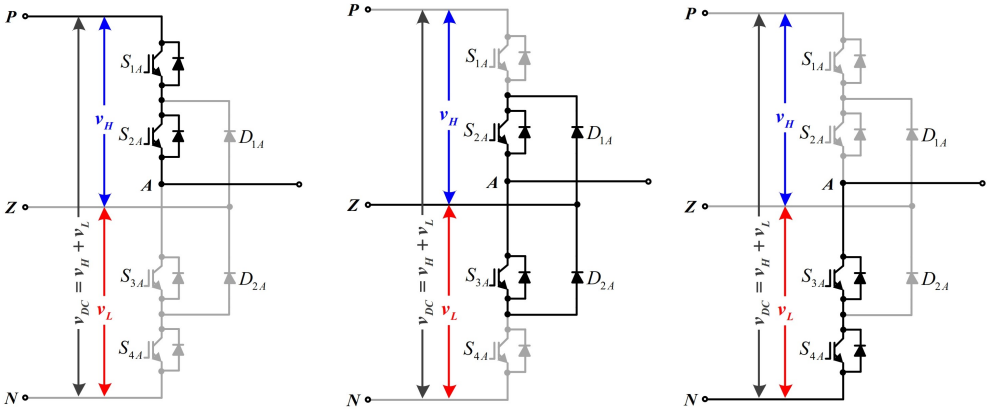

***Fig. 3**: Equivalent circuit diagrams with three switching states (Leg A) of the 2dc-ac converter part for the QSSC.*

***Table 1**: Switching State Definition (Leg A) of the 2dc-ac converter part for the QSSC.*

State Definition	Active Switching Device				Pole Voltage
	S_{1A}	S_{2A}	S_{3A}	S_{4A}	v_{AZ}
[P]	On	On	Off	Off	v_H
[O]	Off	On	On	Off	0
[N]	Off	Off	On	On	$-v_L$

to control the dc-dc converter for producing the HVDC that is varied to be twice as high as LVDC or BESS voltage. That means the dual-port dc voltages of the 2dc-ac converter are regulated to be equal all the time for overcoming the unbalancing dc voltage problem, whether impacting on the power circuit or the control circuit.

2) Due to the proposed control method, the symmetrical CBPWM is performed with the following benefits. i) The PWM stage is simplified from [15] by using CBPWM technique, and [13,16,17] by using symmetrical two-inphase disposition carriers. ii) The voltage and current waveform qualities are improved from [13-17] with the symmetrical and continuous CBPWM scheme. iii) Full dc utilization is achieved by using the continuous non-sinusoidal PWM scheme [25].
3) The bidirectional power control based on the standard current vector control is simple to be applied in order to achieve effective and high performance of active and reactive power controls, as well as power factor (PF) correction (PFC).
4) The proposed system can be controlled with the power control in separating with the balancing voltage control. That means the grid-connected LV BESS with the QSSC can be enhanced for both inverting mode (power grid supply) and rectifying mode (energy storage) without compromising the grid waveform

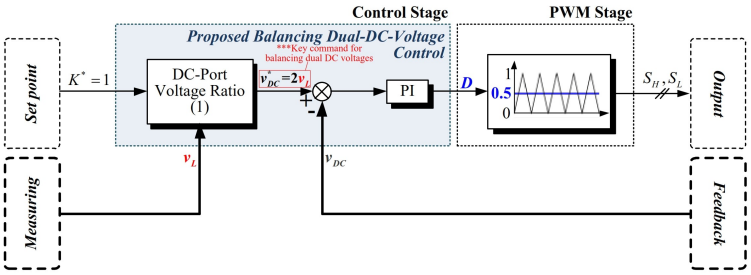

Fig. 4: *Control-circuit block diagram of the proposed balancing dual-dc-voltage control for the QSSC.*

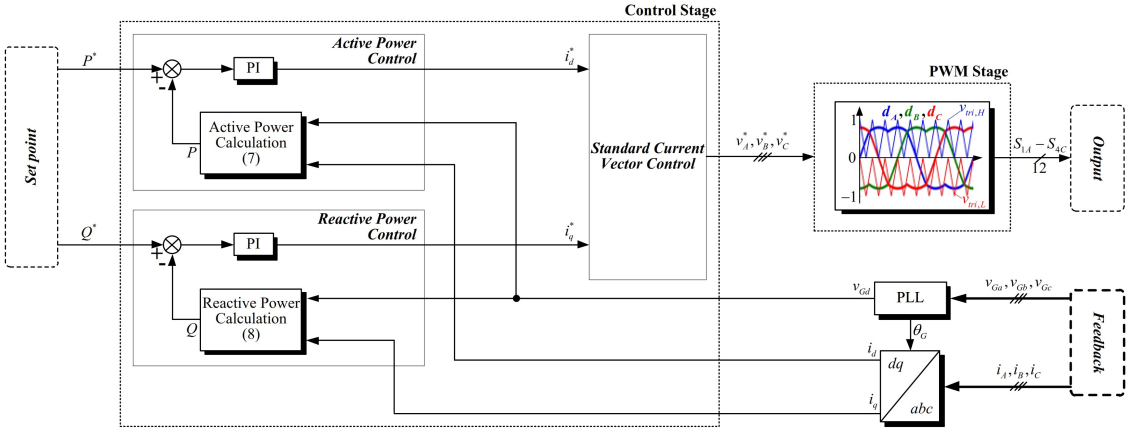

Fig. 5: *Control-circuit block diagram of the active and reactive power controls based on the standard current vector algorithm for the QSSC.*

quality.

To describe the QSSC operation and its benefit attainment, the corresponding operation principle is addressed in Section 2. Then, the key principles of the proposed system are also given. The contributions are verified through the simulation results in Section 3 along with the benchmarking and comparison with the existing works. Section 4 is the summary of this article.

2. PROPOSED BESS WITH BALANCING DUAL-DC-VOLTAGE QSSC

In the BESS with the QSSC, it is developed by using the proposed balancing dual-dc-voltage control. Before moving on to the proposed approach, the operation of the system is initially discussed in Section 2.1. Then, the principle of the proposed control method is expressed in Section 2.2. The continuing impact of the proposed control method on the 2dc-ac converter's PWM stage is discussed in section 2.3 along with the power control based on the standard current vector control for the grid-connected application.

2.1 Operation Principle

From the power-circuit diagram, as shown in Fig. 1, the on-grid BESS with the QSSC consists of the battery system for storing and releasing the dc energy. It is similar to that of the two-stage conversion that the terminal of the battery is connected to the dc-dc converter, but it is different by also connecting the battery terminal to the lower dc port of the 2dc-ac converter. This sharing power flow is the reason behind the power loss reduction in the dc-dc conversion from that of the two-stage conversion, called the QSSC. After that, the 2dc-ac converter converts the dc energy obtained from both dc-dc converter and battery system to the ac energy for the grid. The ratio of the dual dc voltages is defined as

$$K = 2v_L / v_{DC}, \tag{1}$$

where K is the dc-port voltage ratio, v_L is the lower dc-port voltage, v_{DC} is the dc-link voltage, $v_{Batt} = v_L$ is the battery terminal voltage, v_H is the upper dc-port voltage. The operating states of the QSSC per leg are corresponding to the three states of the 2dc-ac converter, as depicted in Fig. 3 and summarized in Table 1.

2.2 Proposed Balancing Dual-DC-Voltage Control and PWM Stage of DC-DC Converter

Based on the aforementioned operation principle, the proposed approach is the balancing dual-dc-voltage control of the dc side to improve the waveform quality of the ac side through the 2dc-ac converter operation. In this method, the dc voltage balancing control is processed in the closed-loop control for the dc-dc converter, as shown in Fig. 4, according to the voltage gains of the dc-dc converter as expressed by

$$v_{DC} = v_L / (1 - D), \tag{2}$$

***Table 2**: Parameters of Control Circuit.*

Parameters		Value
DC-DC Converter		
Set point of dc-port voltage ratio	K^*	0.5
		1
		1.5
Switching frequency	$f_{sw,dc-dc}$	20 kHz
2DC-AC Converter		
Set point of active power	P^*	− 5 kW
		± 10 kW
Set point of reactive power	Q^*	0 kVAR
		± 5 kVAR
Switching frequency	$f_{sw,2dc-ac}$	2.5 kHz

Proposed concept

***Table 3**: Parameters of Power Circuit.*

Parameters		Value
Battery voltage	v_{Batt}	300 V-400 V
Low-voltage ac grid		380 V, 50 Hz
DC-link voltage	v_{DC}	600 V-800 V
Upper dc-port voltage	v_H	$v_{DC}/4$
		$v_{DC}/2$
		$3v_{DC}/4$
Lower dc-port voltage	v_L	$v_{DC}/4$
		$v_{DC}/2$
		$3v_{DC}/4$
Rated Power		10 kW
Filter resistance for grid-side	R_G	10 mΩ
Filter inductance for grid-side	L_G	5 mH
Filter inductance for dc-dc converter	L_{DC}	20 mH
Filter capacitance for dc-dc converter	C_{DC}	1,000 µF

Proposed concept

$$v_L = Dv_{DC}, \tag{3}$$

where D is the duty cycle of the dc-dc converter's PWM stage. In (2) and (3), they are the voltage gains of the dc-dc converter for the inverting and rectifying modes, respectively. With the proposed control diagram, the set point of the dc-port voltage ratio (K^*) is assigned at 1 to generate $v_{DC}^* = 2v_L$ according to (1), where v_{DC}^* is the corresponding set point of dc-link voltage based on the proposed control method. Substituting v_{DC}^* into (2) and (3), the command of D results in 0.5 for the PWM stage to modulate the dc-dc converter, providing $v_{DC} = 2v_L$ for both inverting and rectifying modes. This leads to the balancing of the dual dc voltages as follow:

$$v_H = v_{DC} - v_L = v_{DC}/2 = v_L \tag{4}$$

In (4), although v_{Batt} is varied decreasingly and increasingly based on the inverting and rectifying modes, respectively, the balancing dual dc voltages ($v_H = v_L$) is regulated all the time by the dc-dc converter based on the proposed control method. This is to improve the ac-side waveform quality for all voltages and currents in order to develop the system performance from that of the other existing unbalancing dual-dc-voltage control methods [13-17], where the detail is discussed in the next subsection.

2.3 Active and Reactive Power Controls and PWM Stage of 2DC-AC Converter

From the balancing dual dc voltages of the QSSC with the proposed control method, the PWM stage of the 2dc-ac converter results in the identical magnitudes of both upper and lower high-frequency triangular carriers ($v_{tri,H}$ and $v_{tri,L}$), as shown in Fig. 5. Therefore, the general symmetrical PWM schemes can be applied for modulating the 2dc-ac converter. In this paper, the well-known continuous non-sinusoidal PWM scheme [25] is performed and its duty cycle expressions are given as follow:

$$\begin{cases} d_A = m_a\left(2/\sqrt{3}\right)\sin(\omega t) + d_0 \\ d_B = m_a\left(2/\sqrt{3}\right)\sin(\omega t - 2\pi/3) + d_0 \\ d_C = m_a\left(2/\sqrt{3}\right)\sin(\omega t + 2\pi/3) + d_0 \end{cases}, \tag{5}$$

where d_A, d_B, and d_C are the three-phase duty cycles for modulating Legs A, B, and C, respectively, of the 2dc-ac converter. d_0 is the zero-sequence component. ω is the angular fundamental frequency. m_a is the modulation index that is 0 to 1 for the linear operation. Based on the PWM scheme of (5), the voltage gain of the 2dc-ac converter is

$$\hat{V}_{LL,1} = m_a V_{DC}, \tag{6}$$

where $\hat{V}_{LL,1}$ is the fundamental component's peak value of the line-to-line voltages. For the power control, it is carried out with the outer closed-loop control based on the standard current vector control with the inner closed-loop control (see Fig. 5), according to the expressions as

$$P = \left(3/2\right) v_{Gd} i_d, \tag{7}$$

$$Q = -\left(3/2\right) v_{Gd} i_q, \tag{8}$$

where P and Q are the active and reactive powers, respectively. With the Park transformation principle [26], v_{Gd} is the direct component of the three-phase grid voltages. i_d and i_q are direct and quadrature components, respectively, of the three-phase grid currents.

Based on (5) and (6), it is generally known that the symmetrical PWM scheme is able to provide the better waveform qualities of the voltages and currents than

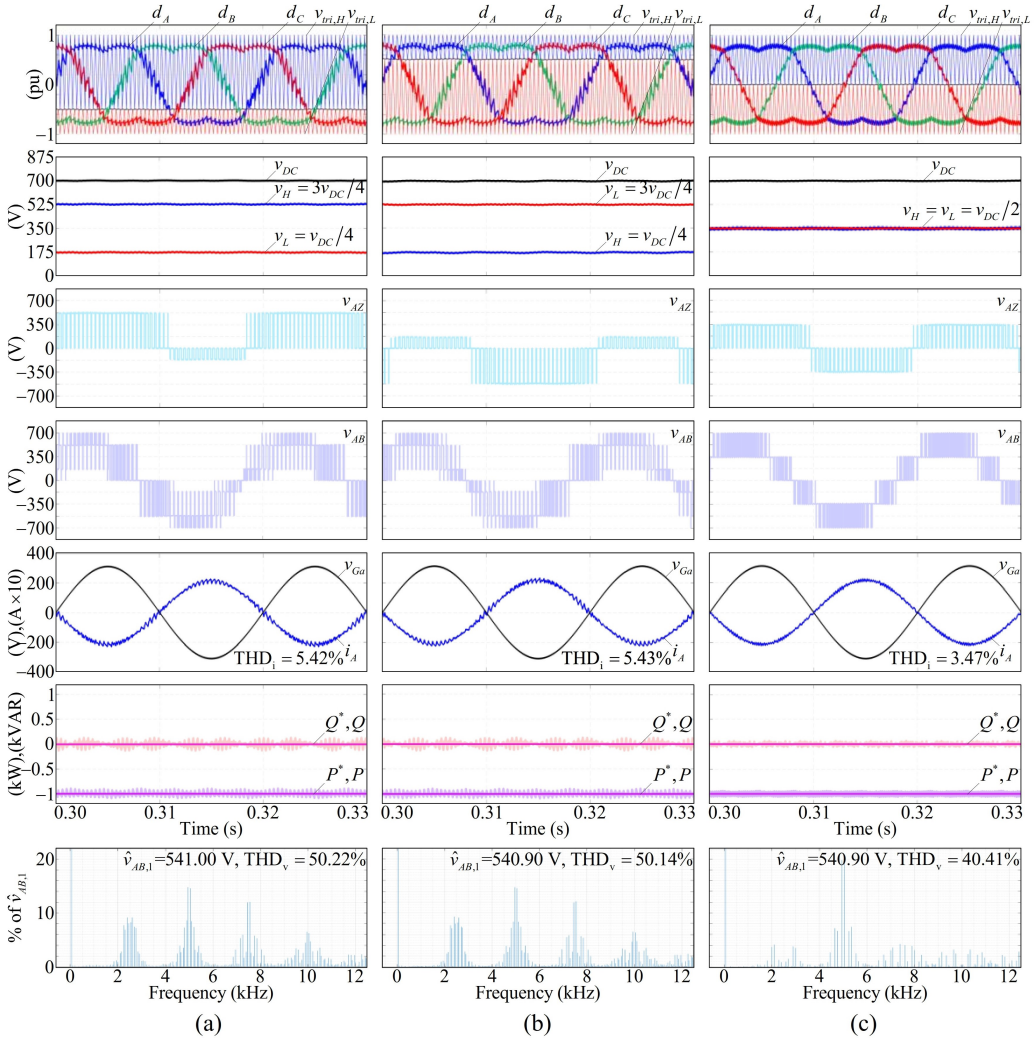

***Fig. 6**: Steady-state simulated results of the BESS with the grid-connected QSSC. (a) Unbalancing dual dc voltages with $K = 0.5$. (b) Unbalancing dual dc voltages with $K = 1.5$. (c) Balancing dual dc voltages with $K = 1$ (proposed concept).*

those of asymmetrical PWM schemes, which are caused by the unbalancing dual dc voltages owing to the other existing control methods [13-17]. The aforementioned improvement of the system with the proposed control method and the simply applicable power control based on (7) and (8) are then verified by the simulation results.

3. RESULTS AND DISCUSSIONS

To verify the performance of the proposed balancing dual-dc-voltage QSSC for developing the grid-connected LV BESS, a MATLAB/Simulink simulation platform of the proposed system is built in accordance with Fig. 2 for the power circuit and Figs. 4 and 5 for the control circuit. The corresponding parameters are specified in Tables 2 and 3, respectively. The comparisons of the results along with the evaluation between the proposed system and that of the other unbalancing dual-dc-voltage conditions are also revealed in order to support the attractiveness of the proposed system to be a good candidate for the on-grid LV BESS.

Fig. 6 shows the PWM stage waveforms of the 2dc-ac converter with the fundamental-frequency duty cycles d_A, d_B, and d_C along with the switching-frequency triangular carrier waveforms $v_{tri,H}$ and $v_{tri,L}$ operated under the modulation index at 0.77, according to (6) for the BESS with the constant v_{DC} at 700 V connected to the LV ac grid. Subsequently, the dc waveforms of v_{DC}, v_H, and v_L, as well as the corresponding ac waveforms of v_{AZ}, v_{AB}, v_{Ga}, and i_A, are performed. To verify the applicable power control loop, the waveforms of P^*, P, Q^*, and Q are displayed accordingly. Eventually, the frequency spectrums of v_{AB} are demonstrated. In line with (1), the case studies of the unbalancing dual dc voltages are related to the results of $v_H = 3v_{DC}/4 = 525\ V$ and $v_L = v_{DC}/4 = 175\ V$ for a given $K = 0.5$ and those of $v_H = v_{DC}/4 = 175\ V$ and $v_L = 3v_{DC}/4 = 525\ V$ for a given $K = 1.5$, as shown in Figs. 6(a) and 6(b), respectively. For the case study of the proposed system, the dual dc voltages are regulated to be equal as $v_H = v_L = v_{DC}/2 = 350\ V$ according to the concept of (**??**), as shown in Fig. 6(c). As a result of the unbalancing dual dc voltages, the asymmetrical carrier

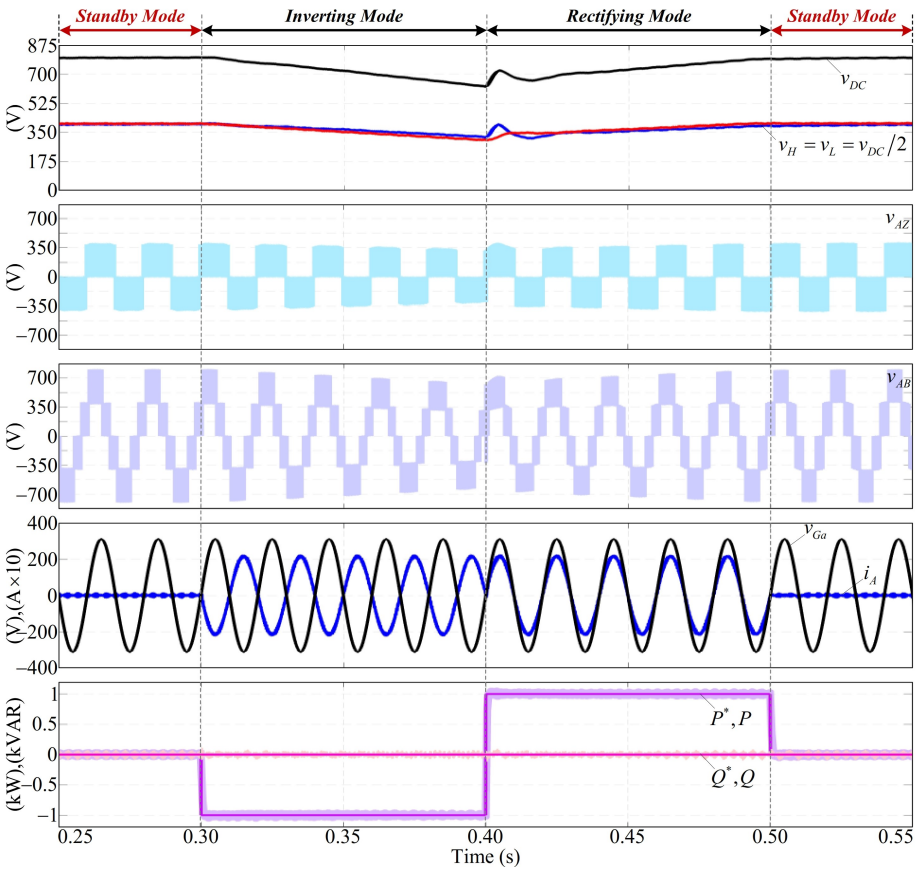

***Fig. 7**: Dynamic response of the proposed BESS through simulation in the assumed real application according to the operating range of the battery (300V-400V).*

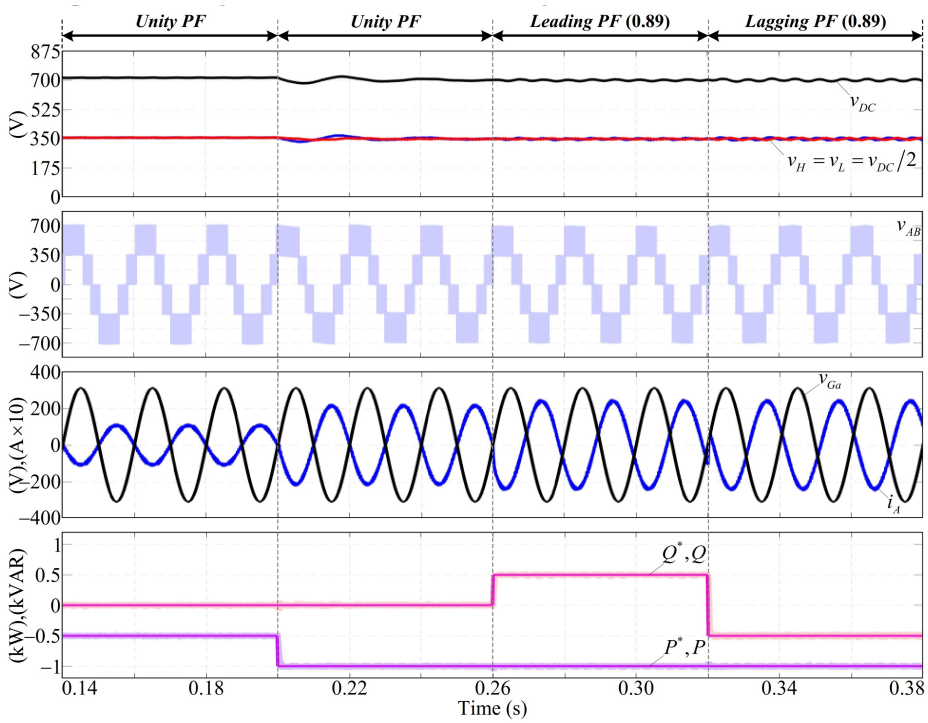

***Fig. 8**: Dynamic response of the proposed BESS through simulation by controlling the active and reactive powers with the step variations.*

waveforms are conducted in the PWM stage, resulting in the asymmetrical PWM scheme for modulating the part of the 2dc-ac converter. On the contrary, the proposed concept of the balancing dual dc voltages is performed with the symmetrical PWM scheme. Thence, the QSSC for the BESS with the proposed concept provides the symmetrical ac PWM waveforms, as can be observed and compared in terms of v_{AZ} and v_{AB} waveforms. This can be also validated by the corresponding result of the frequency spectrum presenting the lower calculated total harmonic distortion (THD) of v_{AB} with THD_v around 10 % than that of the others. For this reason, even though the BESS with all these case studies can support the same active power along with the unity PF to the grid, the proposed BESS can be connected to the grid with the better power quality, as it is evident by the lower ripples of the grid current i_A with $THD_i < 5\%$, according to IEEE Std. 519-2022 [27], the active power P, and the reactive power Q. This confirms the performance of the proposed control method that can improve the waveform quality and the power quality for the on-grid LV BESS with the QSSC from the existing unbalancing dual-dc-voltage control methods [13-17].

In Fig. 7, the dynamic response of the proposed BESS is illustrated, which consists of the dc response waveforms (v_{DC},v_H, and v_L), ac response waveforms (v_{AZ}, v_{AB}, v_{Ga}, and i_A), and power response waveforms (P^*, P, Q^*, and Q). Based on real application of the BESSs, the simulation results are divided into four scenarios, as follows.

Scenario 1 (0.25 s to 0.30 s): represents as the standby mode of the BESS that is in a fully charged state, when there is still enough power in the grid. Therefore, there is no any power entered into the grid during this time period.

Scenario 2 (0.30 s to 0.40 s): represents as the inverting mode of the BESS to deliver the power into the grid, when the grid lacks the power at the rated value. It can be seen that v_{Batt} or v_L is decreased from the full-charged voltage at 400 V to 300 V while i_A is constant, which is proportional to the constant active power of 10 kW for this mode. As expected, the unity PF is also achieved.

Scenario 3 (0.40 s to 0.50 s): represents as the rectifying mode of the BESS to recharge the power into the BESS, when it is in a low state of charge (v_{Batt} or v_L at 300 V). During this mode, v_{Batt} or v_L is increased from 300 V to the full-charged voltage at 400 V again. Due to charging at the same rated power and PF control as the previous mode (10 kW), the magnitudes of i_A and P are still the same with the unity PF but have an opposite direction.

Scenario 4 (0.50 s to 0.55 s): represents as the standby mode again when the BESS is fully charged and the grid still has a sufficient power. This leads to the similar results to those of scenario 1.

For these four scenarios, it can be seen that the dual dc voltages (v_H and v_L) are able to be kept at the identical level as $v_H = v_L = v_{DC}/2$ while the battery voltage is varied according to the BESS function. Such a good agreement with the proposed principle leads to the symmetrical PWM waveforms of v_{AZ} and v_{AB}, resulting in a good waveform quality of i_A and a further good power quality. This can guarantee the practical feasibility of the proposed control method for the grid-connected QSSC in the BESS application.

Fig. 8 shows the usability of the power control loop when applied to the proposed balancing dual-dc-voltage QSSC for the BESS, where the test is divided into four time periods under the inverting mode for example. For the first and second time periods, the active power is set to be changed in step from 5 kW to 10 kW while the reactive power is set to 0 kVAR for the entire duration. It can be seen that the proposed system can accomplish the PFC and the desired active power control while maintaining the balancing of the dual dc voltages. For the last two intervals, the settings of the reactive power at 5 kVAR and -5 kVAR are carried out to inject 0.89 leading and lagging PF, respectively, into the grid. As a consequence, the corresponding response of i_A is then leading and lagging v_{Ga} by 27 degrees. This can prove the effectiveness of the proposed BESS serving as the function to balance the reactive power consumption and production of the utility grid, as independent from the active power supporting function. This is in good accordance with the theoretical principle of the power control based on the standard current vector algorithm (7) and (8). Besides, the high-quality waveform and power of the grid-connected BESS are obtained based on the proposed balancing dual-dc-voltage QSSC.

The comprehensive calculated THD_v of v_{AB} and THD_i of i_A for the BESS with the QSSC at the operating (nominal) voltage of 700 V under the variation of the power are depicted in Figs. 9 and 10, respectively. To compare the results obtained between the proposed balancing dual-dc-voltage control, $K = 1$, and the other existing unbalancing dual-dc-voltage controls [13-17], such as $K = 0.5$ and $K = 1.5$, the lower THD_v and THD_i obtained by the proposed control method can confirm the improvement of the waveform qualities for both voltages and currents of the system from those of the other exiting methods for the entire low-to-high power operating range. This can authenticate the development of the on-grid LV BESS with the QSSC by using the proposed balancing dual-dc-voltage control. Note that due to the same unbalanced voltage levels of v_H and v_L for the cases of $K = 0.5$ and $K = 1.5$, which just alternate each other between these two cases, their THD curves result in the same profiles, as can be validated by seeing again in Figs. 6(a) and 6(b) for the operating point of 10 kW.

4. CONCLUSION

In this paper, the balancing dual-dc-voltage control method is proposed for developing the on-grid LV BESS with the QSSC in terms of waveform quality and control

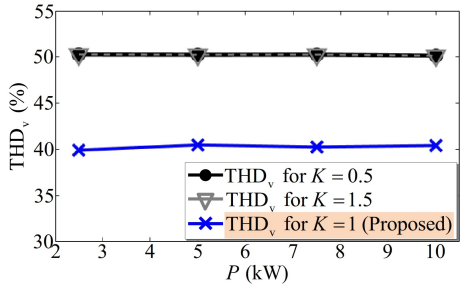

***Fig. 9**: THD_v curves of v_{AB} versus the variation of the active power while regulating v_{DC} at 700 V.*

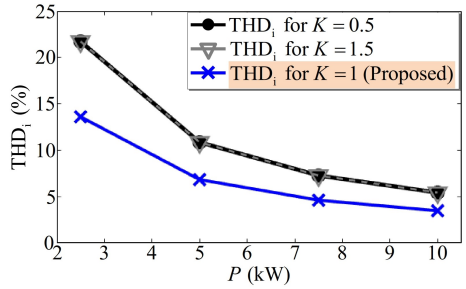

***Fig. 10**: THD_i curves of i_A versus the variation of the active power while regulating v_{DC} at 700 V.*

algorithm. It is utilized to control the internal dc-dc converter by setting the command of the dc-port voltage ratio to 1. The consequence of the HVDC twice the LVDC or BESS voltage makes the dual-port dc voltages identical and balanced. Although their voltage levels are varied according to the BESS voltage, there is no any impact on the system. Due to the achievement of the symmetrical feature in power circuit, the control-circuit PWM stage is also symmetrical and simplified. To make it simpler, the symmetrical two-inphase disposition CBPWM technique is applied. As expected, the ac waveform qualities of the voltages and currents are improved. Moreover, the symmetrical continuous non-sinusoidal PWM scheme is preferred to not only offers the full dc utilization, but also significantly improves the waveform quality in addition to the aforementioned improvements. The power control based on the standard current vector control principle makes the system easy and effective to be implemented for bidirectional active power flows, reactive power injection, and PFC, with inverting and rectifying modes while not impacting the grid waveform quality due to its decoupled control operation from the balancing voltage control algorithm. A 10-kW grid-connected BESS simulation model is employed to validate the performance and practical feasibility of the proposed system. The control ability of the LV BESS within the operating of 300 V to 400 V for microgrid (380 V, 50 Hz) connection ensures the absences of the overcharging and overdischarging in the proposed system. A good agreement and better profiles, compared with that of conventional systems, of the results can confirm the developments of the waveform quality and power quality in the BESS with the QSSC along with high quality in grid-connected performance. It can be noted that the proposed system can be applied by using any other 2dc-ac converter configurations, to other dc ESS microgrid applications, such as photovoltaic, electric vehicle, and so on, and even in other larger-scale systems (front-of-the-meter), such as distribution, transmission, and utility generation.

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