West First Turn Routing Algorithm with Backtracking Mechanism for on Chip Networks

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ABSTRACT

To design high-performance and energy-efficient electronic systems, this research article is an attempt to investigate the usage of Network-on-Chip architectures as a possible substitute for conventional bus-based interconnects in integrated circuits. This study primarily focuses on backtracking strategies for assessing the West First Turn routing protocol, increasing the scalability and efficiency of network-on-chip-based electronic systems by analyzing parameters like energy usage and resource utilization. This article presents a comparative study of XY routing, West First Turn routing, and Odd-Even Turn routing, along with the West First Turn routing with a backtracking mechanism for handling such issues, including wormhole flow control, in the Network on Chip architecture. Simulation results for a 3x3 mesh network coded in Verilog-HDL using Xilinx Vivado 2021.1 infer that West First Turn routing with a backtracking mechanism is found to be better in terms of simplicity, adaptability, and resource utilization efficiency. This article will help researchers offer valuable insights and inferences for their research and development work as a contribution to the comprehension of associated challenges, potential solutions, and advancements for selecting an appropriate routing mechanism under particular design specifications. The knowledge shared in this study not only advances Network-on-chip technology but also offers useful recommendations for creating scalable and effective computing systems.

Keywords: Case Statement, Data Packets, Mesh Networks, Routing Mechanism, RTL Synthesis, Verilog-HDL, Wormhole Flow Control

1. INTRODUCTION

The rapid advancement in the field of high-performance electronic systems with increasing demand for energy-efficient communication architectures has prompted researchers to explore new approaches in computer architecture design [1]. Traditional bus-based interconnects have become a limiting factor in achieving scalability and efficiency in modern computing systems [2]. As a solution to these limitations, network-on-chip (NoC) architectures have gained significant attention in recent years. On-chip networks offer a scalable and efficient interconnect fabric that replaces the conventional bus-based interconnects [3]. They utilize a network of interconnected routers to facilitate communication among on-chip components, including processors, memory units, and accelerators [4]. This paradigm shift in interconnect design has revolutionized system architectures, providing improved performance, reduced latency, enhanced scalability, and lower power consumption [5] [6].

The objective of this research is to compare and evaluate different routing algorithms commonly used in NoC architectures, such as XY routing, West First Turn routing, and odd-even routing, with standard code and with case statements [2][3][4]. Additionally, backtracking techniques will be explored to enhance system performance by effectively managing congestion and deadlocks. The proposed research aims to contribute to the growing demand for efficient and scalable systems in modern computing applications. By assessing key performance resource utilization and energy consumption, we aim to identify novel approaches that can enhance the overall efficiency and scalability of NoC-based systems.

The concept of "West First Turn with Backtracking" represents an evolution of the West First Turn routing technique. This approach incorporates a backtracking mechanism to navigate obstacles or congestion during the routing process effectively. The algorithm aligns with the West First approach but gracefully employs backtracking to find alternative routes when faced with challenges. The remainder of the document is structured as follows: Section 2 provides an overview of the materials and procedures utilized in this study, while Section 3 presents the findings and commentary. Finally, Section 4 concludes with the key highlights of the conducted research work and suggests future directions related to on-chip network architecture.

2. MATERIALS AND METHODS

The historical perspective traces the emergence of Network-on-Chip (NoC) during the early 2000s as a response to on-chip communication challenges in System-on-Chip (SoC) designs [1]. The notion of NoC was further advanced by pioneering work by scholars like Radu Marculescu, Axel Jantsch, and William J. Dally, as well

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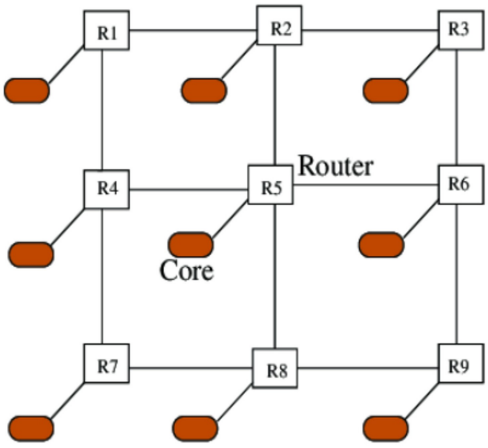

***Fig. 1**: A 3x3 2D mesh Network on Chip Architecture.*

as initiatives like the Scalable Programmable Integrated Network (SPIN). The evolution of NoCs continued with the ongoing exploration of novel routing algorithms, congestion control mechanisms, power management strategies, and other optimizations [7].

NoC technology has become a viable option for creating scalable and modular communication architectures since it naturally supports the integration of diverse cores by standardizing network boundaries [5] [6]. Figure 1 depicts a 2-dimensional 3x3 mesh NoC architecture, which, like any other network, consists of nodes and edges representing communication links. Among various aspects of NoC design, the routing algorithm plays a crucial role in determining the network's performance. Therefore, understanding and optimizing routing algorithms are of paramount importance for achieving efficient NoC designs.

An on-chip network stands as a revolutionary communication infrastructure designed to enhance data transfer and communication efficiency among various processing elements (PEs) within a chip or System-on-Chip (SoC) architecture. In contrast to traditional bus-based interconnects, NoC employs a network of interconnected routers, thereby ushering in benefits such as heightened performance, reduced latency, improved scalability, and lower power consumption [7][8].

2.1 Network on Chip Architecture

Network Interfaces (NI): Serving as crucial intermediaries between IP cores and the NoC, Network Interfaces handle data conversion and adaptation. They ensure seamless communication between the internal components and the NoC, facilitating efficient data exchange [7].

Routers: Routers play a pivotal role in the NoC structure, responsible for routing and forwarding data packets from source to destination. Employing sophisticated routing algorithms and buffering policies, routers manage congestion and optimize the flow of data within the network [9].

Links: The physical connectivity between routers is facilitated by links, establishing communication channels essential for data transmission. The efficiency and speed of these links directly impact the overall performance of the NoC [10].

2.1.1 Network on Chip Topologies

The arrangement or structure of the interconnect network is defined by NoC topologies, with several common options:

Mesh: Utilizing a grid-like structure, mesh topologies offer simplicity and ease of implementation. However, they may suffer from potential congestion points and limitations in fault tolerance [11].

Torus: Similar to a mesh but with wraparound connections, torus topologies aim to address some of the congestion issues in mesh networks, providing improved fault tolerance [12].

Fat Tree: Characterized by a hierarchical structure, fat tree topologies offer enhanced fault tolerance and efficient routing, making them suitable for large-scale systems [6].

Butterfly: Employing a recursive binary structure, butterfly topologies are known for their scalability. However, they may have limitations in fault tolerance and overall complexity [13].

Irregular Topologies: Customized irregular topologies allow for tailored designs based on specific application requirements, providing flexibility in optimizing for performance, fault tolerance, and scalability [14].

2.1.2 Switching Techniques

Switching techniques in NoCs make decisions on how data is routed and transferred between network entities and nodes:

Store-and-Forward: This technique involves buffering complete packets before forwarding, ensuring that the entire packet is received before transmission. While reliable, it can introduce latency, especially in high-traffic scenarios [15].

Virtual Cut-Through: Offering lower latency, virtual cut-through switches forward packets as soon as they are received. This technique reduces the delay associated with store-and-forward but may increase the likelihood of congestion [16].

Wormhole Switching: Dividing packets into smaller flits and forwarding them in a pipelined fashion, wormhole switching enhances concurrency and reduces overall latency. However, it introduces the potential for head-of-line blocking, where smaller flits may get delayed behind larger ones [8].

2.2 Routing Algorithm for On Chip Networks

The network topology and routing algorithm are key factors that differentiate various Network-on-Chip (NoC) architectures. The routing algorithm determines the path a packet should take to reach its destination, and it plays a crucial role in achieving high performance, load

balancing, deadlock-free and livelock-free operation, and fault tolerance. Routing algorithms can be categorized into source routing, where the path is determined before the packet is sent, and distributed routing, where the packet chooses its path hop by hop [17].

Routing methods are further categorized as deterministic, partially adaptive, and completely adaptive in the context of wormhole switching. Deterministic routing algorithms restrict packets to predefined paths, simplifying the routing architecture but limiting the ability to avoid congested channels. On the other hand, fully adaptive routing algorithms allow packets to dynamically choose any available channel, improving packet delivery time but increasing complexity and energy dissipation in the router.

Partially adaptive routing algorithms aim to strike a balance between determinism and adaptivity. They provide limited adaptivity by allowing packets to use a subset of available channels [10]. These algorithms can be further categorized as minimal or non-minimal. Minimal routing algorithms strictly use the shortest paths between sender and receiver, while non-minimal routing algorithms may deviate from the shortest path.

In the context of wormhole switching, the choice of routing algorithm impacts the efficiency and performance of the NoC. Wormhole switching divides packets into flits and forwards them in a pipelined manner. The routing algorithm determines the specific flit's path through the network. The use of wormhole switching allows for low latency communication and efficient bandwidth utilization [8]. However, the choice of routing algorithm, whether deterministic, partially adaptive, or fully adaptive, affects the network's ability to adapt to changing conditions and optimize performance. Rioting protocols used for this study are described in the following sub-sections.

A. XY Routing

This algorithm is based on the 2D grid topology of the network, where each router has a unique X and Y coordinate [11]. When a router receives a data packet, it examines the destination address in the packet header and compares it with its own coordinate. Depending on the difference between the X and Y coordinates of the source and destination routers, the packet is forwarded to one of the four directions: East, West, North, or South. If both the X and Y coordinates are equal, then the packet has reached its destination and is ejected from the network.

One way to implement XY routing in Verilog is to use a case statement that checks the values of the current and destination coordinates of the data packet and sets a valid direction accordingly. The case statement has 16 cases, each corresponding to a possible combination of the X and Y coordinates. For example, if the current X coordinate is 0 and the destination X coordinate is 1, then the valid direction is East. If the current X coordinate is 3 and the destination X coordinate is 2, then the valid direction is West. If both the X and Y coordinates are equal to 3, then the valid direction is Eject. The case statement also has a default case that handles any invalid values of the coordinates by setting no direction [2].

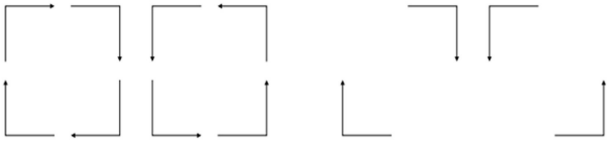

***Fig. 2**: Allowed turns in XY routing algorithm.*

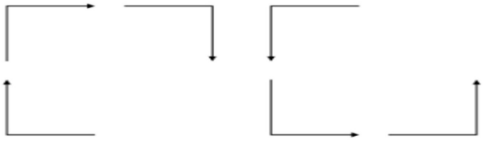

***Fig. 3**: West first allowed turns.*

XY routing is an example of deterministic routing, as it always chooses the same path for a given source and destination pair. Deterministic routing paths, allowed and disallowed turns are illustrated in Figure 2.

B. West First Turn Routing

West First Turn routing is a deterministic routing algorithm based on the West First Turn model shown in Figure 3, which is a deadlock-free turn model for 2D mesh networks [4]. It is a non-minimal routing algorithm that may not choose the shortest path from the source to the destination.

The West First Turn routing approach prevents all turns to the west direction, so the packets going to the west must be first transmitted as far west as is necessary [2]. In other words, all the west hops are taken before other directions. This way, it avoids creating cycles in the channel dependency graph that could cause deadlocks. The algorithm works as follows: Given a 2D grid topology of the network, where each router has a unique X and Y coordinate, when a router receives a data packet, it examines the destination address in the packet header and compares it with its own coordinate. Depending on the difference between the X coordinates of the source node and destination node, the packet is forwarded to one of the four possible directions: East, West, North, or South. If both the X and Y coordinates are equal, then the packet has reached its destination and is ejected from the network [12].

One way to implement West-First turn routing in Verilog is to use a case statement that checks the values of the current and destination coordinates of the data packet and sets a valid direction accordingly. The case statement has four cases, each corresponding to a possible relation between the X coordinates of the source and destination routers. For example, if the current X coordinate is greater than the destination X coordinate, then the valid

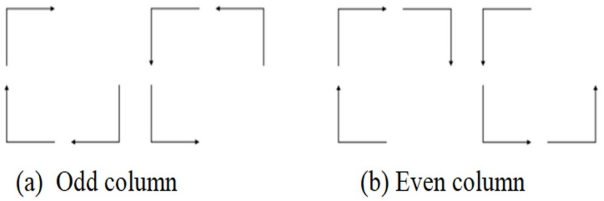

***Fig. 4**: Odd-Even turn routing.*

direction is West. If the current X coordinate is less than the destination X coordinate, then the valid direction is East. If both the X coordinates are equal, then there are three sub-cases based on the relation between the Y coordinates of the source and destination routers, which are handled by another case statement. For example, if both the X and Y coordinates are equal, then the valid direction is Eject. The case statement also handles any invalid values of the coordinates by setting no direction.

C. Odd-Even Routing

The odd-even routing mechanism is an adaptive routing approach that works on the odd-even turn model as shown in Figure 4. It is a deadlock-free turn model for 2D mesh networks. It is also a shortest path routing algorithm that always prefers a minimal path from the source to the destination. In the odd-even turn model, a column is even if its x-coordinate is even and odd if its x-coordinate is odd. This odd-even routing mechanism prohibits even column routing tiles from routing data packets east to north and east to south and prohibits odd column routing tiles from routing the data packets north to west and south to west [13]. The routing mechanism is illustrated in figure 4. In this way, it avoids creating iterative cycles in the channel dependency graph that could cause deadlocks.

The algorithm works as follows: Given a 2D grid topology of the network, where each router has a unique X and Y coordinate, when a node receives a data packet for transmission, it extracts the destination address in the packet header and compares it with its own coordinate. Depending on the parity (odd or even) of the X and Y coordinates of the source and destination routers, as well as some rules to avoid deadlocks and livelocks, the packet is forwarded to one of the four directions: East, West, North, or South. If both the X and Y coordinates are equal, then the packet has reached its destination and is ejected from the network [3].

One way to implement Odd-Even routing in Verilog is to use a case statement that checks the values of the current and destination coordinates of the data packet and sets a valid direction accordingly. The case statement has three main cases, each corresponding to a possible combination of the parity of the X and Y coordinates of the source router.

D. Backtracking Mechanism

In the context of routing, backtracking refers to a

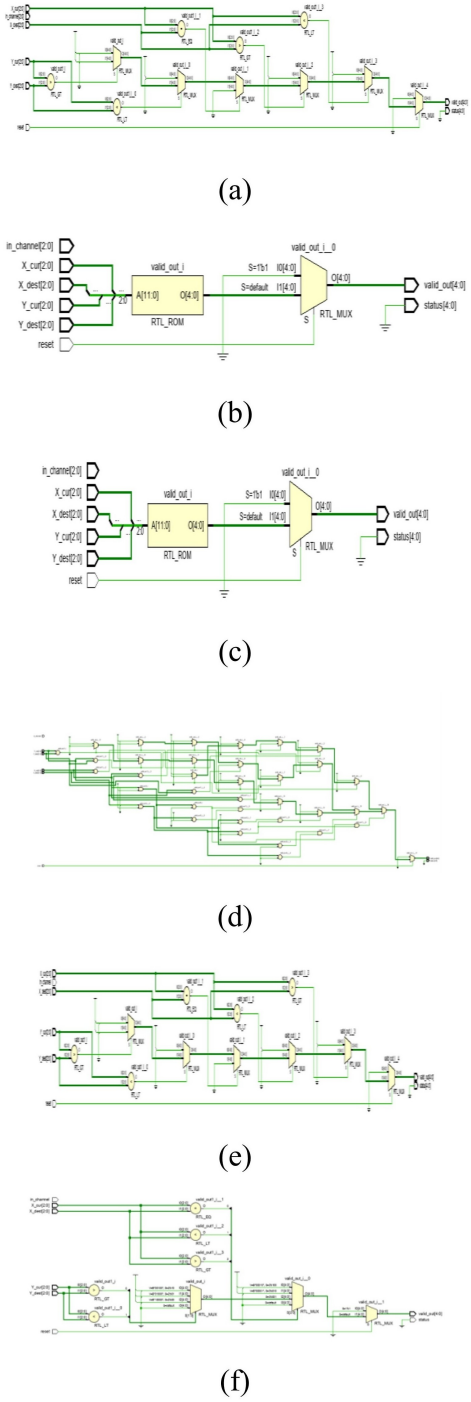

***Fig. 5**: RTL schematic diagram for (a) XY routing with if-else Statement (b) XY routing with case statement (c) Odd-Even routing (d) Odd-Even routing with case statement. (e) West First Turn routing (f) West First Turn routing with case statement.*

mechanism employed by routing algorithms to handle situations where a packet encounters obstacles or dead ends while attempting to reach its destination. It allows the packet to retrace its steps and go back to a previous node it visited in order to explore alternative routes 18][19]. Backtracking in routing algorithms is

primarily used to avoid deadlocks, resolve congestion, or find alternative paths when the initially chosen path becomes blocked or congested. It enables the packet to dynamically adapt its route based on the current network conditions.

When a packet reaches a point where it cannot proceed further or encounters an unfavourable condition, such as a congested link or an unavailable route, the backtracking mechanism kicks in. The packet then returns to the previous node it visited and selects a different path to continue its journey towards the destination. Through the use of backtracking, routing algorithms can improve the efficiency and reliability of packet delivery by dynamically adapting to changing network conditions. It helps in finding alternate routes and avoiding situations where packets are stuck or unable to reach their destinations.

3. RESULTS AND DISCUSSION

In this section, a comparative analysis of the routing algorithms in terms of resource utilization and power dissipation, based on the results obtained from the Xilinx Vivado tool, is summarized. For synthesis and implementation purposes, the Xilinx Virtex 4 FPGA was used as the target device. It also analyzes the effect of using case statements for optimizing the RTL synthesis and static timing analysis of different routing approaches, as shown in Figure 5.

3.1 Resource Utilization

The FPGA resource utilization summary for the covered routing algorithms with if-else statements and case statements is shown in Table 1. XY routing with the if-else statement and the West First Turn routing algorithm have similar resource utilization, using 11 cells, 26 and 24 I/O ports, 50 nets, and 9 LUTs, respectively. The odd-even routing algorithm requires more resources, using 37 cells, 24 I/O ports, 184 nets, and 15 LUTs. Figure 5 (a), (c), and (e) show the schematic routing with if-else statements. The use of case statements reduces the resource utilization significantly for the XY routing algorithm with only 2 cells, 26 I/O ports, and 7 nets. The West First Turn Routing algorithm also benefits from case statements, with 8 cells and 20 I/O ports. However, the odd-even routing algorithm still requires more resources than the other algorithms, even with case statements, with 23 cells, 20 I/O ports, and 133 nets. Figure 5 (b), (d), and (f) represent the schematic routing with case statements.

3.2 Power Dissipation:

The power dissipation of the covered routing algorithms with and without case statements is shown in Table 2. We can see that the total on-chip power ranges from 0.705 W to 1.325 W for the different algorithms. The XY routing algorithm with case statements has the lowest total on-chip power consumption of 0.705 W, while the odd-even routing algorithm without case statements has the highest power consumption of 1.325 W. The dynamic power consumption varies from 0.113 W to 0.730 W for the different algorithms. The XY routing algorithm and the west-first turn routing algorithm have similar dynamic power consumption of 0.537 W and 0.536 W, respectively. The odd-even routing algorithm without case statements has the highest dynamic power consumption of 0.730 W, while using case statements reduces it to 0.532 W. The static power consumption is relatively consistent across the algorithms, ranging from 0.592 W to 0.596 W.

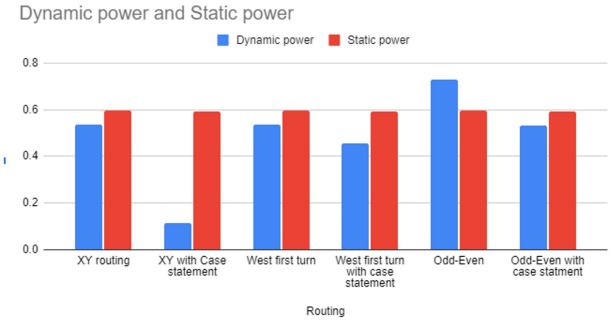

Fig. 6: *Comparison of power consumption for routing approaches.*

The comparison of the routing algorithms reveals trade-offs between resource utilization efficiency and power consumption. Power consumption in different routing approaches is illustrated in Figure 6.The XY routing algorithm demonstrates efficient resource utilization and low power consumption, making it an attractive option for network-on-chip design. The west-first turn routing algorithm balances simplicity and power consumption while offering deterministic and deadlock-free routing. Despite requiring more resources, the odd-even routing algorithm provides greater flexibility and agility in managing network problems and congestion. The use of case statements proves beneficial in reducing resource utilization and optimizing power consumption for the routing algorithms, emphasizing the importance of implementation techniques in achieving efficient designs. [3][4][11][12].

3.3 West-First Turn Routing Algorithm with Backtracking Mechanism

Following an extensive comparison of six routing algorithms, the West-First Routing algorithm with Backtracking emerges as a standout solution, striking a balance between simplicity and efficiency [19]. This algorithm exhibits advantages aligning with goals of enhanced efficiency, reduced resource utilization, and minimized power consumption [20]. The incorporation of Backtracking further refines the algorithm's adaptability, allowing it to make well-informed routing choices in various scenarios [21].

Resource Utilization: The algorithm's implementa-

***Table 1**: FPGA resource utilization summary.*

Routing Mechanism	Cells Utilized	I/O ports	Nets	LUTs
XY routing	11	26	50	9
XY routing with Case statement	2	26	24	7
West First Turn routing	11	24	50	9
West First Turn routing with case statement	8	20	35	9
Odd- Even routing	37	24	184	15
Odd- Even routing with case statement	23	20	133	11

***Table 2**: Power Consumption of the covered routing algorithms*

Routing Mechanism	Total On Chip Power Consumption	Dynamic Power Consumption	Static Power Consumption
XY routing	1.132W	0.537W	0.595W
XY routing with Case statement	0.705W	0.113W	0.592W
West first turn routing	1.131W	0.536W	0.595W
West first turn routing with case statement	1.051W	0.457W	0.594W
Odd- Even routing	1.325W	0.730W	0.596W
Odd- Even routing with case statement	1.127W	0.532W	0.594W

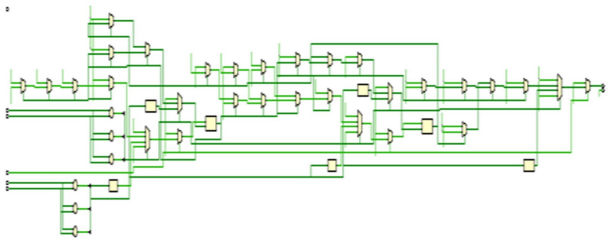

***Fig. 7**: RTL schematic diagram for West First Turn Routing with Backtracking.*

tion utilized 43 cells, integrated 26 I/O ports, established 93 nets, and employed 15 LUTs, effectively utilizing resources within the network is shown in Figure 6. Dynamic resource management in integrated circuits provides a holistic approach for the design of feature-rich electronic systems [22]. While effectively managing the on-chip transistor capacity, the RTL schematic diagram for the West First Turn with Backtracking mechanism is shown in Figure 7.

Power Consumption Analysis: The power consumption analysis reveals dynamic power consumption during active operations at 0.907 W and static power draw of 0.596 W, resulting in a total on-chip power consumption of 1.503 W. This algorithm improves the energy efficiency, and hence it can support emerging communication technologies addressing the scalability limitations for promising applications [23][24].

Path Determination: A critical aspect of the research involved testing the algorithm's adaptability when a potential path became blocked. In this scenario where a node along the designated route was obstructed, the algorithm effectively employed backtracking to explore alternative paths. Specifically, if the node (2,0) became blocked, the algorithm's routing mechanism dynamically recalculated the course to determine an alternative path [21]. The core objective of determining efficient paths for communication between source and destination nodes is achieved through the West-First Turn algorithm. For instance, routing from (0,0) to (3,2) resulted in the successful path, as shown in Figure 8:

Adaptability towards Blocked Paths: In scenarios where potential paths become blocked, the algorithm demonstrates adaptability through backtracking. For instance, if node (2,0) is obstructed, the algorithm dynamically recalculates an alternative path:

(0,0) -> (1,0) -> (1,1) -> (2,1) -> (3,1) -> (3,2)

Routing paths in West-first routing algorithm with backtracking are shown in Figure 9.

RTL Simulation: The simulation window in Figure 10 illustrates the implementation of the West-First Turn Routing Algorithm with backtracking for the designed mesh network. The routing module receives packets with different source and destination coordinates and input channels and decides the output channel for each packet

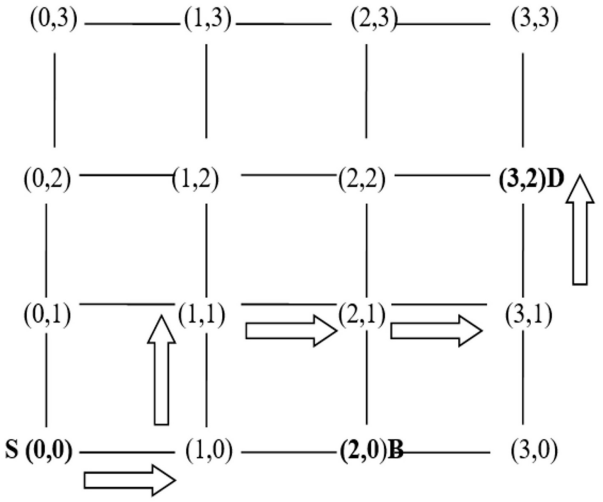

***Fig. 8**: Routing paths in West-first turn routing algorithm.*

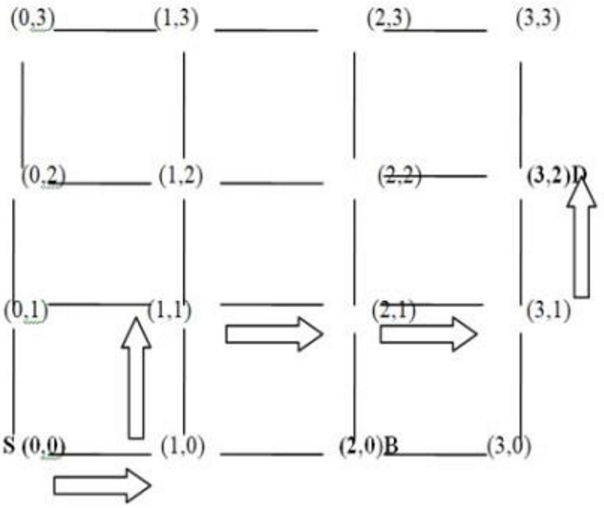

***Fig. 9**: Routing paths in West-first routing algorithm with backtracking.*

based on the routing algorithm. The routing module, Route_Func, employs backtracking to avoid deadlocks and congestion, ensuring efficient packet routing. The simulation illustrates the routing paths for the data packet from the source node (0,0) to the destination node (3,2) while considering various scenarios.

Key parameters analyzed during the RTL simulation include: X_cur, Y_cur: Representing current coordinates; X_dest, Y_dest: Indicating destination coordinates; in_channel: Flag for the packet's incoming direction, reset: Signal resetting the module, valid_out: Vector indicating valid output directions, and status: Flag indicating solution status. Simulation results help in the visualization of the process followed for the path selection to forward data packets from the source node to the destination node in the West First Turn Routing with Backtracking Mechanism. Through simulation and RTL synthesis, the on-chip network's performance is compared to three different routing strategies: XY

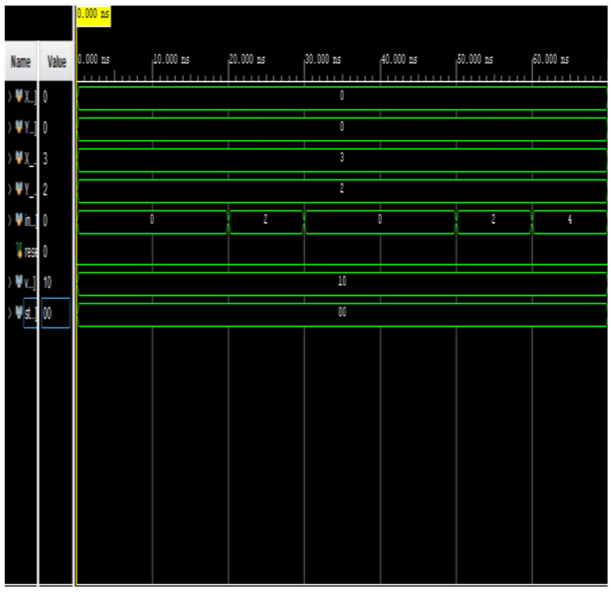

***Fig. 10**: RTL Simulation results for West First Turn Routing with Backtracking Mechanism.*

routing, West First Turn routing, and Odd-Even routing.

This organized exploration of the West-First Turn algorithm with backtracking in mesh networks highlights its robustness in adapting to dynamic scenarios. The algorithm demonstrated its ability to establish efficient paths, even in the presence of blocked nodes, offering valuable insights for enhancing routing solutions within complex mesh network architectures [25]. The research's findings underscore the algorithm's potential to contribute to the optimization of communication paths in various applications, from on-chip networks to broader communication systems [26][27][28].

4. CONCLUSION AND FUTURE SCOPE

This paper has comprehensively examined routing algorithms in mesh networks, focusing on XY routing, West first-turn routing, and Odd-Even routing. Through RTL coding in Verilog and performance evaluations using synthesis and implementation reports for the On the Vetex-4 FPGA Board, the results obtained demonstrate that XY Routing emerged as the most resource-efficient, emphasizing simplicity. West First-turn routing displayed a balance between simplicity and power efficiency, showcasing adaptability for further optimization. Odd-Even routing, while exceptionally efficient, revealed higher resource requirements due to its complexity. The integration of case statements consistently reduced resource utilization across all algorithms, highlighting their optimization potential. The West-First Turn routing algorithm with a backtracking mechanism stood out, exhibiting dynamic adaptability and recalibrating routes in response to blocked nodes, making it valuable for dynamic networking environments.

Looking ahead, future research should explore additional hardware optimization techniques, such as pipelin-

ing, parallelism, machine learning, and resource sharing. These strategies promise to enhance resource utilization efficiency and performance of NoC architectures, contributing to reliable and efficient on-chip communication systems [27]. The area of on-chip network routing is crucial for addressing emerging challenges in this field. Additionally, future research could delve into further optimization techniques such as pipelining, parallelism, and resource sharing, which hold the potential to amplify the efficiency and performance of NoC architectures. These strategies will pave the way for more efficient and dynamic on-chip electronic systems for a smarter world.

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