A New Single-Source Switched-Capacitor Based 9-Level Boost Inverter Topology with Reduced Part Count

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ABSTRACT

This study presents a step-up 1-φ inverter utilizing a switched-capacitor (SC) configuration. The proposed topology (PT) incorporates twelve switches, two capacitors, and a single power diode, enabling the generation of a nine-level output voltage at the load terminal. This novel contribution details the structural design, operating principles, modulation strategy, and the optimum capacitance values. Additionally, simulation and experimental analyses have been performed across various loading conditions to validate the performance of the PT. A brief comparative analysis with existing advanced SC topologies is also provided, highlighting metrics such as gain, component count per level, total standing voltage, and cost-effectiveness, thereby showcasing the benefits of this innovative approach.

Keywords: Cost Function, Multilevel Inverter, Switched-capacitor, gain, voltage stress

1. INTRODUCTION

Multilevel inverters (MLIs) are extensively utilized in power generation and distribution applications, including renewable energy systems, FACTS devices, uninterruptible power supplies (UPS), and electric vehicles. Multilevel inverters (MLIs) have numerous advantages over conventional two-level inverters, including superior output waveform quality, diminished total harmonic distortion (THD), decreased power losses, reduced voltage stress, and the removal of transformers or magnetic components [1-4]. Three basic forms define conventional multilevel inverters (CMLIs): flying capacitor (FC), neutral point clamped (NPC), and cascaded H-bridge inverters. Despite their widespread use, these configurations suffer from certain limitations, such as unbalanced capacitor voltages in NPC and FC inverters, a higher number of active and passive components for achieving voltage levels beyond three, complex control requirements, and unity voltage gain.

To address the issue of excessive switching components in CMLIs, designs with reduced switching component counts have been proposed [5]. While these configurations mitigate the problem of component proliferation, they typically lack voltage-boosting capability, making them unsuitable for applications involving photovoltaic (PV) systems, wind energy, fuel cells, and electric vehicles. Voltage boosting is crucial for grid-tied systems since renewable energy sources typically generate low output voltages. To address this, a front-end boost converter or a rear magnetic circuit/transformer is typically employed to elevate the input voltage. However, incorporating boost converters or magnetic circuits adds bulk and weight to the system, reduces efficiency, and increases overall costs, making the design less practical [6]. The challenges mentioned above can be effectively addressed using the SC-based series/parallel technique. This technology provides numerous advantages, such as a voltage gain surpassing unity, automatic self-regulation of capacitor voltages, the removal of transformers or magnetic components, and a modular architecture. Consequently, much research attention has been directed into the construction and enhancement of SC topologies in recent years [7-20].

There are two main types of SC topologies used by SCMLIs: single-stage and two-stage. In order to generate bipolar voltage levels, two-stage setups necessitate an H-bridge (HB) at the rear end. The four HB switches in these topologies, however, encounter a blocking voltage that is equal to the maximum load voltage. This characteristic restricts their suitability for high-voltage applications [7-11]. The need for an HB at the output terminal's back end is eliminated in single-stage topologies. In addition, they lower the voltage stress that all switches experience together [11–20]. Voltage self-balancing and a voltage gain of four are achieved via the 9-level topology described in [12–15]. Nevertheless, these designs employ a greater number of switching components than other designs. On the other hand, the 9-level configurations introduced in [16] and [19] lack voltage-boosting capability, limiting the unity gain.

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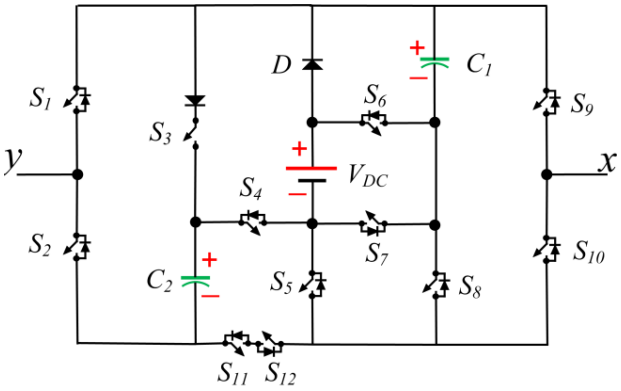


***Fig. 1**: Proposed step-up 1-φ SCMLI.*

Furthermore, these designs employ a relatively greater quantity of active and passive components. The triple-gain 7-level structure presented in [20-22] also exhibits a considerable component count.

The preceding discussion inspires the development of a step-up 9-level SCMLI with the following key features:

1. Voltage boosting ability
2. The PT relies on a single input DC source
3. The lower number of active and passive components
4. Self-balancing properties of capacitor voltage
5. Operated for different power factor

The subsequent sections are organized as follows: Section II introduces the proposed 9-level switched-capacitor (SC) topology, covering its structural design, operating principles, capacitor voltage self-balancing mechanism, and the method for determining the optimal capacitance values. Section III explains a suitable logic gate modulation scheme. Section IV presents comparative studies with existing SCMLIs to highlight the advantages of the PT. Section V presents the results analysis confirming the efficacy of the PT. Finally, Section VI concludes the paper.

2. PROPOSED 9-LEVEL SC INVERTER TOPOLOGY

2.1 Description of Proposed Design

Fig. 1 illustrates the proposed cost-efficient step-up 9-level switched-capacitor (SC) inverter design. It incorporates two types of MOSFETs power switches: one type includes an anti-parallel diode, while the other features a series-connected diode. The PT comprises two capacitors and one power diode. This inverter generates a 9-level output voltage, including 0, $\pm 1V_{DC}$, $\pm 21V_{DC}$, $\pm 3V_{DC}$, $\pm 4V_{DC}$, with a peak output of $4V_{DC}$. Table 1 summarizes the valid switching combinations for the several operational modes; idle states are indicated as "-" charging and discharging states of the capacitors as "C" and "D" respectively. The operational principles of the PT for different states are demonstrated using equivalent circuit diagrams in Fig. 2.

***Table 1**: Valid switching stages.*

A1	Active switch	B1	B2	V_{out}
1	S_2, S_7, S_9	C	-	0
2	S_2, S_{11}, S_{12}, S_{10}, S_7	C	-	0
3	S_1, S_7, S_8, S_{10}	C	-	$+1V_{DC}$
4	S_1, S_3, S_5, S_6, S_{10}, S_{11}, S_{12}	D	C	$+2V_{DC}$
5	S_1,S_5,S_7,S_{10},S_{11},S_{12}	C	D	$+3V_{DC}$
6	S_1,S_4,S_6,S_{10},S_{11},S_{12}	D	D	$+4V_{DC}$
7	S_2,S_5,S_7,S_9,S_{11},S_{12}	C	-	$-1V_{DC}$
8	S_2,S_3,S_5,S_6,S_{11},S_{12}	D	C	$-2V_{DC}$
9	S_2,S_4,S_7,S_9	C	D	$-3V_{DC}$
10	S_2,S_4,S_7,S_9	D	D	$-4V_{DC}$
A1: Mode, B1: Effect of C_1, B2: Effect of C_2, C: Charging, D: Discharging V_{out} : Output voltage, "-": idle				

2.2 Operating principles

The working principle of the proposed topology is explained through nine separate operating states.

***State** A_1 $V_{out} = 0$*

In *State* A_1, the output voltage is zero, as indicated by the conduction path for the load current (represented in red). The switches S_2-S_7-S_9 are in the ON state. Additionally, as depicted by the conduction path in black, capacitor C_1 is connected in parallel with the input DC source, thereby getting charged to V_{DC}. The circuit representation corresponding to this mode is illustrated in Fig. 2(a).

***State** A_2 $V_{out} = 0$*

In *State* A_2, the output voltage is zero, as indicated by the conduction path for the load current (represented in red). The switches S_2-S_{11}-S_{12}-S_{10}-S_7 are in the ON state. Additionally, as depicted by the conduction path in black, capacitor C_1 is connected in parallel with the input DC source, thereby getting charged to V_{DC}. The circuit representation corresponding to this mode is illustrated in Fig. 2(b).

***State** A_3 $V_{out} = 1V_{DC}$*

Switches S_1-S_7-S_8-S_{10} are turned on, enabling the load current to follow the red-marked path, while the capacitor current flows along the black-marked line. The output voltage is $1V_{DC}$, with capacitors C_1 connected across the input V_{DC} to maintain self-voltage balance. The circuit representation corresponding to this mode is illustrated in Fig. 2(c).

***State** A_4 $V_{out} = 2V_{DC}$*

State A_4 is depicted in Fig. 2(d). Switches S_1-S_3-S_5-S_6-S_{10}-S_{11}-S_{12} are activated, allowing the load current to follow the red-marked path, while the capacitor current flows along the black-marked line. Capacitor

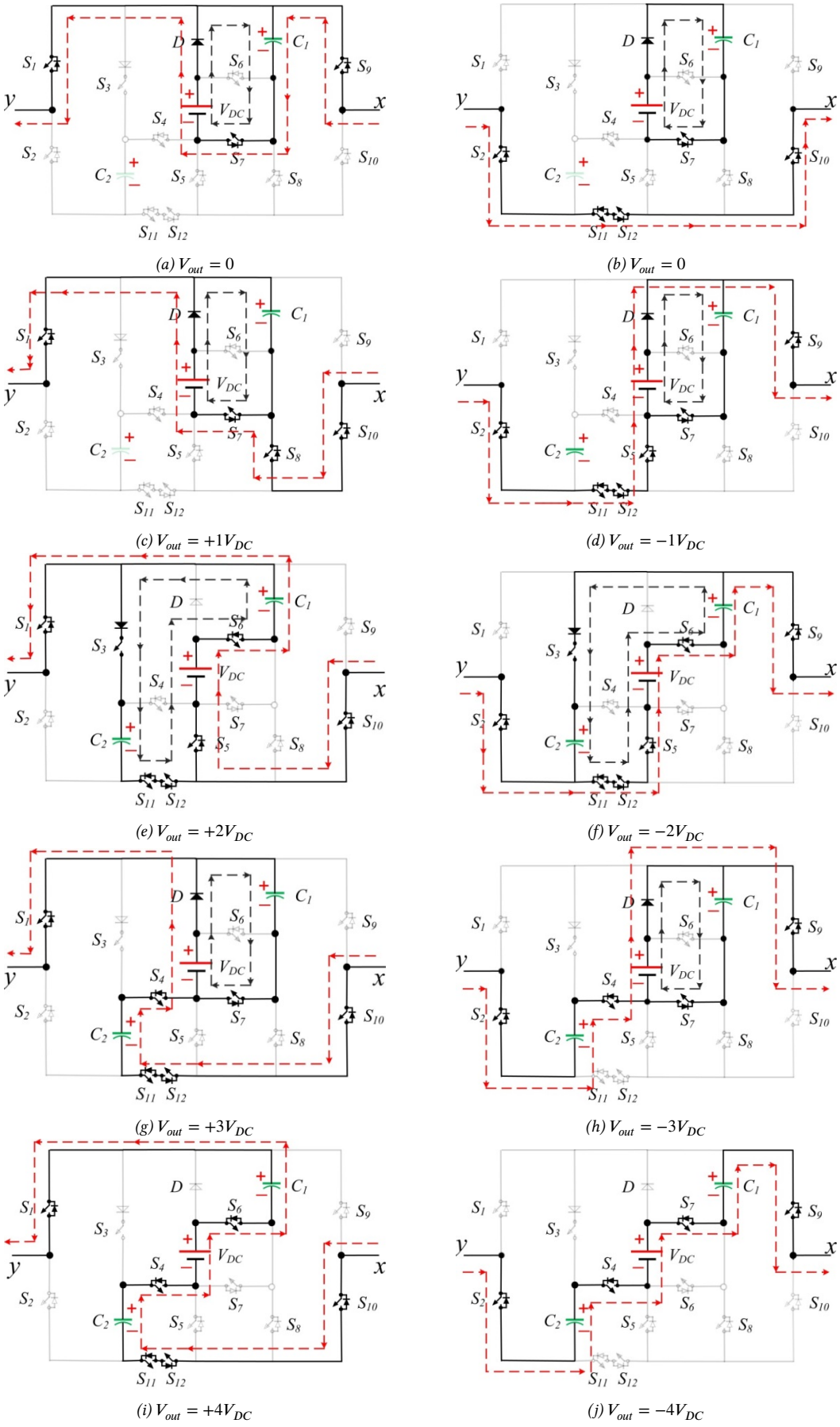


***Fig. 2**: Different operating states voltage.*

C_1 discharges through the load, increasing the output voltage to $2V_{DC}$ without the need for any additional switch. Meanwhile, C_2 remains connected in parallel with the input DC supply and capacitor C_1 through S_3, S_{11}, and S_{12}, ensuring it charges to a voltage of $2V_{DC}$.

State A_5 $V_{out} = 3V_{DC}$

State A_5 is depicted in Fig. 2 (e). Switches S_1-S_5-S_7-S_{10}-S_{11}-S_{12} are turned on, enabling the load current to follow the red-marked path, while the capacitor current flows along the black-marked path. The output voltage is $3V_{DC}$, with capacitor C_1 connected across the input V_{DC} (through S_7) to maintain self-voltage balance.

State A_6 $V_{out} = 4V_{DC}$

State A_6 is depicted in Fig. 2 (f). During the states, switches S_1-S_4-S_6-S_{10}-S_{11}-S_{12} are turned ON, directing the load current along the red-marked conduction path and generating a voltage of $4V_{DC}$ at the load terminals. Capacitors C_1 and C_2 discharge through the load, increasing the output voltage to $4V_{DC}$.

State A_7 $V_{out} = -1V_{DC}$

Switches S_2-S_5-S_7-S_9-S_{11}-S_{12} are turned on, enabling the load current to follow the red-marked path, while the capacitor current flows along the black-marked line. The output voltage is $-1V_{DC}$, with capacitors C_1 connected across the input V_{DC} to maintain self-voltage balance. The circuit representation corresponding to this mode is illustrated in Fig. 2(g).

State A_8 $V_{out} = -2V_{DC}$

State A_8 is depicted in Fig. 2 (h). Switches S_2-S_3-S_5-S_6-S_{11}-S_{12}, are turned ON, causing capacitor C_1 to discharge during the negative cycle, generating an output voltage of $-2V_{DC}$. The load current follows the conduction path indicated by the red line mark. Simultaneously, capacitor C_2 is connected to the DC supply, as shown by the blue-marked path, allowing it to charge (through S_3) $2V_{DC}$.

State A_9 $V_{out} = -3V_{DC}$

State A_9 is depicted in Fig.2 (i). Switches S_2-S_4-S_7-S_9 are turned ON, causing capacitor C_2 to discharge during the negative cycle, generating an output voltage of $-3V_{DC}$. The load current follows the conduction path indicated by the redline mark. Simultaneously, capacitor C_1 is connected to the DC supply, as shown by the blue-marked path, allowing it to charge (through S_7) $1V_{DC}$.

State A_{10} $V_{out} = -4V_{DC}$

State A_{10} is depicted in Fig. 2 (j). During the states, switches S_2, S_4, S_7, and S_9 are turned ON, directing the load current along the red-marked conduction path and generating a voltage of $-4V_{DC}$ at the load terminals. Capacitors C_1 and C_2 discharge through the load, increasing the output voltage to $-4V_{DC}$.

2.3 Self-balancing mechanism of capacitor voltage

Using a series/parallel configuration of capacitors, the PT helps to enable self-balancing of capacitor voltages as described in [8]. The charging/discharging mechanisms of the capacitors at different voltage levels are described as follows:

Capacitor C_1 is parallelly linked with the input source during the output voltage levels of 0 and $\pm 1V_{DC}$ therefore enabling it to charge to $1V_{DC}$. States 1, 2, 6, and 7 all undergo this charging procedure. Capacitor C_1 discharges its stored energy to the load when connected in series with the input source, contributing to the voltage levels of $\pm 2V_{DC}$, $\pm 4V_{DC}$.

This series/parallel charging and discharging mechanism allows C_1 to self-balance automatically to V_{DC}. Similarly, capacitor C_2 charges to $2V_{DC}$ when it is connected in parallel with both the input source and C_1, as indicated in Fig. 2 for state-3 and state-8. C_2 discharges its energy to the load for the voltage levels of $\pm 3V_{DC}$ and $\pm 4V_{DC}$. Throughout one cycle C_2 undergoes multiple charging and discharging processes for different voltage levels, ensuring automatic self-balancing of its voltage.

2.4 Determination of capacitance

The capacitance plays a significant role in SCMLI design. Since, during the discharging period, the voltage across the capacitor drops, i.e., known as voltage ripple. The design performance suffers from this voltage ripple of the capacitor. Thus, to enhance performance, a perfect amount of capacitance is required [7]. Henceforth, the voltage ripple (ΔV) for C_1 and C_2 of the PT can be expressed for a purely resistive load as

$$\Delta V_1 = \frac{1}{\omega C_1}\int_{\theta_1}^{\theta_2} i_l d\theta + \frac{1}{\omega C_1}\int_{\theta_3}^{\pi-\theta_3} i_l d\theta \tag{1}$$

$$\Delta V_1 = \frac{1}{\omega C_1}\int_{\theta_1}^{\theta_2} \frac{2V_{DC}}{R} d\theta + \frac{1}{\omega C_1}\int_{\theta_3}^{\pi-\theta_3} \frac{4V_{DC}}{R} d\theta \tag{2}$$

$$\Delta V_1 = \frac{V_{DC}}{\omega C_1 R}\left[4\pi - 2\theta_1 - 2\theta_2 - 8\theta_3\right] \tag{3}$$

$$\Delta V_2 = \frac{1}{\omega C_2}\int_{\theta_2}^{\theta_3} i_l d\theta + \frac{1}{\omega C_2}\int_{\theta_3}^{\pi-\theta_3} i_l d\theta \tag{4}$$

$$\Delta V_2 = \frac{V_{DC}}{\omega C_2 R}\left[4\pi - 3\theta_2 - 5\theta_3\right] \tag{5}$$

where θ_1, θ_2, θ_3 can be obtained from Fig 3 as

$$\theta_1 = \frac{\sin^{-1}\left(\frac{1}{4}\right)}{2\pi f} \tag{6}$$

$$\theta_2 = \frac{\sin^{-1}\left(\frac{2}{4}\right)}{2\pi f} \tag{7}$$

$$\theta_1 = \frac{\sin^{-1}\left(\frac{3}{4}\right)}{2\pi f} \tag{8}$$

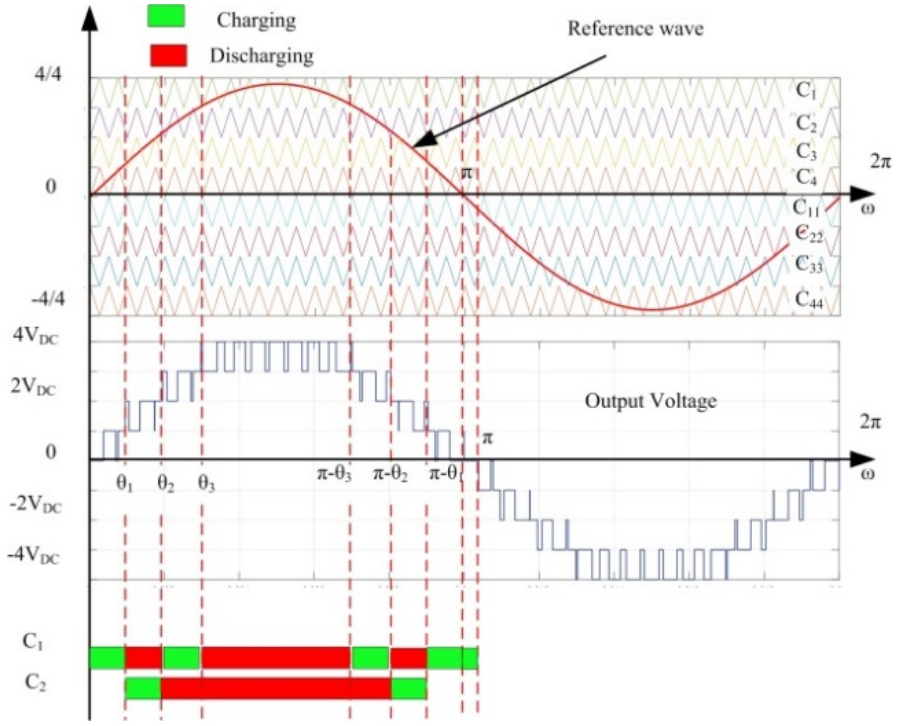


***Fig. 3**: Charging /discharging states of the capacitors.*

However, the discharge capacity of the capacitor is influenced by the power factor, load current i_l, and the longest discharging interval $(\theta_x - \theta_y)$. The amount of voltage drop during discharge (ΔVQ) can be calculated accordingly.

$$\Delta VQ_i = \int_{\theta_x}^{\theta_y} i_l \sin\theta d\theta \tag{9}$$

Hence, the optimum values of the capacitor C_1 and C_2 satisfy the equations (10) and (11).

$$C_1 \geq \frac{\Delta Q_1}{\Delta V_1} \tag{10}$$

$$C_2 \geq \frac{\Delta Q_2}{\Delta V_2} \tag{11}$$

3. CONTROL SCHEME

The PDPWM technique has been utilized for the PT. The process involves developing the PDPWM technique; the following steps are considered: A sine wave with a fundamental frequency of 50 Hz, f_r is compared against seven constant reference signals (0+, 1/4, 2/4, 3/4, 4/4, 0-, -1/4, -2/4, and -3/4, 4/4). The resulting outputs are processed through a combination of 'AND' gates and 'Ex-OR' gates to generate the signals (P_1, P_2, P_3, P_{11}, P_{22}, P_{33} as shown in Fig. 4(a-b). Next, the signal f_r is compared with seven carrier signals (C_1, C_2, C_3, C_4, C_{11}, C_{22}, C_{33}, C_{44}), each with a height of 1/3, to generate output signals (q_1, q_2, q_3, q_4, q_{11}, q_{22}, q_{33}, q_{44}) as shown in Fig. 4(c-d). These signals are obtained by feeding them into "AND" gates with their inverted counterparts. Ultimately, using "OR" gates, the outputs from Fig. 4(b-d) create driving pulses for switches S_1 through S_{11}.

***Table 2**: Simulation Parameters.*

Input supply (V_{DC})	100V
Capacitance (C_1)	6000μF
Capacitance (C_2)	4700μF
Modulation Index (M)	0.95
Carrier frequency	2kHz
Resistive-Inductive Load	80Ω-120mH
Fundamental frequency (f)	50Hz

4. SIMULATION AND EXPERIMENTAL RESULTS

Both simulation and experimental work have been conducted in order to validate the effectiveness of the PT. Both Table 2 and Table 3 contain tabulations of the major parameters that have been utilized in the process of conducting booth simulation and experimental work, respectively.

4.1 Simulation results

Theoretical principles have been demonstrated through the MATLAB/Simulink environment. The simulation

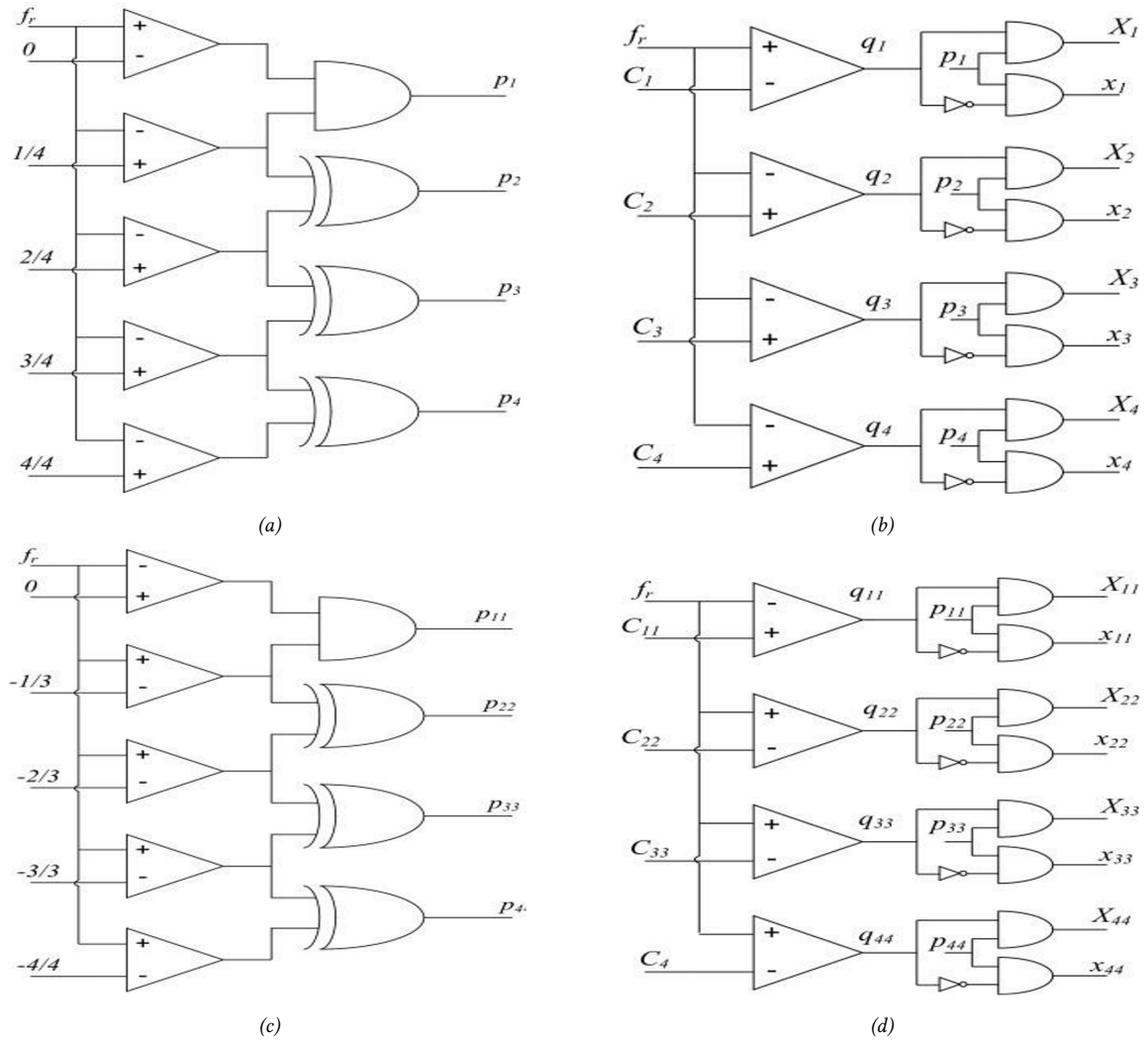


***Fig. 4**: Simple logic gate LSPWM scheme(a-b) Positive half cycle(c-d) Negative half Cycle.*

***Table 3**: Experimental Parameters.*

Capacitor C_1	PG6DI(600V and 3000 μF)
Capacitor C_2	PG6DI(600V and 2200 μF
Switch (IGBT)	G60N100
Fundamental frequency	50Hz
Carrier frequency	2kHz
Modulation Index (M)	0.95
RL-Load	80Ω-120mH
Input Voltage	12V

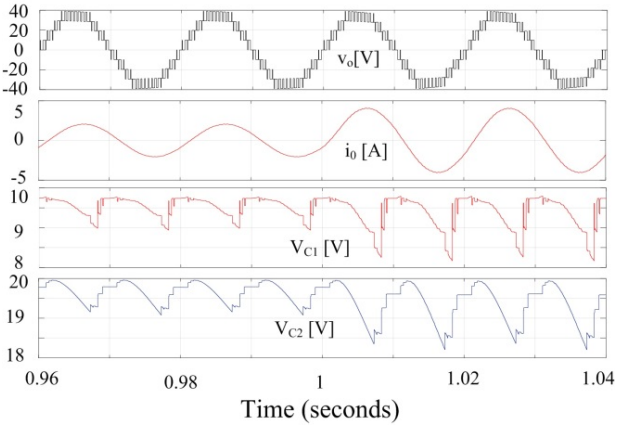


***Fig. 5**: Simulation results under dynamic state of RL-load.*

results depicted in Fig. 5 demonstrate the system's performance under dynamic situations with diverse resistive-inductive loads. The output exhibits a 9-level waveform with a stable magnitude, even in response to a step change in load. The maximum load voltage attains $4V_{DC}$., whilst the voltages across capacitors C_1 and C_2 remain self-regulated at $1V_{DC}$ and $2V_{DC}$, respectively.

Figure 6 depicts the voltage and current stresses on switches S_9 and S_3.

As illustrated in Fig.7(a), FFT study of the voltage waveform reveals a maximum fundamental voltage mag-

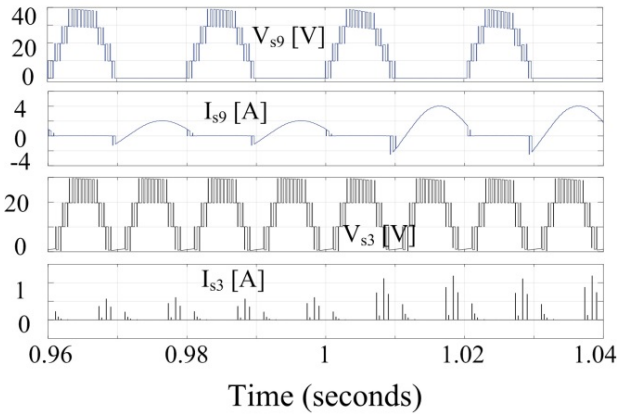


***Fig. 6**: Voltage and current stress of switch S_1 and S_3.*

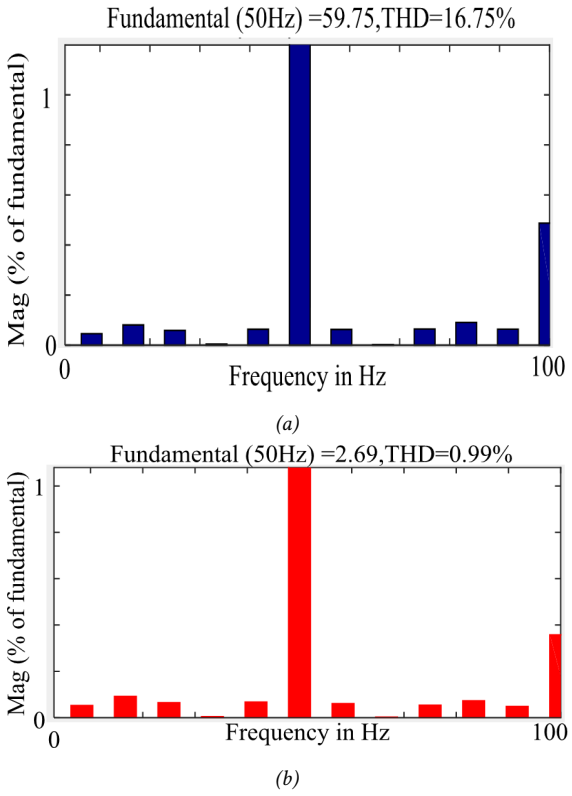


***Fig. 7**: FFT Analysis of (a) Voltage(b) Current.*

nitude of 59.75V and a THD of 16.75% for $R = 80\Omega$ and $L = 120mH$. Fig. 7(b) shows that the current waveform, when analyzed using FFT, reaches a peak fundamental current of 2.69 A and THD of 0.899%.

4.2 Experimental Results

Fig. 8 shows the results of experimental testing that validated the performance of the PT using a laboratory prototype model. Fig. 9(a-b) displays the experimental outcomes for an RL load having a modulation index (MI) of 0.95. The results show how well the system works both when the RL load is constant and when there is a sudden change, as illustrated in Fig. 9(b). There are nine separate levels to the output voltage, as seen in the Fig. 9(b). The voltages across capacitors C_1 and C_2, denoted as V_{C1} and V_{C2}, are equalized, with V_{C1} measuring 10V and V_{C2} measuring 20V. The peak voltage is 40V for both the constant load and the load with a step change. The peak current is 1.2A for the continuous load and 1.9A for the load with a step change. This diagram shows that the currents lag the voltage when an RL load is present. Figure 9(c) illustrates the variation in switching frequency for the RL load when using frequencies of 500 Hz and 2 kHz. It is evident from the graph that altering the switching frequency does not impact the voltage levels. Fig. 9(d) shows the results of RL load evaluations using three different modulation indices: 0.95, 0.50, and 0.25. The graph shows that the number of output voltage levels is directly affected by the modulation index (MI) change. For MI values of 0.95, 0.5, and 0.2, the graph shows 9, 5, and 3 output voltage levels, respectively. The magnitude will decrease as the MI is reduced while keeping the load constant. Figure 9(e-f) illustrates the voltage stress of different switches.

The efficiency study for output power ranging from 50W to 350W is presented in Fig. 9(g). The graph illustrates the relationship between efficiency and output power. Fig. 9(g) indicates that the PT attains a peak efficiency of 95.85% at an output power of 200 W. At an output power of 350W, the efficiency tested was 94.7%.

5. POWER LOSSES IN THE TOPOLOGY

In SCMLIs, power losses are classified into three main types: conduction losses, switching losses, and capacitor ripple losses. On the other hand, conduction losses are a combination of less switching, but the resistance from semiconductor switches coupled with capacitor equivalent series resistance at output and input will affect the efficiency. Switching losses occur due to energy dissipation during the turn-on and turn-off transitions of semiconductor devices. The capacitor losses occur by the charge-discharge cycle, which results in power dissipation in the capacitor's internal resistance. The detailed loss calculations are given below:

5.1 Power losses in capacitors

The power losses due to capacitor ripples are expressed as

$$P_{Ripple\ Losses} = \frac{f_o}{2} C \left(\Delta V_c\right)^2 \tag{12}$$

Each capacitor's equivalent series resistance (ESR) contributes to power losses in SCMLI. Based on this, the conduction losses of each SC can be calculated using this formula:

$$P_{Conduction\ losses\ in\ C} = \frac{R_{ESR} f_o}{2} \int_{t_x}^{t_y} i^2{}_C dt \tag{13}$$

The sum of the power losses of an SCMLI can be calculated by adding equations (12) and (13).

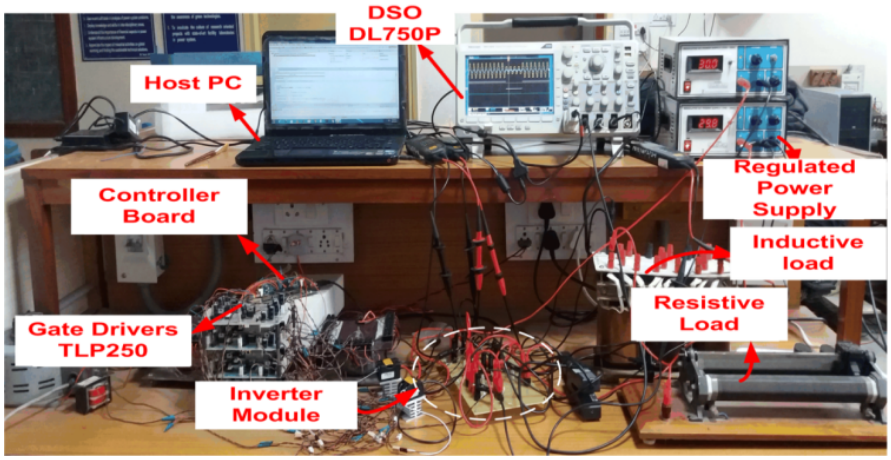


***Fig. 8**: Prototype Module.*

***Table 4**: Comparative analysis in relation to the SCMLIs.*

Ref	N_l	N_{sw}	N_d	N_c	N_{dri}	A	B	C	$F_{C/L}$	CF	THD	% η
[20]	7	12	-	2	11	5.3	2	3	3.57	4.32	21.31	97.32
[21]	7	16	-	2	15	5.3	1	3	3.57	5.47	21.88	95.12
[22]	7	8	2	2	8	6	3	3	2.85	3.71	21.76	96.52
[19]	9	12	-	3	12	6	1	1	3	3.66	16.83	96.45
[16]	9	10	4	4	10	19	1	1	3.11	5.22	16.76	93.78
[17]	9	11	-	3	10	5	1	2	2.66	4.14	16.85	94.85
[18]	9	11	-	2	11	5.2	1	2	2.66	3.24	16.72	95.34
[12]	9	12	-	3	12	6	4	4	3	3.66	16.76	95.76
[7]	9	13	-	3	13	6.3	4	4	3.22	3.92	16.82	96.78
[8]	9	8	6	3	8	8	4	4	2.77	3.66	16.72	95.68
[9]	9	10	3	3	10	6.3	4	4	2.88	3.58	16.73	96.32
[15]	9	19	3	3	19	4.8	1	4	4.88	5.42	16.87	95.65
[PT]	9	12	1	2	11	7	4	4	2.88	**3.66**	**16.75**	95.85
A: TSV_{pu}, B: Max. Blocking voltage, C: Gain												

5.2 Switching Power Losses

Intrinsic delays during the switching of a power semiconductor device result in switching losses. The losses incurred during the activation and deactivation of each power switch can be determined as [16]:

$$P_{Switching\ Losses} = \frac{1}{6} V_{in} i(t) \left\{ t_{ON} + t_{OFF} \right\} f_s \qquad (14)$$

where V_{in} = voltage stress borne by the switch during its OFF state; $i(t)$ = current-bearing capability of the switch during conduction; t_{ON} = the time at which the switch is ON; t_{OFF} = the time at which the switch is OFF; f_s = switching frequency.

5.3 Conduction Power Losses

Conduction losses for the transistor and diode part of a given power switch are obtained using the following equations, with the description of the variables given in [18]:

$$P_{Conduction\ Losses\ of\ Transistor} = V_{on,sw} I_{sw,avg} + R_{on,sw} I^2_{sw,rms} \qquad (15)$$

$$P_{Conduction\ Losses\ of\ Diode} = V_{on,d} I_{d,avg} + R_{on,d} I^2_{d,rms} \qquad (16)$$

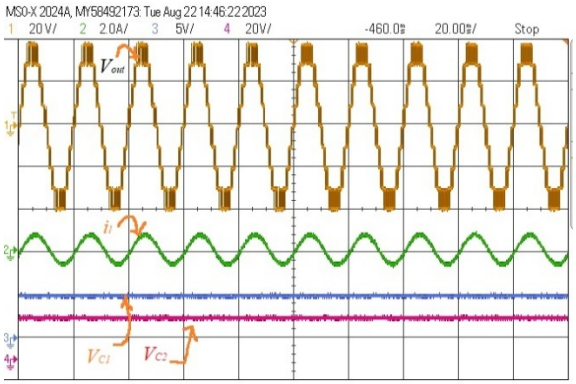
Therefore, the power losses of the proposed SCMLI can be calculated as an aggregation of these losses.

The overall effectiveness can be represented as follows:

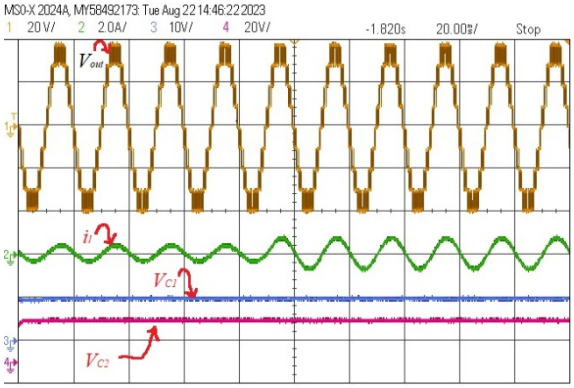
$$\%\eta = \frac{P_{out}}{(P_{out} + total\ losses)} \times 100 \qquad (17)$$

6. COMPARATIVE ANALYSIS WITH THE EXISTING SC TOPOLOGIES

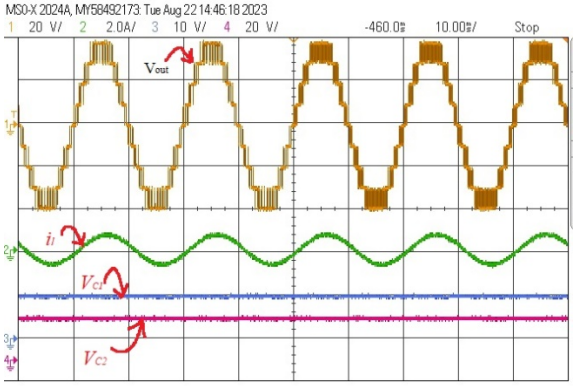
The advantages of the PT have been shown by a thorough comparison study with existing single-source



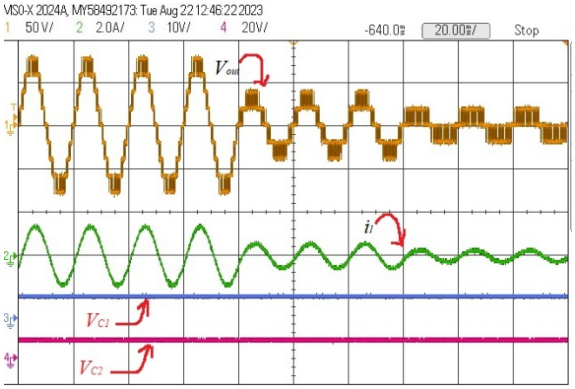
(a)



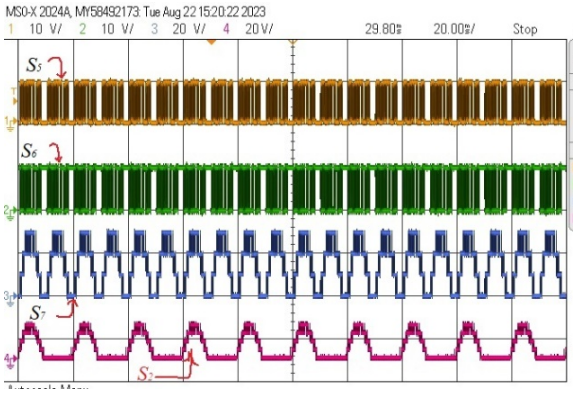
(b)



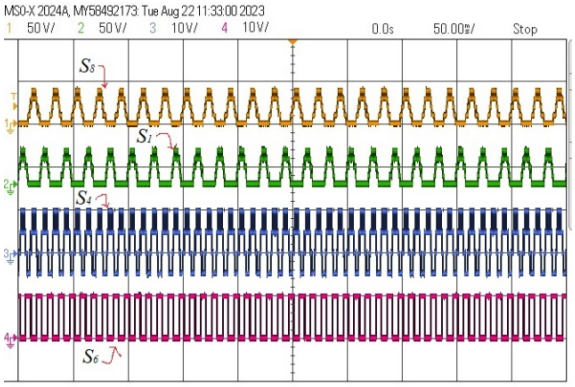
(c)



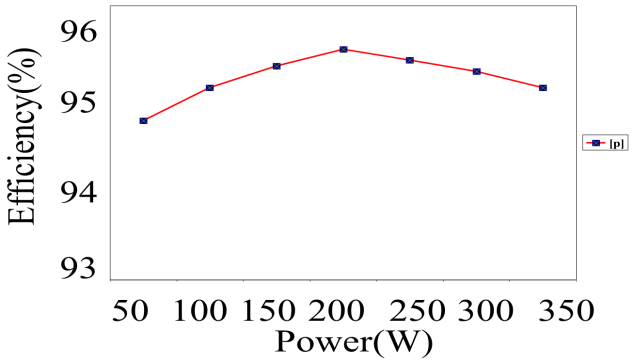
(d)



(e)



(f)



(g)

Fig. 9: *The experimental outcomes of the PT(a) steady state condition; (b) change in load; (c) change in switching;(d) change in MI;(e-f) Voltage stress on individual switches; (g) efficiency and power graph..*

SC topologies producing the same number of voltage levels. Table 4 lists the thorough comparison. The primary objective of the PT is to produce enhanced waveforms utilizing a minimized quantity of active and passive components while achieving the lowest cost function and enhanced voltage-boosting capability.

The PT uses only 12 switches, two capacitors, and one diode to generate quadruple voltage gain. The topologies presented in [16-19] have the least voltage gain as compared to the PT with a higher cost function. Quadruple boosting topologies advocated in [7-9] and [15] require larger components. Additional capacitors of the topologies [15-16], [7-9] result in high costs, more losses, and complexity in charging and discharging.

Further, two parameters, component count and the cost function of the PT, are less than the other topologies, which proves the merits of the structural design. Component count per level is defined as the summation of the total number of active and passive components to the total number of levels, and it can be expressed as

$$F_{C/L} = \frac{(N_{sw} + N_c + N_d + N_{dri})}{N_l} \tag{18}$$

And cost function is defined by [23]

$$F = \frac{(N_{sw} + N_d + N_{dri} + N_c + \alpha * TSV) * N_s}{N_l} \tag{19}$$

The weight coefficient, denoted as α, depends on the relative significance of the switching components or the TSV. The value of α varies based on the priority given to either the TSV or the switching components, making it either greater than or less than one. The PT weight coefficient is considered as one ($\alpha = 1$) when both the parameter TSV and switching components. The proposed topology achieves a THD of 16.75% and an efficiency of 95.85%.

7. CONCLUSION

The proposed SCMGIT utilizes the SC principle to produce seven unique voltage levels, with the peak voltage attaining three times the DC input. The suggested SCMGIT is advantageous, as shown by a thorough comparison with existing seven-level SC topologies. Effectively lowering voltage stress, increasing voltage gain, decreasing the cost function, and lowering the component count per level are all outcomes. Furthermore, the single-stage power transfer mechanism guarantees elevated efficiency. The modeling and experimental findings match the theoretical study, illustrating the SCMGIT's capacity to function dynamically under fluctuating load circumstances without inducing voltage imbalances among the capacitors.

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