An Asynchronous C-ternary Combinational logic for Low-Voltage Applications

Pitchayapatchaya Srikram† and **Thanasin Bunnam**, Non-members

ABSTRACT

An asynchronous C-ternary logic circuit employs an asynchronous C-ternary combinational logic operates based on a tripartite logic system, where the intermediate value $(V_{DD}/2)$ represents a spacer state. Spacer detector (SD) circuits are essential for identifying this spacer value. However, ultra-low supply voltages impose challenges on the reliable representation of the intermediate logic level. To overcome this limitation, this work proposes a low-voltage C-ternary combinational logic circuit that leverages the resistive-like characteristics of MOSFETs to generate the logical middle value. In addition, an optimized SD circuit is presented, which reduces transistor count and improves circuit efficiency. The proposed circuits were implemented and simulated using the 65 nm UMC low-leakage (LL) process at supply voltages of 0.5V and 0.9 V in the Cadence Virtuoso analog design environment. The simulation results demonstrate the impact of temperature variations and analyze the propagation delay under both operating conditions.

Keywords: Asynchronous Combinational logic circuit, C-ternary Combinational logic, Low supply voltage

1. INTRODUCTION

Asynchronous circuits [1] depend on signal transitions instead of a global clock to coordinate their operation. Consequently, the handshaking protocol is essential for communication between circuit modules in asynchronous digital systems. It enables the exchange of requests, acknowledgments, and data transmission through wires.

A key component of this system is the two-rail logic protocol, which encodes request signals and acknowledgments for each data bit. This protocol uses a two-phase handshake signal to represent data bits: logic "0" is encoded as "01", logic "1" as "10" and "00" serves as a spacer (non-data). Whereas logic "11", is not used in this encoding scheme. The two-rail logic protocol requires two wires to transmit one-bit data. As the number of communication wires increases, routing on-chip transmission networks becomes significantly more complex [2 - 3]. The new data encoding has been proposed to decrease interconnection and transistor count, with particular emphasis on circuits utilizing multi-valued logic (MVL) approaches as ternary logic [4].

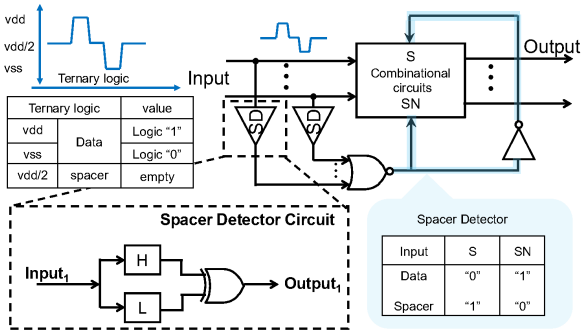


***Fig. 1**: Space detector with its functional output.*

The ternary logic expresses the logic "0" , "1", and "2" represent low, middle, and high, respectively. The middle represents as $(V_{DD}/2)$ voltage that is difficult to handle due to exceeding the threshold voltages of pMOS and nMOS transistors.

In [5 - 7], ternary logic circuits were employed using CMOS technology. There were different designs to generate the middle value, such as additional $(V_{DD}/2)$ supply voltage and divider voltage with two resistances, as well as depletion MOSFET due to varying the threshold voltage. In [8 - 9] presented the ternary logic circuit based on tunneling-based MOSFET (T-CMOS), which has a lower current level than the sub-threshold current of binary CMOS. However, ternary-based T-CMOS circuits faced the logic state "0" due to its pre-charge critical paths.

There have been numerous studies have investigated ternary logic circuits based on carbon nanotube FET (CNTFET) [10 - 15] and graphene nanoribbon field-effect transistors (GNRFETs) [16 - 17], owing to their ability to support multiple threshold voltages. However, some of the ternary logic circuit-based CNFETs require two voltage supplies— (V_{DD} and $V_{DD}/2$)—to reduce the transistor count and energy consumption [15]. Unlike, the passive-element-based devices such as memristors utilize their resistive properties as load impedances to generate the logical middle value using only a single supply voltage [18 - 19].

In C-ternary logic systems, the logical middle value

Manuscript received on June 13, 2025; revised on August 11, 2025; accepted on August 14, 2025. This paper was recommended by Associate Editor Krit Angkeaw.

The authors are with Department of Computer Engineering, Faculty of Engineering, Rajamangala University of Technology Thanyaburi, Pathum Thani, Thailand.

†Corresponding author: pitchayapatchaya.s@en.rmutt.ac.th

Digital Object Identifier: 10.37936/ecti-eec.2525233.259688

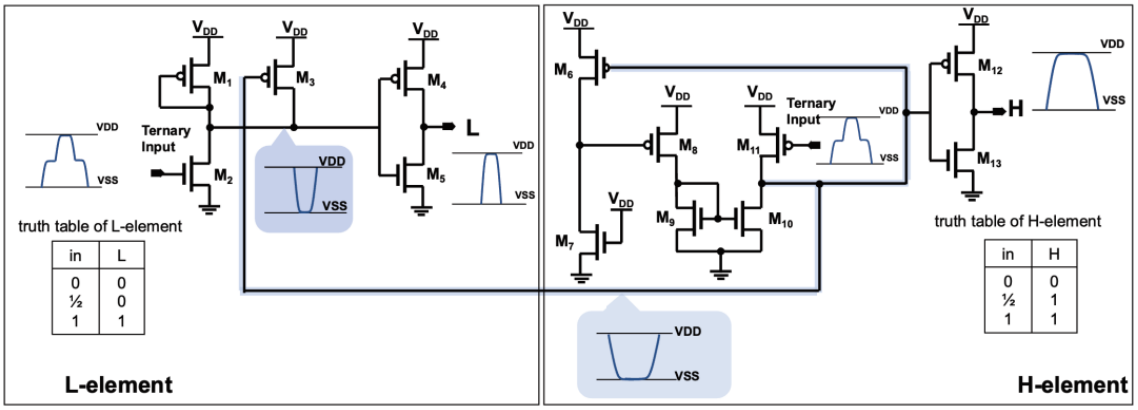


***Fig. 2**: Schematic of proposed L-element and H-element circuits.*

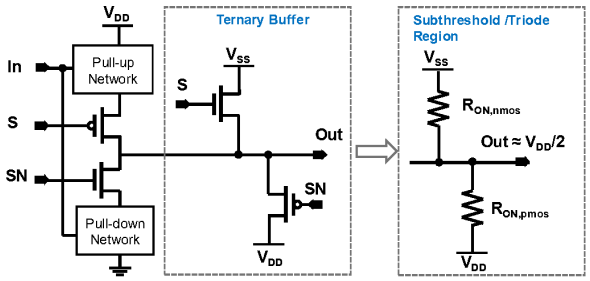


***Fig. 3**: The scheme of proposed ternary buffer yields a middle output voltage instead of a resistor.*

$(V_{DD}/2)$ typically represents invalid data or serves as a spacer. Spacer detectors (SDs) are employed to identify whether the input voltage corresponds to this logical middle value. The spacer detector circuit subsequently processes the output of the C-ternary combinational logic circuit. To reduce power consumption, asynchronous circuits leverage the advantages of CMOS technologyscaling to operate at lower supply voltages [20 – 24].

Nevertheless, the threshold voltage does not scale down proportionally. Asynchronous ternary combinational logic gates have not been demonstrated to operate under sub-threshold or near-threshold conditions while relying on a single supply voltage.

This study introduces a low-voltage C-ternary combinational logic circuits and spacer detector designed for asynchronous ternary logic. The goal is to achieve sub- or near-threshold voltage operation by using a single supply voltage value. Additionally, the proposed C-ternary combinational logic circuit was designed on the 65-nm UMC LL process technology in the Cadence Virtuoso analogue design environment.

The rest of the paper is organized as follows. Section 2 describes the optimized spacer detector circuits, which aim to minimize transistor count. Section 3 details the proposed C-ternary combinational logic circuits, incorporating fundamental logic gates such as inverters, NAND, and NOR gates. Section 4 presents the experimental results of the proposed circuit operating at supply voltages of 0.5 V and 0.9 V, along with an analysis of temperature variation effects. Finally, section 5 concludes the study.

2. A PROPOSED OPTIMIZED SPACAER DETECTOR CIRCUTS

C-ternary combinational logic circuits consist of two main parts: C-ternary combinational logic circuits and Spacer Detector (SD) circuits. The SD circuits are constructed of H-elements and L-elements, as shown in Fig. 1. The outputs from these H-elements and L-elements are connected to a binary XOR gate, determining whether the input signal is a spacer signal. The XOR gate is implemented using transmission gate logic. When the input signal is identified as a spacer, the output is set to logic "1". Each input signal is processed by its corresponding SD circuit, and the output signals from all SD circuits are connected to an NOR gate, which we refer to as the S signal. The SN signal represents the data of the input signal.

The main parts of the H-element and L-element have been presented in [27], which are based on a pseudo-differential amplifier that lacks a tail current source; thus, they can operate at a low supply voltage.

In this study, we have developed an optimized L-element that leverages the negative feedback loop from the H-element. As a result, we can eliminate the need for a pseudo-differential amplifier in the L-element.

The H-element is constructed around a pseudo-differential amplifier, as shown in Fig. 2. This amplifier operates by comparing two input voltages applied to the pMOS transistor M_{11}. A voltage divider, composed of transistors M_6 and M_7, generates an output voltage that is influenced by the amplifier's output. The inverter provides the bias voltage for the pMOS transistor M_6 and the nMOS transistor M_7. The pMOS transistor M_{11} senses an input voltage that is greater than half of the supply voltage $(V_{DD}/2)$, while the pMOS transistor M_8 experiences a lower input voltage compared to M_6. The inverter then outputs a signal that is the opposite of

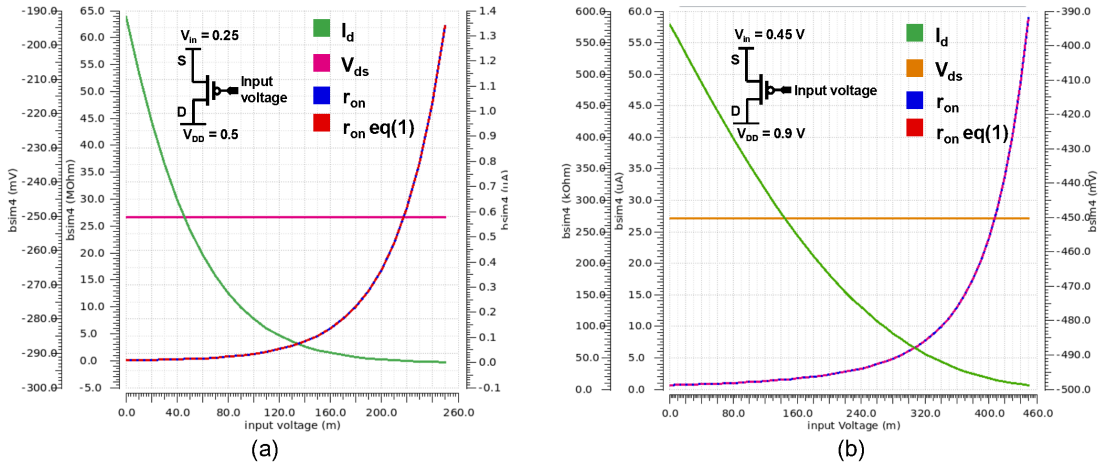


***Fig. 4**: The on-resistance (R_{on}) of the pMOS transistor was compared between simulation results and the theoretical values calculated using Eq. (1), under two operating conditions: (a) when the drain (D) was set to 0.5 V, and (b) when the drain was set to 0.9 V. In both cases, the source (S) voltage was defined as half the corresponding drain voltage.*

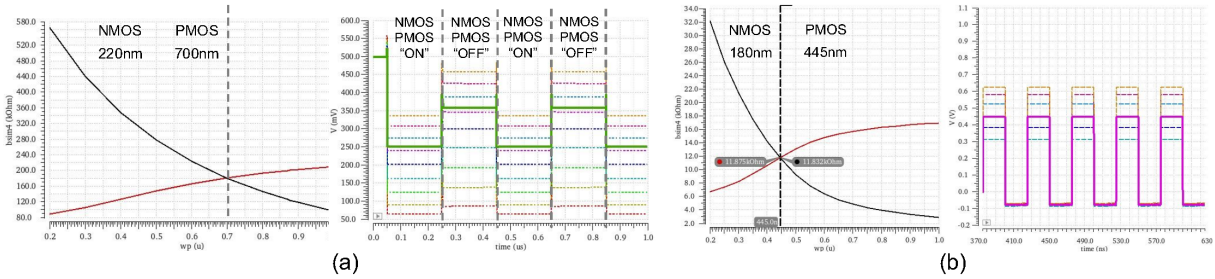


***Fig. 5**: The results of equivalent on-resistance of pMOS and nMOS transistors at (a) 0.5 supply voltage operation and (b) 0.9 supply voltage operation its output voltage dependent on on-resistance (R_{on}) value of pMOS and nMOS transistors. The on-resistance (R_{on}) of the pMOS transistor was compared between simulation results and the theoretical values.*

the input, with a voltage swing from the maximum to minimum levels. H-element generates a logical output of "1" when the input signal value exceeds (V_{DD}/2). In this case, the current mirror comprises nMOS transistors instead of pMOS transistors.

The L-element produces a logical output of "1" when the input signal is at a high voltage level equal to the supply voltage, as shown in Fig. 2. In this design, a common-source (CS) stage with a pMOS diode-connected load outputs a low voltage when the nMOS transistor M_2 detects a standard input voltage. This low voltage is then used as a bias input in a negative feedback loop to control the pMOS transistors M_3. As a result, M_3 turns ON and restores the output voltage derived from the CS stage, which remains low when the input is high. The resulting output signal is passed through an inverter, producing a rail-to-rail voltage swing and yielding the final inverted output.

3. A LOW-VOLTAGE C-TERNARY LOGIC

3.1 C-ternary combinational logic circuit

This section describes the low voltage C-ternary inverter, C-ternary-NAND, and C-ternary NOR gate, the combinational circuit that combines the S and SN signals from the SD circuits to control their output, as shown in Fig. 2. When the signal at S is low, and SN is high, the transistors connected to the networks are ON, and the data signal comes out.

The ternary buffer generates a spacer signal which is logical middle value (V_{DD}/2). In [25 – 26], the ternary buffer is constituted by a CMOS gate connected to V_{DD}/2; hence, that circuit was applied more than the supply source. This study emphasized circuits that operated by a one value of supply voltage (V_{DD}/2). Therefore, the ternary buffer constitutes a source follower with a pMOS load in which the drain (D) is connected to the supply voltage, as shown in Fig. 3. When the signal at S is high, and SN is low, the transistors connected to the networks are ON; thus, the transistors operate in the triode region.

Consequently, MOSFETs in ternary buffer are responsible for on-resistance (R_{on}), which is characterized by Eq. (1). as well as operating in the subthreshold region. The drain current (I_d) varies depending on the region of operation of MOSFET [28].

$$R_{on} \approx \frac{V_{ds}}{I_d} \approx \frac{1}{\mu_c C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \quad (1)$$

Figure 4 illustrates the on-resistance (R_{on}) of the pMOS transistor in a ternary buffer configuration, where the drain (D) is connected to the supply voltage at 0.5 V and 0.9 V, as shown in Fig. 4(a) and 4(b), respectively. The source (S) is connected to the output of the C-ternary logic. The on-resistance (R_{on}) is plotted as a function of the input voltage, represented by the SN signal, which varies from 0 to half of the supply voltage. The simulation results are compared with the theoretical values calculated using Eq. (1). There was no significant difference observed between the simulation results, indicated by the blue line, and the theoretical values, indicated by the dashed red line, confirming the accuracy of the analytical model expressed in Eq. (1).

All MOSFETs in ternary buffer can operate as a resistor whose the resistance value is controlled by the overdrive voltage. The output voltage is expressed by Eq. (2).

$$V_{out} = V_{DD}\frac{R_{on,pmos}}{R_{on,pmos} + R_{on,nmos}} \quad (2)$$

The on-resistance (R_{on}) of pMOS and nMOS transistors might be the identical value. The Eq. (1) is the step forward to determine the sizing of pMOS and nMOS transistors due to on-resistance (R_{on}) depending on $\mu_C C_{OX}$, the device dimension, and aspect ratio of W/L. We estimate the sizing transistor by using Cadence Virtuoso and plot out of the on-resistance (R_{on}), as shown in Fig.5(a). The size of the nMOS transistor was set to 220 nm, and the pMOS transistor size was determined by sweeping width over range of 200 nm to 1 μm.

3.2 C-ternary inverter, NAND and NOR gate

The C-ternary inverter gate relies on the CMOS inverter connected to S and SN signals to control the inverter output. The schematic and the truth table of C-ternary inverter shown in the Fig.6(a). The pMOS transistor M_1 and nMOS transistor M_4 are inverter gate. If the input voltage is a spacer, the output will be a logical middle value generated by the ternary buffer. Fig.6(b) shows the output of the C-ternary inverter operating at 0.5 supply voltage with different nMOS and pMOS transistor sizing, in which the ternary buffers have identical on-resistance (R_{on}). The functional operation remains the same, whereas the power consumption, including that of the SD circuits, does not differ significantly, as shown in Table 1. However, the configuration with a 700nm pMOS and a 220nm nMOS resulted in lower power consumption than the others.

In addition, the schematics and truth tables of the C-ternary NAND and NOR gates, each with two input signals, are shown in Fig.7(a) and Fig.7(b), respectively. The input signals, In1 and In2, can represent either data or spacer values. The control signals S and SN determine the output, and logical middle value are generated when one or both inputs are in the spaced logic by the ternary buffer.

***Table 1**: Size of ternary buffer circuits.*

C-ternary NOT gate		Power
pMOS (M_6)	nMOS (M_5)	(μW)
870n	85n	2.983
728n	150n	2.935
700n	220n	2.927
800n	330n	2.959

***Table 2**: Size of transistor used in SD Circuits.*

L-element		H-element	
transistor	W	transistor	W
M_1	6.4 μ	M_6	2.2 μ
M_2	1.8 μ	M_7	640 n
M_3	1.8 μ	M_8, M_{11}	2.7 μ
M_4	4 μ	M_9, M_{10}	1.8 μ
M_5	2 μ	M_{12}, M_{13}	4 μ

***Table 3**: Power consumption of SD Circuits depended on supply voltage.*

Supply Voltage	Power (μW)	
	In [27]	This work
0.35	0.082	0.062
0.40	0.309	0.233
0.45	1.093	0.825
0.50	3.329	2.524
0.60	18.27	14.17
0.70	60.4	47.21
0.80	144.6	112.8
0.90	281.1	218.1

4. RESULTS AND ANALYSIS

The proposed SD circuit and C-ternary inverter, as well as the NAND and NOR circuit, were designed and simulated by the Cadence Virtuoso analog design environment. The simulation results are based on a typical process corner and a temperature of 27 ℃. All the MOS transistors are implemented on the UMC LL process in which the lengths of transistors are 65nm. The threshold voltage of the pMOS transistor is approximately 0.45 volts, while that of the nMOS is approximately 0.54 volts. When the circuit operates at 0.5 volts, it operates at a near-threshold voltage.

4.1 Optimized Spacer Detector Circuits

The voltage transfer characteristics (VTC) of the SD circuit were simulated to evaluate the behaviour of the proposed H-element and L-element circuits under varying supply voltages. The simulation results, which illustrate the changes in output voltage corresponding to different supply voltage levels, are shown in Fig. 8(a) and 8(b) for the voltage ranges of 0.35 V to 0.5 V and 0.6 V to 0.9 V, respectively. The width of the transistors utilized in the H- and L-elements is detailed in Table 2.

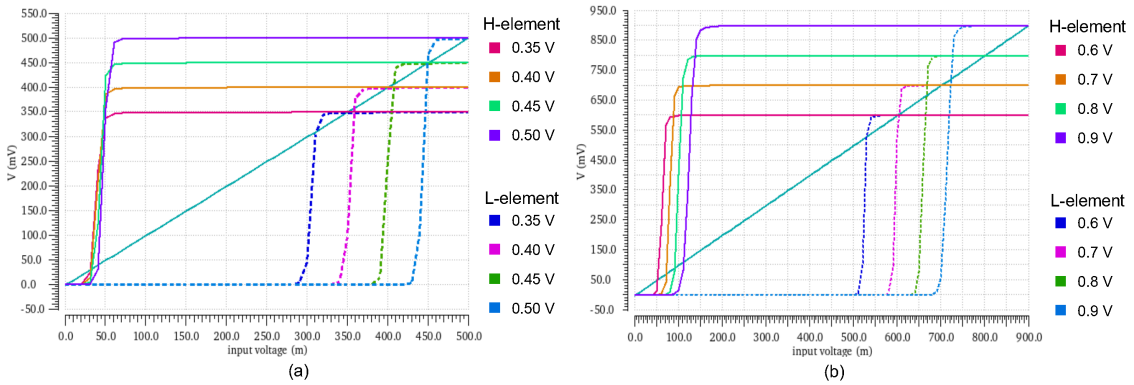


***Fig. 6**: The voltage transfer curve (VTC) simulation results of the SD circuit with (a) sub- or near-threshold supply voltage and (b) near-threshold and nominal supply voltage.*

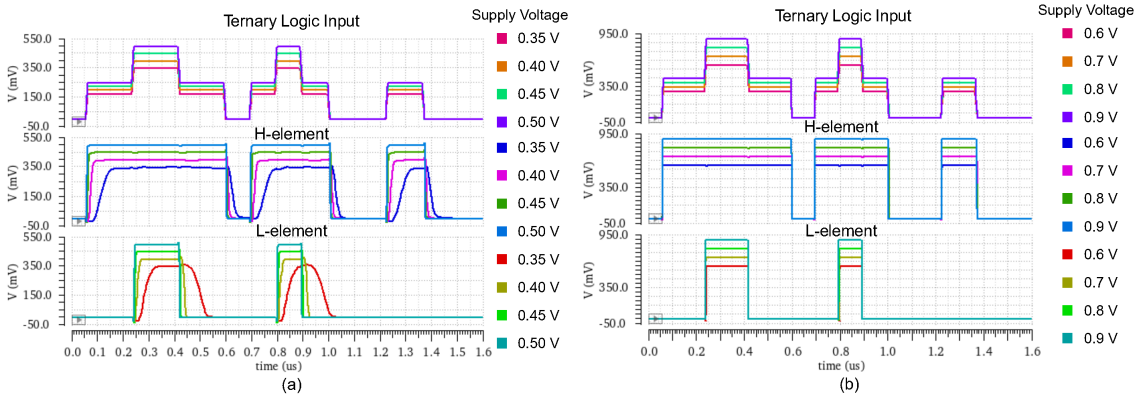


***Fig. 7**: The input waveform of H- and L-element at (a) voltage range of 0.35 to 0.5 voltage operation and (b) at voltage range of 0.6 to 0.9 voltage operation, and the corresponding output waveforms exhibit.*

According to H and L element operation function, the ternary logic is given the input signal corresponding as 0 1/2 1 1/2 0 and 0 1/2 0. The output waveforms of the L-element and H-element with a 0.35 – 0.5 supply voltage and a 0.6 – 0.9 supply voltage are shown in Fig. 9(a), and Fig. 9(b), respectively.

The power consumption of the SD circuit varies with the applied supply voltage, which ranges from 0.35 to 0.9 volts, as shown in Table 3. We also compare the result with [27], in which the L-element relied on the pseudo-differential amplifier. Consequently, the power consumption of the new SD was lower than work in [27] by approximately 25%.

4.2 Delay analysis of optimized spacer detector circuits

Since each input signal is processed by its corresponding SD circuit, the output signals from all SD circuits are connected to a NOR gate to determine the spacer when S yield high logic or data when SN yields high logic. Figure 10 shows the output of the S, and SN signals to control signal for all the C-ternary combinational logic gates at 0.5 operating voltage, indicating a small delay between S and S2, and SN and SN2. Therefore, the propagational delay might be determined when the C-ternary combinational logic gates are implemented in any arithmetic circuit.

The proposed C-ternary combinational logic circuit is composed of a ternary buffer circuit that behaves as a resistance to divider voltage to logical middle value ($V_{DD}/2$). Therefore, the resistance, as expressed in Eq. (3), is one of the key factors affecting propagation delays when C-ternary combinational logic circuits are cascaded or connected with fan-out.

$$t_{pd} = \sum_i R_i C_i \approx (1+h)\,RC \tag{3}$$

Where h denotes the fan-out count, R represents the total effective resistance along the path from the input node to the output node, and C is the sum of the input capacitances at each node (denoted as node **i**) along with the load capacitance [29].

We demonstrated the propagation delay by using a C-ternary delay circuit, the construction of which is shown in Fig.11(a). The output of Out2 is varied by different fan-out counts. The shape of the waveform appears as a small glitch when the number of fan-out is more than the fan-out-8 inverter, as shown in Fig.11(b). Additionally, fan-out count varies the propagation delay with different

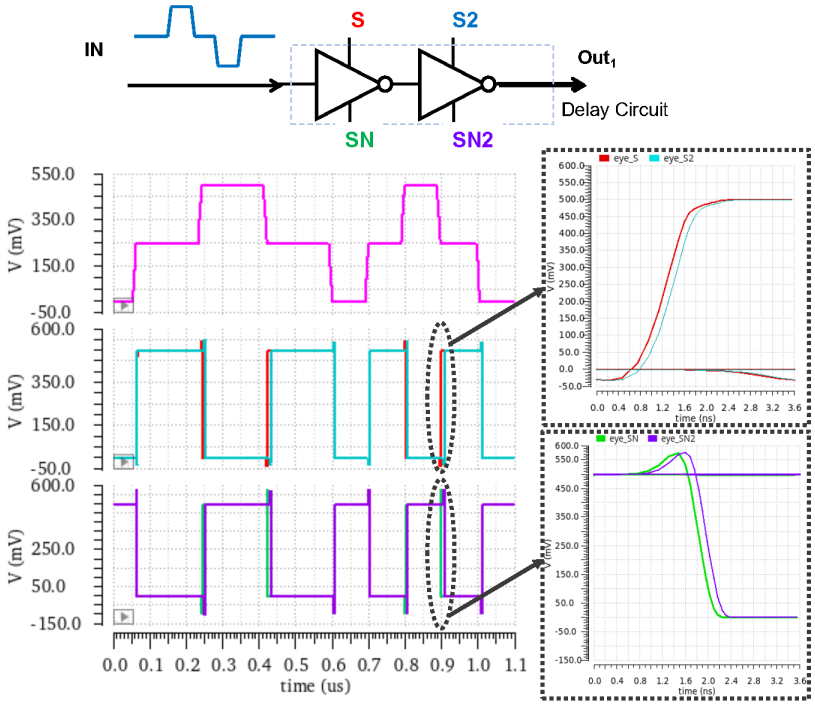


***Fig. 8**: The eye diagram results show the delay characteristics of the S and SN signals, which serve as control signals for the two C-ternary delay circuits.*

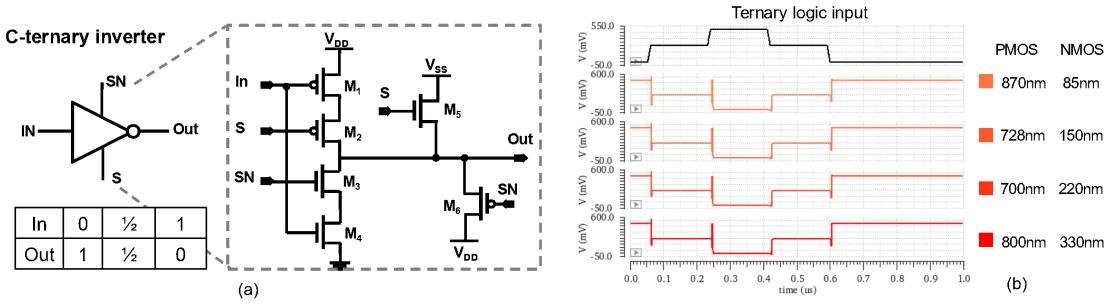


***Fig. 9**: (a) Schematic of proposed C-ternary inverter and its truth table (b) The simulation results of C-ternary inverter operating at 0.5 supply voltage with different transistor sizing of ternary buffer.*

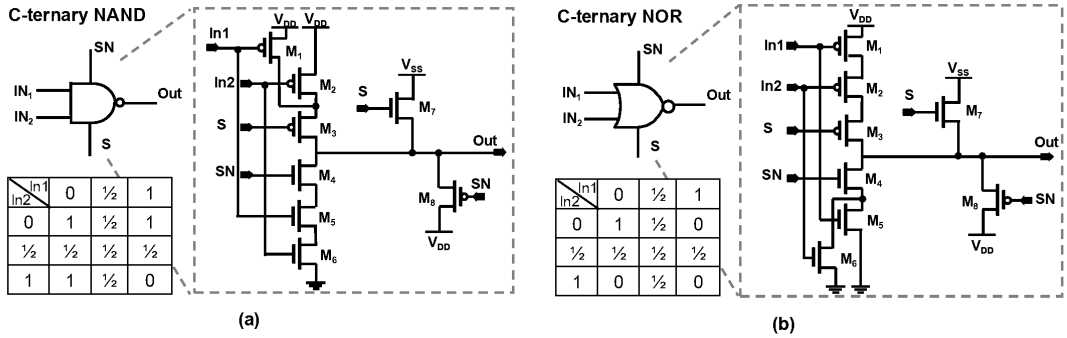


***Fig. 10**: Schematic of proposed (a) C-ternary NAND gate and its truth table, and (b) C-ternary NOR gate and its truth table*

transistor sizes of pMOS and nMOS in a ternary buffer, which are shown in Fig.11(c), demonstrating that there was no significant difference in propagation delay among them when the fan-out count is not more than fan-out-4 inverter due to the capacitance value.

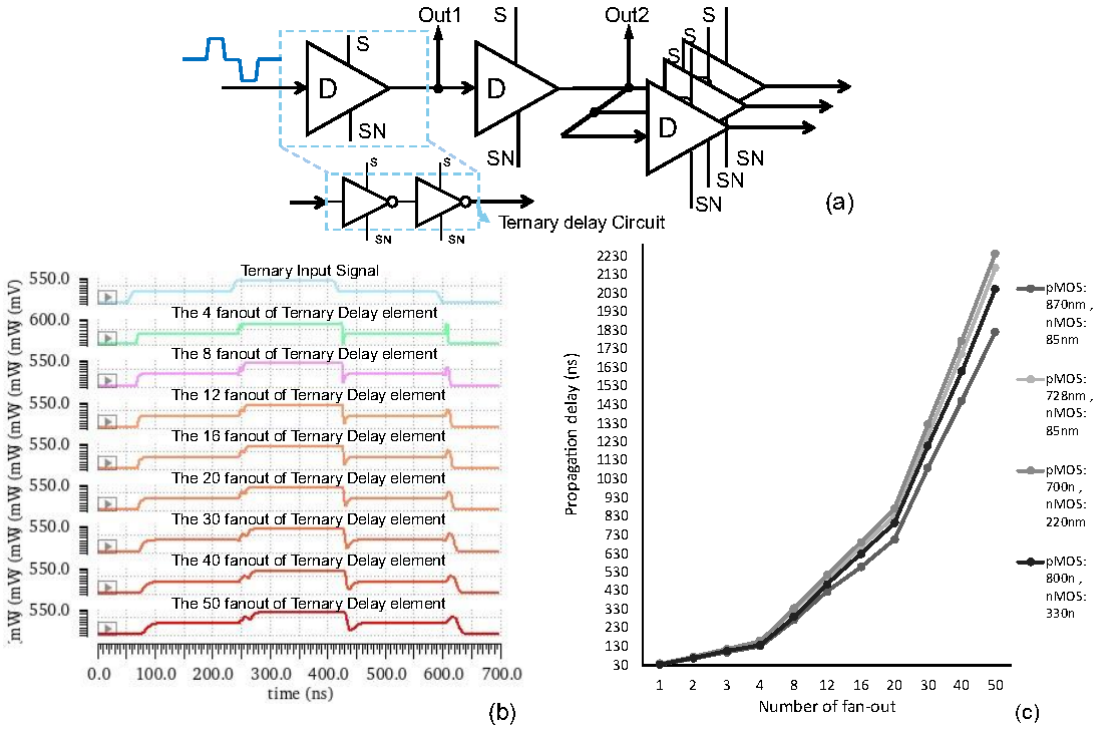


***Fig. 11**: The propagation delay affected the output voltage of (a) C-Ternary delay circuits with a variation of fan-out count and (b) corresponding output of Out2 and (c) the propagation delay of variation of transistor sizing of the ternary buffer circuit along with a variation of fan-out count.*

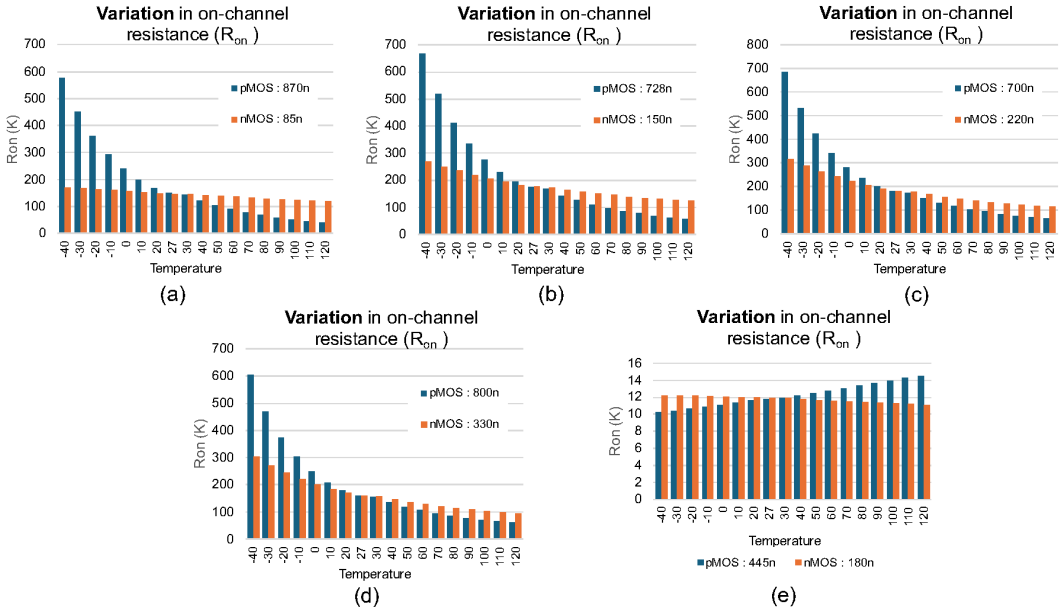


***Fig. 12**: The results of equivalent on-resistance (R_{on}) of pMOS and nMOS transistors (a)-(d) at 0.5 supply voltage operation and (e) at 0.9 supply voltage operation which those on-resistance (R_{on}) are variant of temperature from -40℃ to 120℃.*

4.3 C-ternary Combinational logic Circuits

The C-ternary combinational logic circuits are controlled by two signals - S and SN. The output of the operation function depends on the input signal and the S and SN signals.

Table 4 shows the widths of the transistors in C-ternary inverter, NAND, and NOR Circuits operating at 0.5 supply voltage and 0.9 supply voltage. However, only

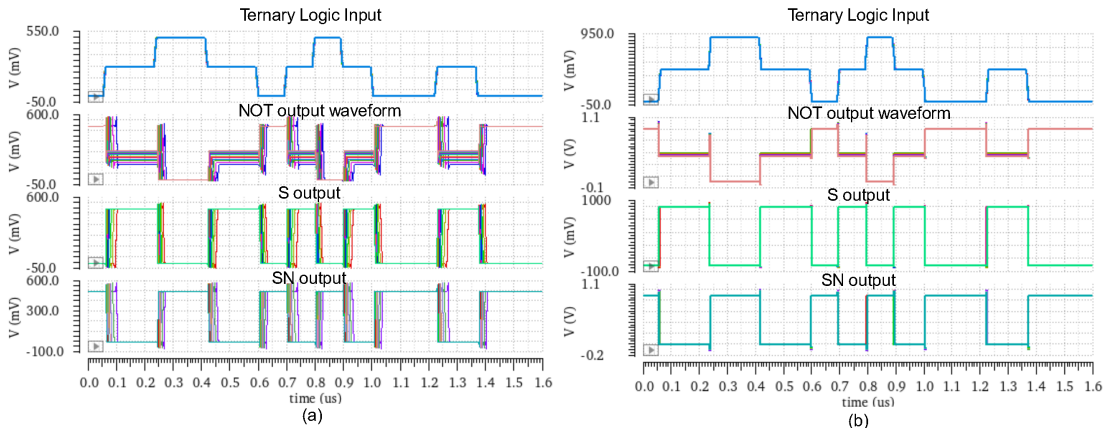


***Fig. 13**: Different output of C-ternary inverter when temperature variation from -50℃ to 50℃ (a) at 0.5 operating voltage and (b) at 0.9 operating voltage.*

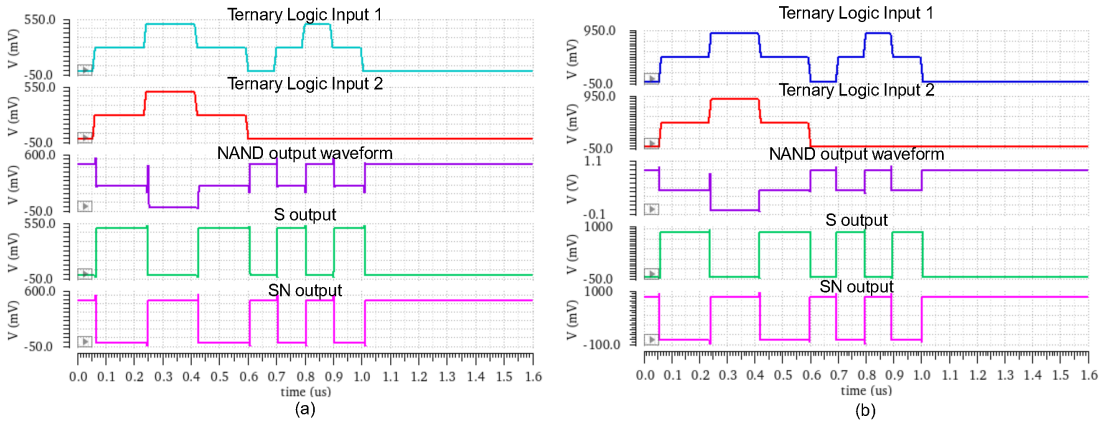


***Fig. 14**: The simulation result of C-ternary NAND circuit (a) at 0.5 operating voltage and (b) at 0.9 operating voltage.*

***Table 4**: Size of transistor used in C-ternary inverter, NAND and NOR gate.*

C-ternary NOR (NAND)		C-ternary inverter	
transistor	W	transistor	W
M_1, M_2	350 n	M_1	350 n
M_3	1 µ	M_2	1 µ
M_4	450 n	M_3	450 n
M_5, M_6, M_7	220 n	M_4, M_5	220 n
M_8	700 n	M_6	700 n

the widths of the transistors of the ternary buffer circuit in C-ternary inverter, NAND, and NOR gate were 445nm pMOS and 180nm nMOS, as shown in Fig. 5(b).

Figure 12 (a) - (d) shows the functional operation of the C-ternary inverter operating at a 0.5 supply voltage. The threshold voltage and on-resistance (R_{on}) of each device can be affected by temperature variations [30]. We simulated the C-ternary inverter with different pMOS and nMOS transistor sizing in the ternary buffer circuit, operating at a 0.5 supply voltage across a temperature range from -40℃ to 120℃. pMOS transistor in the ternary buffer is more sensitive to temperature than nMOS transistor. The results of the pMOS and nMOS transistors in the ternary buffer of a C-ternary inverter operating at a 0.9 supply voltage are not significantly varied by temperature, as shown in Fig. 12(e).

The transient analysis of C-ternary inverter operating at 0.5 supply voltage across a temperature range of -50℃ to 50 ℃, shows in Fig.13(a) which characteristic of the middle value significantly fluctuated. Meanwhile, the temperature variation of the C-ternary inverter operating at 0.9 supply voltage showed a slight fluctuation in the middle voltages, as shown in Fig. 13(b).

The two input C-ternary signals and their C-ternary NAND waveforms at 0.5 supply voltage and 0.9 supply voltage are shown in Fig.14(a) and Fig.14(b), respectively. Additionally, the two input C-ternary signals and their C-ternary NOR waveforms at 0.5 supply voltage and 0.9 supply voltage are shown in Fig.15(a) and Fig.15(b), respectively. Our proposed C-ternary combinational logic gates are satisfied with its truth table.

The average power consumption of the C-ternary inverter circuit, including the SD circuit, was 3.067 μW. In addition, the average power consumption of the C-ternary NAND and NOR circuit operating at 0.5 voltage, including two SD circuits due to the two ternary input

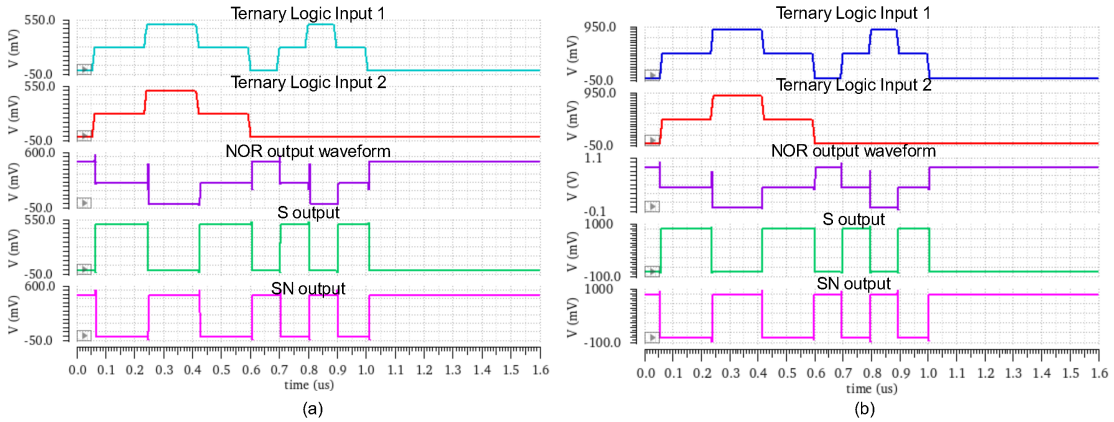


***Fig. 15**: The simulation result of C-ternary NOR circuit (a) at 0.5 operating voltage and (b) at 0.9 operating voltage.*

signals, was 3.93 µW. Meanwhile, the average power consumption of the C-ternary NAND and NOR circuit operating at 0.9 voltage was 234.8 μW.

5. CONCLUSION

This study introduced low-voltage C-ternary inverter, NAND, and NOR gate that efficiently perform according to their truth table. The proposed circuits employed a new ternary buffer to yield a logical middle value when the input signal is a spacer in order to utilize one supply voltage. The C-ternary combinational logic circuit is controlled by a spacer detector circuit. We also presented an optimized spacer detector circuit for a small transistor cost. The proposed circuit can operate at sub- and near-threshold voltage levels. Temperature and capacitance affected the middle voltage value of the ternary buffer at sub-threshold operation. In future work, we will improve the ternary buffer to compensate for the temperature variation in CMOS technology.

REFERENCES

[1] T. E. Williams, *Self-timed rings and their application to division*, PhD. Thesis, Stanford University, Stanford, CA, USA, 1992.

[2] T. Felicijan and S. B. Furber, "An asynchronous ternary logic signaling system," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 6, pp. 1114 –1119, Dec. 2003.

[3] J.-M. Philippe, E. Kinvi-Boh, S. Pillement, and O. Sentieys, "An energy-efficient ternary interconnection link for asynchronous systems," in *Proceedings of 2006 IEEE International Symposium on Circuits and Systems*, May 2006, p. 4 – 1014.

[4] E.-J. Choi, K.-R. Cho, and J.-H. Lee, "New Data Encoding Method with a Multi-Value Logic for Low Power Asynchronous Circuit Design," in *36th International Symposium on Multiple-Valued Logic (ISMVL'06)*, May 2006, pp. 4–4.

[5] A. Doostaregan, M. H. Moaiyeri, K. Navi, and O. Hashemipour, "On the design of new low-power CMOS standard ternary logic gates," in *2010 15th CSI International Symposium on Computer Architecture and Digital Systems*, Sep. 2010, pp. 115–120.

[6] G. Thrishala and K. Ragini, "Design and Implementation of Ternary Logic Circuits for VLSI Applications," *International Journal of Innovative Technology and Exploring Engineering*, vol. 9, no. 4, pp. 3117–3121, Feb. 2020.

[7] G. Zhao, Z. Zeng, X. Wang, A.G. Qoutb, P. Coquet, E.G. Friedman, B.K. Tay, and M. Huang, "Efficient Ternary Logic Circuits Optimized by Ternary Arithmetic Algorithms," *IEEE Transactions on Emerging Topics in Computing*, vol. 12, no. 3, pp. 826–839, Jul. 2024

[8] J. Ko, K. Park, S. Yong, T. Jeong, T. H. Kim, and T. Song, "An Optimal Design Methodology of Ternary Logic in Iso-device Ternary CMOS," in *2021 IEEE 51st International Symposium on Multiple-Valued Logic (ISMVL)*, May 2021, pp. 189–194.

[9] J. Ko, J. Kim, T. Jeong, J. Jeong, and T. Song, "Exploration of Ternary Logic Using T-CMOS for Circuit-Level Design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 9, pp. 3612–3624, Sep. 2023.

[10] A. S. Vidhyadharan and S. Vidhyadharan, "A novel ultra-low-power CNTFET and 45 nm CMOS based ternary SRAM," *Microelectronics Journal*, vol. 111, p. 105033, May 2021.

[11] E. Abbasian, S. Sofimowloodi, and A. Sachdeva, "Highly-Efficient CNTFET-Based Unbalanced Ternary Logic Gates," *ECS Journal of Solid State Science and Technology*, vol. 12, no. 3, p. 031007, Mar. 2023.

[12] S. Kim, S.-Y. Lee, S. Park, K. R. Kim, and S. Kang, "A Logic Synthesis Methodology for Low-Power Ternary Logic Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 9, pp. 3138–3151, Sep. 2020.

[13] C. K. Vudadha and M. Srinivas, "Design Methodolo-gies for Ternary Logic Circuits,"

in *2018 IEEE 48th International Symposium on Multiple-Valued Logic (ISMVL)*, May 2018, pp. 192–197.

[14] K. Chauhan, S. Mittra, R. Sinha, and D. Bansal, "Noise Margin analysis of Efficient CNTFET-based Standard Ternary Inverter," in *2023 International Conference for Advancement in Technology (ICONAT)*, Jan. 2023, pp. 1–7.

[15] R. A. Jaber, A. M. Haidar, A. Kassem, and F. Zahoor, "Ternary Full Adder Designs Employing Unary Operators and Ternary Multiplexers," *Micromachines*, vol. 14, no. 5, Art. no. 5, May 2023.

[16] Z. T. Sandhie, F. U. Ahmed, and M. H. Chowdhury, "Design of Ternary Logic and Arithmetic Circuits Using GNRFET," *IEEE Open Journal of Nanotechnology*, vol. 1, pp. 77–87, 2020.

[17] B. D. Madhuri and S. Sunithamani, "Design of ternary logic gates and circuits using GNRFETs," *IET Circuits, Devices & Systems*, vol. 14, no. 7, pp. 972–979, 2020.

[18] Yang, H. Lee, J. H. Jeong, T. H. Kim, S.-H. Lee, and T. Song, "A Practical Implementation of the Ternary Logic Using Memristors and MOSFETs," in *2021 IEEE 51st International Symposium on Multiple-Valued Logic (ISMVL)*, May 2021, pp. 183–188.

[19] X.-Y. Wang, C.T. Dong, P.F. Zhou, S.K. Nandi, S.K. Nath, R.G. Elliman, H.H.C. Iu, S.M. Kang, and J.K. Eshraghian, "Low-Variance Memristor-Based Multi-Level Ternary Combinational Logic," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 6, pp. 2423–2434, Jun. 2022.

[20] G.-C. Lizeth, T. Asai, and M. Motomura, "Low-power asynchronous digital pipeline based on mismatch-tolerant logic gates," *IEICE Electronics Express*, vol. 11, no. 15, pp. 20140632–20140632, 2014.

[21] Y. Shizuku, T. Hirose, N. Kuroki, M. Numa, and M. Okada, "Energy-efficient AES SubBytes transformation circuit using asynchronous circuits for ultra-low voltage operation," *IEICE Electron. Express*, vol. 12, no. 4, pp. 20141157–20141157, 2015.

[22] A. Wheeldon, J. Morris, D. Sokolov, and A. Yakovlev, "Self-timed, minimum latency circuits for the internet of things," *Integration*, vol. 69, pp. 138–146, Nov. 2019.

[23] Z. Zhu, Y. Yu, X. Bai, S. Qiao, and Y. Hei, "Snake: An asynchronous pipeline for ultra-low-power applications," *IEICE Electron. Express*, vol. 16, no. 12, pp. 20190293–20190293, 2019.

[24] A. Wheeldon, A. Yakovlev, R. Shafik, and J. Morris, "Low-Latency Asynchronous Logic Design for Inference at the Edge," in *2021 Design, Automation \& Test in Europe Conference & Exhibition (DATE)*, Feb. 2021, pp. 370–373.

[25] Y. Nagata and M. Mukaidono, "Design of an asynchronous digital system with B-ternary logic," in *Proceedings 1997 27th International Symposium on Multiple- Valued Logic*, May 1997, pp. 265–271.

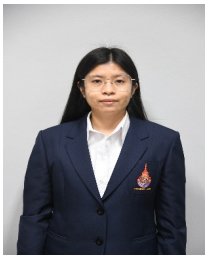
[26] T. Bunnam and A. Thongtak, "An Approach for the Delay Simulation of D-Inverter in C-Ternary Logic Circuits," in *Proceedings of the 2008 International Conference on Computer Design, CDES 2008*, Las Vegas, Nevada, USA, July 14-17, 2008, H. R. Arabnia, Ed., CSREA Press, 2008, pp. 224–228.

[27] P. Srikram and T. Bunnam, "A Design of Low Voltage Spacer Detector Circuits for Asynchronous Ternary Logic System," in *TENCON 2023 - 2023 IEEE Region 10 Conference (TENCON)*, Oct. 2023, pp. 460–463.

[28] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. USA: McGraw-Hill, Inc., 2000.

[29] N. H. E. Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed., Boston, MA, USA: Addison-Wesley, 2010.

[30] S. Kalra, "Effect of temperature dependence on performance of Digital CMOS circuit technologies," in *2013 International conference on signal processing and communication (ICSC)*, Dec. 2013, pp. 392–395.



Pitchayapatchaya Srikram received the B.Eng. degree in Electronic and Computer system from Silpakorn University, Thailand, in 2012, the M.Eng. degree in Computer Engineering from Chulalongkorn University, Thailand, in 2016, and and Ph.D degree in Electronics for Informatics from the Functional Communication Device and Circuits Laboratory at RCIQE, Hokkaido University, Sapporo, Japan in 2023. She is currently an Assistant Professor in Computer Engineering at Rajamangala University of Technology Thanyaburi (RMUTT), Thailand. Her current research interests are analog and mixed-signal IC design and intelligent image processing at edge device.

Thanasin Bunnam received the B.Eng. degree in Computer Engineering from Mahidol University, Thailand, in 2005, the M.Eng. degree in Computer Engineering from Chulalongkorn University, Thailand, in 2009, and the Ph.D. degree from the uSystem Research Group, Newcastle University, U.K., in 2021. He is currently an Assistant Professor in Computer Engineering at Rajamangala University of Technology Thanyaburi (RMUTT), Thailand. His research interests include in-memory computing, memristors and memristive circuits, circuits and systems for energy-efficient AI, and IoT systems for agriculture.