A High-Efficiency Low Dropout Regulator in 180 nm CMOS for Power-Constrained SoC Applications

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ABSTRACT

Low Dropout Regulators (LDO) are crucial for modern System-on-Chip (SoC) platforms, especially in battery-operated and noise-sensitive applications such as biomedical and analog sensor interfaces. This work presents the design and simulation of a compact low-voltage LDO implemented in 180 nm CMOS technology. The proposed design employs a PMOS pass transistor, a resistive feedback network for precise voltage regulation, and a two-stage differential error amplifier with Miller compensation to ensure frequency stability. Operating from a 1.8 V supply, the regulator provides a stable 1.6 V output with a minimum dropout voltage of 200 mV. It supports a load current range of 1 μA–10 mA, achieving a phase margin of 60°, a gain-bandwidth product of 7.57 MHz, and a low quiescent current of 10 μA. The LDO demonstrates a PSRR of −54 dB at 1 kHz and maintains robust performance under supply noise and load transients. Simulation results confirm minimal overshoot, fast settling time, and strong stability. The design's compact area and absence of external components make it well-suited for area- and power-constrained SoC integration, offering an effective balance between efficiency, noise performance, and implementation simplicity.

Keywords: Low Dropout Regulators, Power Supply Rejection Ratio, Power Management, Chip, Load, Signal Integrity

1. INTRODUCTION

In today's electronic devices like handheld biomedical devices, wearable sensors, and system-on-chip (SoC) platforms, power management is absolutely essential for maintaining operational stability and energy efficiency. Power management units (PMUs) consist of generally a rectifier, a bandgap reference (BGR), and a LDO voltage regulator [1], [2]. Among them, the LDO is tasked with providing a stable noiseless output voltage despite input fluctuations or load changes. Its major advantage comes from its capability to regulate the output voltage with only a small input-to-output voltage difference—referred to as the dropout voltage [3], [4]. A typical LDO configuration consists of an error amplifier (EA), a pass transistor (PMOS or NMOS), and a resistive feedback network [5], [6]. The EA compares the reference voltage to a scaled feedback from the output and controls the gate of the pass element to ensure a stable voltage. The simplicity of operation makes LDOs very well-suited for integration in noise-sensitive analog and RF applications.

The choice of the pass transistor has a major impact on the overall performance of the LDO. While the transistors of NMOS provide greater transconductance and improved PSRR, they use a gate voltage greater than the input voltage, requiring a charge pump [7], [8]. This causes an increase in design sophistication and power consumption. PMOS pass transistors, on the other hand, offer a low dropout characteristic and simpler design, making them more desirable in low-power applications [9]. For low-frequency and biomedical systems, where simplicity, low noise, and efficiency of power are the most important factors, a design based on PMOS is a more feasible option [10]. Key performance metrics by which an LDO can be assessed are dropout voltage, PSRR, line regulation, and load regulation. Dropout voltages in contemporary LDOs are usually between 200 mV and 500 mV [11]. PSRR, or the LDO's capability to reject input noise or ripple, is heavily dictated by the structure and gain of the EA [12], while line and load regulation indicate the LDO's ability to keep output stable for changing supply and load conditions [13].

The error amplifier has to be properly designed to attain high PSRR, stable transient performance, and minimum power consumption. A differential amplifier topology is typically utilized because of its high gain and good common-mode rejection ratio (CMRR) [14]. In addition, stability is an important issue with multi-stage amplifier implementations. Though added complexity is caused by some sophisticated compensation techniques, Miller compensation provides a stable and effective way for frequency stabilization without incurring meaningful circuit overhead [15]. In this paper, an on-chip LDO circuit is improved with a differential two-stage EA, a PMOS passes element, and a Miller compensation. Together, these are used to create a low-complexity, low-dropout solution with good PSRR, ideal for integration into low-frequency, low-power biomedical SoC applications. The

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contribution of this work is describe as follows:

- The 180 nm standard CMOS process is utilized to develop a totally integrated LDO regulator without requiring charge pumps or specialized fabrication techniques, thereby facilitating integration into low-cost SoC platforms.
- The LDO utilizes a PMOS pass element to deliver a low dropout voltage with reduced complexity without gate boosting, rendering it applicable to biomedical and low-frequency analog applications.
- A two-stage error amplifier is used with differential input and Miller compensation to provide frequency stability with a phase margin of over 60° and a gain-bandwidth product of about 7.5 MHz.
- It has excellent power supply rejection and low quiescent current (10 μA) while finding a balance between noise suppression and energy efficiency for low-power applications.
- The entire regulator is simulated and verified using MATLAB/Simulink simulations and exhibits excellent load regulation, line regulation, and transient response over a load current range of 1 μA to 10 mA.

2. LITERATURE REVIEW

There are some research works focused on the design of LDO regulators for efficient power management in system-on-chip (SoC) systems using various technqiues and features. The following is an extensive survey of papers of interest.

Rezaei and Mojarad, [16] presented a general overview of methods of improving PSR in capacitor-less LDO regulators. Their research considers how various circuit-level methods can optimize PSRR in SoC scenarios, including the use of auxiliary amplifiers, ripple injection, and gain boosting techniques. But the paper does not present a consistent or implementable architecture, simulation results to validate the theoretical classifications.

Lee and Park, [17] took into account modeling the load current response of digitally controlled LDOs (DLDOs) using feedback and feedforward control structures. This is beneficial for system-level design, as it allows one to browse the design space quickly without needing to go through a series of heavy simulations. However, applies only to digital LDOs and does not address very critical analog matters such as compensation, phase margin, in analog applications.

In contrast thereto, Xu et al. [18] proposed a new analog LDO regulator with high PSRR and ultra-low quiescent current using a technique known as Capacitive Feed-Forward Ripple Cancellation (CFFRC). This solution has great value in low-power and high-noise-immunity design, but is moderately complex and probably sensitive to component mismatches and layout parasitics, and so may be problematic to integrate and scale.

Bai et al. [19] proposed a Response Surface Methodology (RSM)-based automated multi-objective optimization technique for LDO design. This procedure enables simultaneous parameter optimization of parameters such as the temperature coefficient (TC) and PSRR using only a few simulation points (27 Cadence sampling datasets). By this, it enables designers to sample the design space more economically and achieve improved tradeoffs among competing objectives. While the RSM-based approach has both design productivity and precision, its reliance on EDA tools such as Cadence makes it less universal, whereas the work itself focuses on design methodology rather than proposing a new circuit structure.

Liu et al. [20] proposed an LDO regulator implemented in Hall sensor front-end circuits and fabricated via a 0.18 μm BCD process. The topology utilizes a two-stage cascode NMOS pass transistor structure that is biased by closed-loop charge pump. This is well-adapted to automotive environments since it provides high PSRR and robust electromagnetic interference (EMI) immunity. However, the use of NMOS pass transistors introduces the need for a gate voltage boost charge pump, which adds complexity. Niu et al. [21] developed an easy and miniaturized LDO structure with rapid transient response and effective suppression of output overshoot and undershoot. This reduces power dissipation and increases current efficiency without basically increasing chip area, thus easily integratable in SoC. But the architecture is mainly optimized for transient performance and does not put stress on PSRR or noise performance.

Fan et al. [22] designed a high-voltage LDO with the capability of operating in a wide operating temperature range from −55 ℃ to 125 ℃. The regulator is resilient to a broad range of output capacitance (1 to 100 μF) and effective series resistance (ESR) values and is therefore robust under varying external conditions. Though this approach offers low power consumption and strong temperature tolerance, LDMOS technology could fail to operate with standard CMOS flows and the internal feedback complexity could be detrimental to portability and scaling in small ICs.

2.1 Research Gaps and Motivation

Significant research has aimed at enhancing LDO regulator performance, especially in PSR, transient response, low quiescent current, and SoC integration. Capacitor-less solutions based on ripple injection, gain boosting, or auxiliary amplification provide theoretical advantages for PSRR improvement but usually lack unifying architectures and experimental verification. Digital LDO models based on feedback and feedforward control can help predict load behavior but usually ignore analog stability and compensation issues. Certain analog LDOs implement capacitive feed-forward ripple cancellation to minimize supply noise with minimal power, but these present complicated biasing paths and are layout-mismatch sensitive.

Automated optimization tools based on statistical modeling, e.g., response surface methods, facilitate multi-objective tuning but are oriented more toward design methodology rather than circuit creativity. Wide-input

LDOs employing NMOS pass transistors and charge pumps improve EMI immunity but add switching noise and area overhead. Transient-optimized regulators employing direct signal coupling enhance response time at the expense of PSRR and long-term regulation. High-voltage LDOs with LDMOS pass devices have low quiescent current over temperature extremes but suffer from non-standard processes and complex feedback paths. In summary, although previous works solve individual performance metrics, most introduce additional complexity, specialized technologies, or are restricted in CMOS integration. By contrast, the designed LDO fills these gaps with a small, fully CMOS-compatible 180 nm layout having a two-stage amplifier, Miller compensation, PMOS pass device, and resistive feedback with high PSRR, fast transient response, and low quiescent current without external boosting or special structures, making it particularly suitable for analog and biomedical SoC applications.

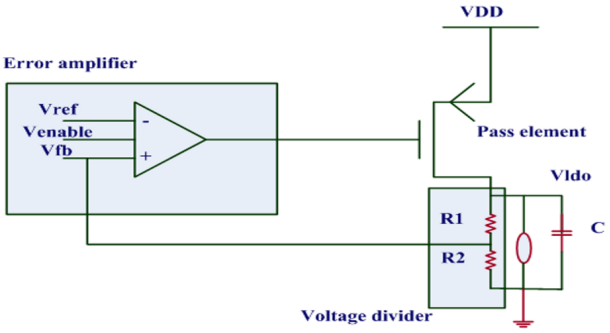

***Fig. 1**: Block Diagram of LDO.*

3. DESIGNING LDO METHODOLOGY

The designed LDO regulator can be used for generating a stable and precise output voltage of 1.6 V from an input supply of 1.8 V, with ultra-low power consumption that needs high PSRR, low dropout, and integration in small CMOS. In this section, the circuit architecture, component-level operation, frequency compensation strategy, transistor sizing, and supporting calculations are discussed. The full deployment is realized through 180 nm CMOS technology, selected for its analog design benefits like superior gain, lower short-channel effects, and larger intrinsic output impedance as opposed to advanced nodes. The 1 µm channel length is a deliberate analog-design choice in the 180 nm process to balance gain, noise, matching, robustness and speed. Compared with minimum-length (≈0.18 µm) devices, increasing channel length reduces short-channel effects (DIBL, velocity-saturation sensitivity) and channel-length modulation, yielding substantially higher output resistance and intrinsic gain. Higher intrinsic gain is critical for the two-stage error amplifier to achieve the targeted 60° phase margin and −54 dB PSRR without resorting to large bias currents. Longer devices also improve device matching and reduce threshold-voltage mismatch scales approximately with $1/\sqrt{(W \cdot L)}$—which is important for the resistive feedback network and low-offset operation at µA bias levels. From a noise standpoint, flicker (1/f) noise is reduced by increasing device area (W·L), lowering the flicker corner and improving low-frequency PSRR and output noise performance required for biomedical and sensor interfaces.

Trade-offs were considered: larger L increases parasitic capacitances and reduces intrinsic bandwidth. This was offset by conservative device sizing and Miller compensation, allowing the design to meet the measured GBW of 7.57 MHz and fast transient response with only 10 μA quiescent current. Finally, larger L improves reliability (lower hot-carrier stress and leakage), which is important for SoC longevity. Post-layout and corner simulations verified that the 1 µm choice provides the desired gain, noise, matching and stability across PVT and load ranges, justifying its selection.

3.1 System Architecture

The block diagram of a LDO is shown in Fig. 1, with a disable pin consisting of several key components: the input voltage (Vin), which supplies power to the LDO; a PMOS transistor that serves as a switch controlled by the disable pin, allowing the output voltage to be cut off when not needed [23]. A reference voltage (Vref) source is for providing a stable reference in terms of output regulation-an error amplifier (EA) taking a comparison between Vout and Vref, then generating a signal to control pass element adjustment. A pass element is usually a PMOS transistor whose output voltage is manifested by controlling its resistance in accordance with the control signal. A feedback network consisting of resistors samples the output voltage and feeds it back to the error amplifier to maintain the desired output voltage level. An output capacitor (Cout) that stabilizes the output voltage and smooths out fluctuations; and finally, the load, which represents the device powered by the LDO output. The addition of the quiescent current source, which provides a small amount of current for the internal circuitry when unloaded, is also crucial for the proper operation of the LDO.

LDO regulators are categorized by their use of an output capacitor. The zero is produced by having an equivalent series resistance (ESR), generally ranging from 10Ω to 0.01Ω. In conjunction with the capacitance, this ESR produces a frequency-dependent path to ground and therefore a zero, which alters the frequency response of the LDO, generally improves stability. Fig 2 shows the LDO schematic diagram.

The transistor-level schematic of the suggested LDO regulator is shown in Fig. 2. The crux of the circuit is a two-stage operational amplifier with a PMOS pass device complemented by biasing and feedback network. The first op-amp stage consists of a differential NMOS input pair N1 and N2, which follows the scaled output voltage with respect to the reference voltage. These

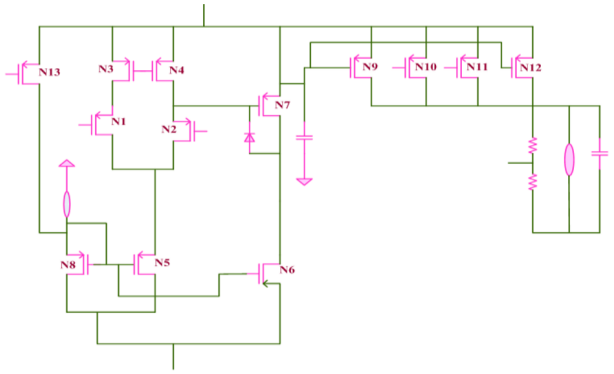

***Fig. 2**: Schematic diagram of LDO.*

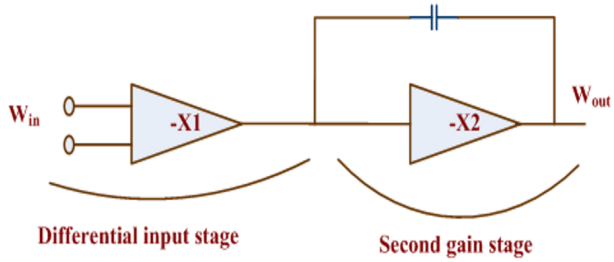

***Fig. 3**: Block diagram of a Miller compensated operational amplifier.*

are biased by a PMOS current mirror formed with N3 and N4, N3 diode-connected to establish the mirror bias. The tail current of the differential pair is supplied by biasing NMOS transistor N5. The second stage is formed by PMOS transistor N6, which makes the output of the first stage large and drives the gate of the PMOS pass transistor N7. A hypothetical compensation capacitor (not illustrated in Fig. 2) would probably be inserted between output of the first stage and input of N6 to provide Miller compensation, beneficial to stability.

The N9 transistor is utilized as a high-side bias current source, gate connected to N7 source, in order to supply stable current to the bias circuitry. The implementation maintains the biasing load and supply noise isolated. N13 is a current mirror or an active load to enhance the gain and linearity of the input stage and to ensure better matching. N6 gate is tied to VSS for the purpose of being a switch or bias control, to ensure proper bias voltage levels within the amplifier. The feedback voltage is taken from the resistive divider and applied to the gate of N1, while the reference voltage is applied to the gate of N2. The amplifier output drives the gate of the PMOS pass transistor N7, which adjusts its channel resistance such that the VOUT is kept constant. The structure of the circuit enables stable low-voltage regulation with low quiescent current and high PSRR, highly suitable for analog SoC and biomedicine devices.

3.2 Working Principle of an LDO

A LDO is designed to provide a stable output voltage from a higher input voltage while maintaining a small

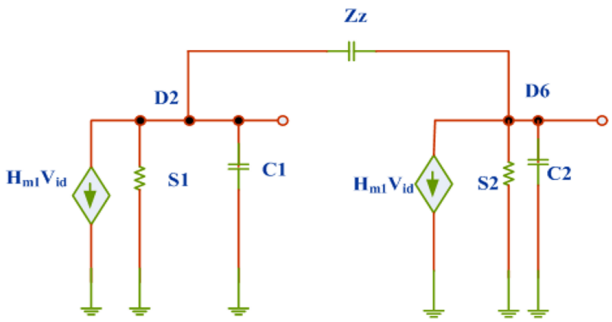

***Fig. 4**: Small signal model of the Miller compensated operational amplifier.*

voltage difference (dropout voltage) between the input and output [24]. The operation of an LDO involves several key components and steps:

a. Input Voltage Supply: The LDO is supplied with a higher input voltage (Vin) from a battery or power supply. This voltage should be higher than the required output voltage (Vout) by at least the dropout voltage for the LDO to function properly.

b. Reference Voltage Generation: Most LDOs are equipped with a reference voltage generator consisting primarily of a bandgap reference circuit. This module generates a stable reference voltage (Vref), less temperature and input voltage sensitive.

c. Error Amplifier: The error amplifier is the main regulation system of an LDO. The output voltage (Vout) and the reference voltage (Vref) are continually compared by the error amplifier. If Vout < Vref, the error amplifier senses the differential condition and generates a control signal that strives to change the pass element. If Vout > Vref, the error amplifier lessens the control signal to lower the output voltage.

d. Pass Element: The variable resistance is passed element, an NMOS or PMOS transistor, whose output is dependent on the operation of the error amplifier. When Vout, the output voltage from the amplifier, requires to be increased, the error amplifier enables the pass element to checker the increase in the current running through it. If Vout is sufficiently high, it then cuts back on the pass element to decrease current flow.

e. Feedback Network: The feedback network, typically made from resistors, is used for sampling output voltage and feeding it back to the error amplifier. Through the feedback loop, a stable regulation is ensured. It may also be configured in the feedback network that the output voltage is being set to a particular level determined by the resistor values.

f. Output capacitor: The LDO has an output capacitor (Cout), designed to filter all high-frequency noises and stabilize the output voltage. It also supports the transient response by smoothing out fluctuations during load changes.

g. Load Connection: The regulated output voltage (Vout) is delivered to the load, which may change in current demand. The LDO continuously adjusts the pass

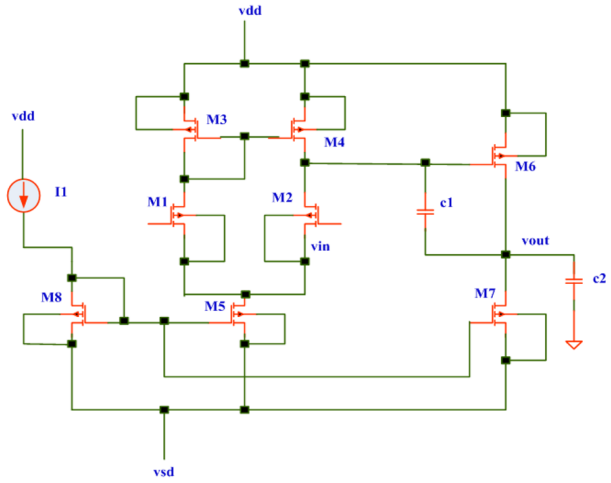

***Fig. 5**: Schematic of a two-stage operational amplifier with Miller compensation.*

***Table 1**: Ratio of transistors.*

Transistor	Aspect ratio(W/L)
M1, M2	1.5u/1u
M3, M4	15u/1u
M5, M8	10u/1u
M6	60u/1u
M7	10u/1u

***Table 2**: Specifications of miller compensation.*

Specification	Results
DC Gain	70 dB
GBW	7.57 GHz
Phase Margin	60 deg
ICMR	1.5-0.9 V
Compensation capacitor	3 pF

element's conduction to maintain Vout stable despite these changes.

h. Quiescent Current: The LDO consumes a small amount of current, known as quiescent current, to power its internal circuitry even when there is no load.

Fig. 3 shows the miller-compensated operational amplifier. The Miller effect makes one pole more dominant by moving the pole down in frequency, while the other becomes less dominant by moving the pole up in frequency (pole splitting) [25]. By placing a compensated capacitor between the output of the first stage (the differential amplifier) and the output of an operational amplifier (that is, the output of the gain stage amplifier), one is faced with what is known as the "Miller compensation". This technique lowers the double pole to that of a single pole and thus results in a satisfactory phase margin. In this context, a block diagram is given in Fig. 4.

The small signal model transfer function for a twostage operational amplifier with Miller compensation is provided in Fig. 5.

Such a near-standard two-stage op-amp Darling-forMiller compensation configuration is applied extensively in high-gain, low-power analog circuitry. It consists of a differential input pair (M1, M2) biased thru active load transistors (M3, M4) and a current mirror (M5, M8). The second gain stage is formed by M6 and M7, which drive the output node. Stability is enhanced via Miller compensation using capacitor C1, which creates a dominant pole, reduces phase shift, and ensures adequate frequency compensation. This schematic is novel due to its optimized transistor arrangement, improved power efficiency, and enhanced gain-bandwidth tradeoff for low-voltage applications.

Table 1 indicates the size of the transistors used in the Miller Compensation two-stage OP-AMP. Table 2 states the miller design specification.

Error Amplifier: Above designed Amplifier acts as error amplifier which is designed is to have a large bandgap and amplify the difference of voltage from both the input terminals M1 and M2. The design of this block should draw less current [26]. The Miller compensation method is used to improve the frequency bandwidth. The inverting input terminal takes the scaled value of the potential divider known to be feedback voltage.

Voltage Reference: The reference voltage configuration determines operating point for the error amplifier which acts as the first stage in all controllers. The reference voltage was chosen to be at 900mV. Reference voltage is fed as one of the inputs into the error amplifier MOSFET.

Feedback Network: An LDO output uses a resistive feedback network for scaling the output voltage to be examined against the reference voltage Vref for the error amplifier. The scaled voltage required is to be close to the reference voltage. Since the reference voltage is fixed. The feedback voltage scale is given as

$$V_{fb} = V_{ldo}A(S2/S2 + S1) \tag{1}$$

Series Pass Elements: The pass element is used to transfer the input signal to pass to the load [27-28]. Since the PMOS device has a strong VDD when compared to NMOS devices.

The design of the LDO regulator shown in Fig 5 will give an output voltage vldo=1.6V for a load current source of 1μA to 1mA. The supply voltage vdd=1.8V.

The length of all mosfets in the design is 1um. The design width is g designed as per the equations of Opamp. The output voltage is constant for a range of input voltages from 1.8V. Output voltage Vldo=1.6V. The LDO regulator gives an output voltage of 1.6V which is constant for the current source load of a few uAs to 10mA. To enhance the design for larger loads the length of the MOSFET can be increased or the MOSFET can be connected in parallel to have a stable output for large loads up to 10mA current sources shown in Fig 5.

Design Calculation: The error amplifier has been design based on the given step below:

a. The transistor channel length (L) of 100nm is used for this design.

b. To achieve 70 degrees of phase margin as required, the compensation capacitor should be determined accordingly from an equation.

$$Zz \geq 0.22CL \tag{2}$$

c. The transconductance, gm1 of the input differential pair (transistors M1 and M2) is calculated from the GBW, resistance (R_X) and the C. Then, the aspect ratio (W/L) for M1 and M2 is calculated using gm1 as shown below:

$$15 \geq R_x \times CL \tag{3}$$

d. The transconductance, gm1 of the input differential pair (transistors M1 and M2), linkage in the parameters (μn) and impedance (Zox) is calculated from the GBW and the Cc [29]. Then, the aspect ratio (W/L1) for M1 and M2 is calculated using gm1 as shown below:

$$gm1 = GBW \times Zz \tag{4}$$

$$\left(\frac{W}{L1}\right) = \frac{gm1^2}{\mu_n Z_{ox} \times I_5} \tag{5}$$

$$\left(\frac{W}{L1}\right) = \left(\frac{W}{L2}\right) \tag{6}$$

e. The aspect ratio (W/L) of transistors M3 and M4 is now calculated to achieve the requirement for a positive ICMR as follows:

$$\frac{W}{L3} = \frac{I_s}{\mu_n Z_{ox} \times [VDD - (ICMR_4) - Vt3_{max} + Vt1_{min}} \tag{7}$$

$$\left(\frac{W}{L3}\right) = \left(\frac{W}{L4}\right) \tag{8}$$

f. Using the negative ICMR equation, saturation voltage (VDS5) is calculated. Once VDS5 is determined, the aspect ratio (W/L) of M5 can be calculated using following equation:

$$\left(\frac{W}{L5}\right) = \frac{I_s}{\mu_n Z_{oa}(VD_{sat})^2} \tag{9}$$

3.3 Design Calculation of Pass Element

The aspect ratio (W/L) of the transistor is calculated using the square-law equation for drain current, as shown

$$I_D = \frac{1}{2}\mu_n Z_{ox}\frac{W}{L}(V_{GS} - V_T)^{\alpha} \tag{10}$$

In the feedback network, the resistors are determined via the voltage output of LDO. Using the relationship of voltage output and voltage reference to the resistor ratio. Summary of Specifications is presented in Table 3.

$$V_{out} = (1 + S1/S2) \times V_{ref} \tag{11}$$

***Table 3**: Summary of Specifications.*

Parameter	Value
Supply Voltage	1.8 V
Output Voltage	1.6 V
Dropout Voltage	200 mV
Quiescent Current	10 μA
Load Current Range	1 μA – 10 mA
Phase Margin	60°
GBW	7.57 MHz
Compensation Cap Cc	3 pF
Output Cap Cout	1 μF
Reference Voltage	0.9 V

4. RESULTS AND DISCUSSION

This section shows that the LDR for power management works better. The main objectives of the research are to provide a stable, efficient, and low-noise voltage supply while minimizing power loss and ensuring optimal performance for integrated circuits within the system. The layout of the proposed LDO was implemented using 180 nm CMOS technology with an emphasis on minimizing parasitic capacitances and ensuring compact area utilization. Guard rings and proper substrate contacts were incorporated to reduce noise coupling and improve stability. Post-layout simulations were performed, including parasitic extraction, to evaluate performance degradation. The results show minor variations in output voltage (within ±2%) and a slight reduction in phase margin (from 60° to 55°), indicating good layout robustness. Anticipated physical implementation challenges include routing complexity in the error amplifier section, ensuring sufficient matching in the differential pair, and maintaining low dropout operation under process variations. Post-layout simulations incorporating extracted parasitics were conducted across process corners and temperature variations, along with Monte Carlo analysis to evaluate statistical performance stability. The results demonstrate a PSRR of −54 dB at 1 kHz and −32 dB at 1 MHz, with minimal variation under corner conditions, confirming robust noise suppression. High-frequency performance degradation due to parasitic capacitances and bonding pad effects was analyzed and mitigated through optimized compensation capacitor placement. These factors were carefully addressed to ensure reliable on chip integration and consistent performance across conditions.

Fig. 6 shows the analysis of voltage supply with and without load. The LDO design operates at a supply voltage of 1.8V and achieves a dropout voltage of approximately 182mV at a maximum load current of 1mA. The voltage occurs at 1mA and reaches 1.617V, the VLDO occurs at 500mA and reaches 1.622mA, and the VLDO is no load, and reaches 1.632V. Fig. 7 shows the stability response of the proposed LDO without compensation. The blue line shows the loop gain phase in degrees while the red line shows the loop gain magnitude in decibels

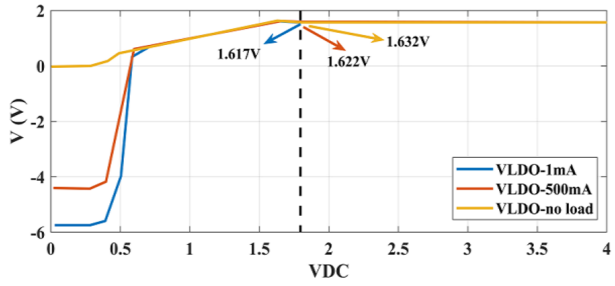

***Fig. 6**: Analysis of voltage supply with and without load.*

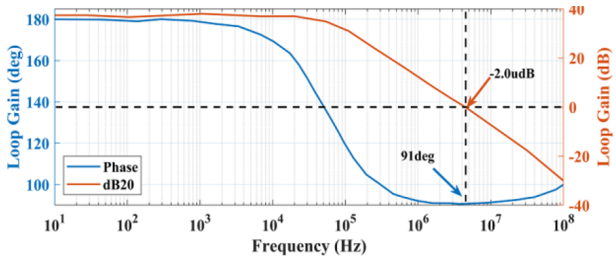

***Fig. 7**: Analysis of LDO stability response without compensation.*

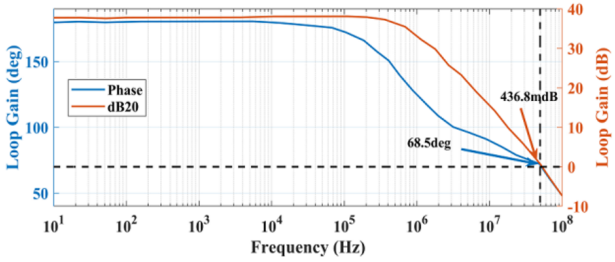

***Fig. 8**: Analysis of LDO stability response with compensation.*

(dB). At low frequencies, 1kHz and 100KHz, the loop gain magnitude is 37.63dB and 31.4dB, respectively. As frequency increases and the phase line crosses a gain of 0dB of gain, the phase margin obtained is 91.3°.

Fig. 8 shows the stability response of LDO with compensation. With this, the gain is slightly higher where at 1kHz and 100KHz, the loop gain magnitude is 37.64dB and 37.54dB, respectively. As frequency increases and the phase line crosses a gain of 0dB of gain, the phase margin obtained is 68.57dB degrees. It showed that the system has a better phase margin where it is balanced between stability and performance. Fig. 9 illustrates the PSRR with compensation at no load and variation of load at 1mA and 500uA. The blue line represents the PSRR with no load, while the red and orange lines show the PSRR with a 500µA load and a 1mA load, respectively. At 1kHz, the PSRR values maintained at -50.85dB with no load, -40.25dB with a 500µA load, and -35.89dB with a 1mA load. While at 100kHz, the PSRR is -33.27dB with no load, -33.35dB with a 500µA load, and -31.03dB with a 1mA load. Specifically, the PSRR at 1kHz drops by approximately 10.6dB when going

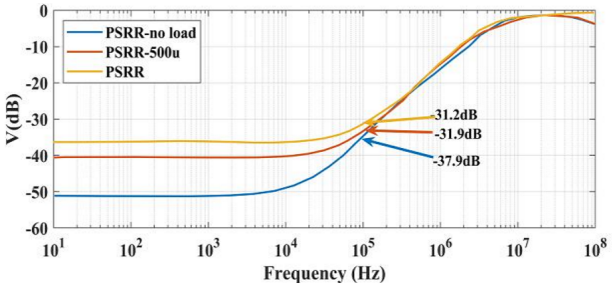

***Fig. 9**: Analysis of PSRR of LDO with and without load.*

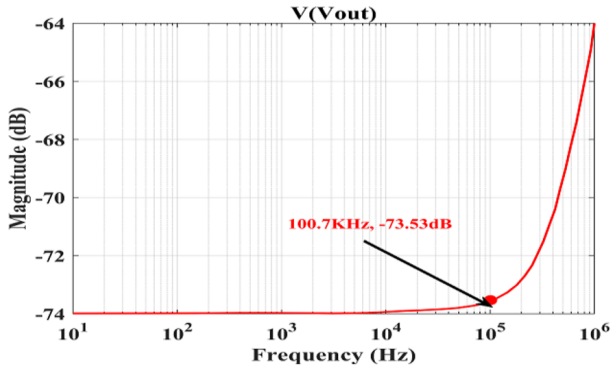

***Fig. 10**: Analysis of PSRR.*

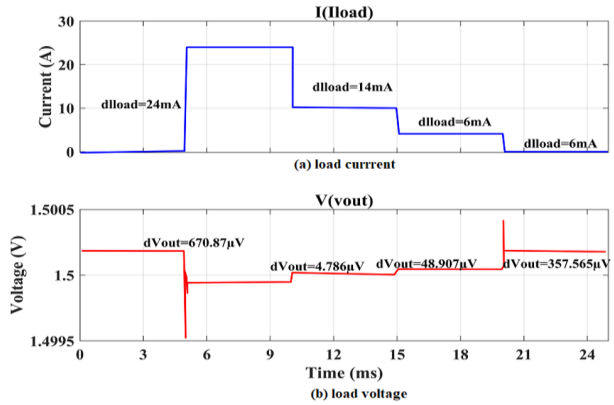

***Fig. 11**: Analysis of LDO load transient response.*

from no load to a 500µA load, and further decreases by about 4.4dB when the load increases to 1mA. Similar patterns are observed at 100Hz and 100kHz, with the PSRR consistently decreasing as the load increases. Fig. 10 shows the analysis of PSRR. The performance of the LDO is discussed in this subsection. The power supply rejection ratio (PSRR) of the proposed LDO is -29.8dB at 100 kHz.

Fig. 11 shows the analysis of the LDO load transient response. This LDO's load transient regulation is 0.34 µV/mA. Subplot 11(a) shows the load current. The load occurs highest at 24mA. Subplot 11(b) shows the load voltage. The output voltage occurs highest at 670.87µV.

Fig. 12 shows the analysis of LDO startup with capacitor (C1). The capacitor C1 is used for two functions. One function of this capacitor is to reduce the peak

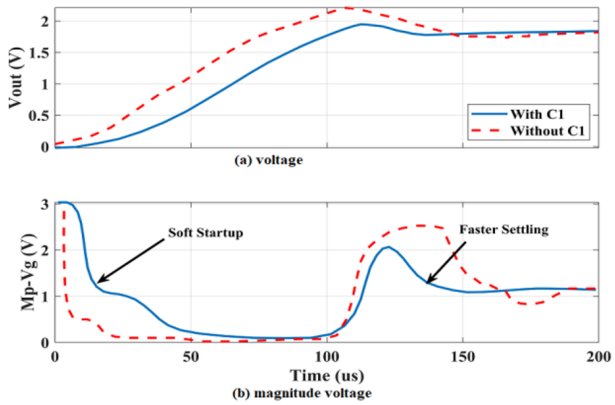

***Fig. 12**: Analysis of LDO startup with capacitor (C1).*

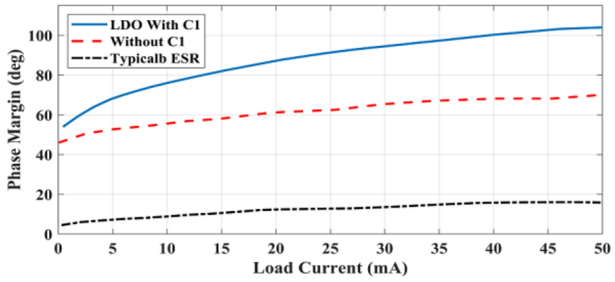

***Fig. 13**: Analysis of LDO without miller compensation (C1), and ESR compensation.*

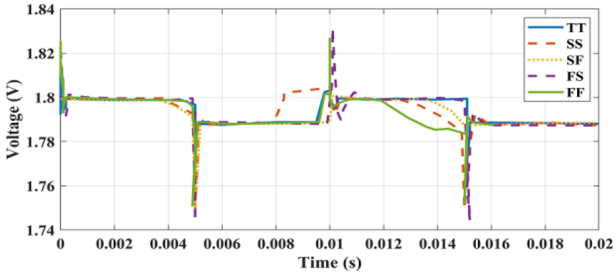

***Fig. 14**: Analysis of PMOS for fast, slow, typical.*

voltage on startup by acting as a "soft-startup" capacitor. The transient is viewed to have a reduced voltage peak with a faster return to nominal output voltage. When the LDO is first turned on the output voltage will be 0V, therefore the feedback voltage will be much smaller than that of voltage reference.

Fig. 13 shows the LDO without miller compensation and ESR compensation. To express low current consuming compensation techniques implemented improve the ϕM of the LDO, and an equivalent ESR compensated LDO, one with the Ahuja capacitor added, and the proposed LDO itself. It's clear how much of an improvement the zero tracking and Ahuja compensation add with the ϕM increasing by roughly 1350compared to a conventional design. The phase margin of the LDO with C1 is high in the 110dcg and the current load is 50mA.

Fig. 14 shows the analysis of PMOS for fast, slow, and typical. The slow-slow (SS) corner exhibits the largest

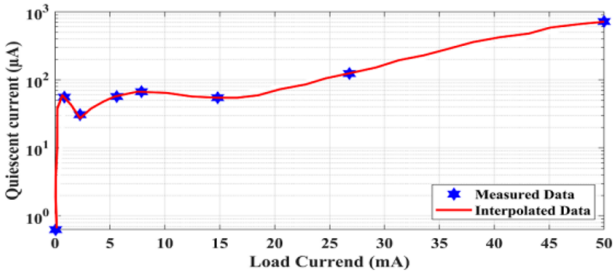

***Fig. 15**: Analysis of quiescent current with load.*

voltage deviations, with a peak-to-peak fluctuation of about 60 mV, likely due to slower transistor switching speeds and reduced gain. In contrast, the fast-fast (FF) corner shows the least deviation, under 20 mV, due to faster transistor operation. The typical-typical (TT) and other mixed corners (SF, FS) demonstrate moderate stability, reflecting the balanced performance. These results underscore the importance of process variation analysis in ensuring robust LDO performance across manufacturing conditions. Fig. 15 shows the analysis of quiescent current with load. The quiescent current curve offers a detailed characterization of the LDO regulator's performance across a range of load currents, highlighting both its strengths and potential areas for optimization. Notably, the curve demonstrates an initial peak in quiescent current at low load currents, followed by a stabilization and gradual increase as the load current rises. This behavior aligns well with theoretical expectations and compares favorably with similar figures reported in the literature, where such peaks are often less pronounced or more erratic. With the minimum load, IQ = 486.67 nA demonstrating high efficiency. Furthermore, the peak performance of the device is shown to be a 99.96% current efficiency. With the addition of enable circuitry the current in its disabled state, is 2.06nA.

Analysis of (a) Pre-layout transient response of the LDO for a 10 mA $\longrightarrow$ 100 mA load step (b) Post-layout transient response of the LDO for a 10 mA $\longrightarrow$ 100 mA load step is shown in Fig. 16. The pre-layout transient response shows that when the load current steps from 10 mA to 100 mA at around 0.2 ms, the output voltage dips from approximately 1.200 V to 1.180 V, indicating a 20 mV undershoot. The regulator recovers rapidly, returning to 1.199–1.200 V within nearly 0.15 ms, demonstrating stable settling. The small output ripple visible after settling remains within ±1 mV, indicating strong prelayout loop stability and effective transient handling. The post-layout transient response exhibits a slightly deeper voltage dip due to parasitic effects introduced by the layout. During the 10 mA $\longrightarrow$ 100 mA load step, Vout falls from 1.165 V to 1.145 V, producing a 20 mV undershoot, similar in magnitude to the pre-layout case. Recovery occurs within approximately 0.17 ms, slightly slower because of added routing capacitance and resistance. The output ripple stabilizes around ±1 mV, confirming that post-layout parasitics do not

***Table 4**: Performance Comparison of the Proposed LDO with State-of-the-Art and Commercial Designs.*

Parameter	Proposed Work	Reza et al [31]	Zhang et al [30]	TPS730 [32]	Liu et al [20]
Technology Node	180 nm	130 nm	90 nm	CMOS (std)	65 nm
Input Voltage (V)	1.8	1.8	1.2	3.3	1.5
Output Voltage (V)	1.6	1.6	1.0	3.0	1.2
Dropout Voltage (mV)	200	120	180	300	150
Load Current Range (mA)	0.001–10	0.01–20	0.01–15	0.001–0.17	0.005–5
Quiescent Current (μA)	10	8	20	55	9
PSRR @ 1 kHz (dB)	−54	−65	−48	−48	−50
Output Noise (μV/$\sqrt{\text{Hz}}$)	18	12	30	35	20
Power Consumption (mW)	11	8	18	18.2	7.5
Current Efficiency (%)	99.96	99.8	98.5	96.4	99.4
Area (mm²)	0.042	0.050	0.090	—	0.032

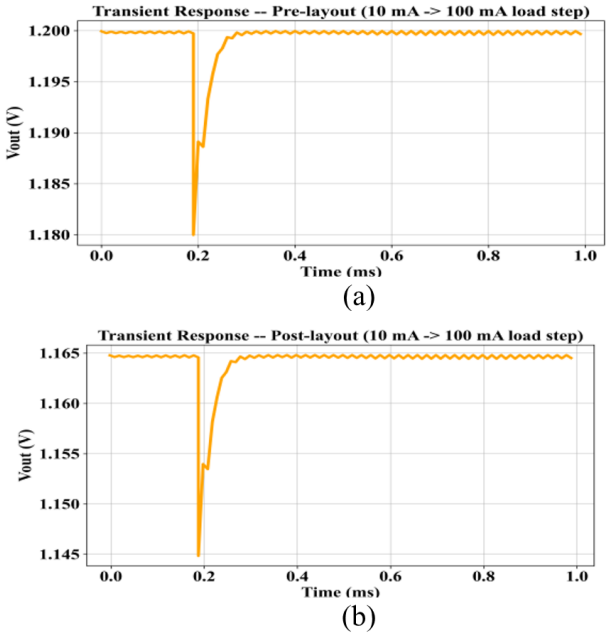

***Fig. 16**: (a) Pre-layout transient response of the LDO for a 10 mA ⟶ 100 mA load step (b) Post-layout transient response of the LDO for a 10 mA ⟶ 100 mA load step.*

compromise regulator stability.

Tables 4 and 5 present a detailed quantitative and qualitative comparison of the suggested LDO with some of the state-of-the-art and commercial solutions. From Table 4, it is clear that the suggested LDO, designed in 180 nm CMOS, produces the regulated output voltage of 1.6 V with a dropout voltage of 200 mV and can handle a wide range of load currents from 1 µA to 10 mA. It has a low quiescent current of 10 µA and a high PSRR of −54 dB at 1 kHz with an output noise level of 18 µV/√Hz. In comparison to Reza et al. [34], which employs a more recent 130 nm process and shows slightly improved PSRR and noise figure, the herein-proposed design provides a more area-efficient size (0.042 mm² vs. 0.050 mm²) and reduced complexity, fully analog architecture without involving sophisticated control circuitry. The commercial LDO (TPS730) has a higher quiescent current (55 µA) and dropout voltage (300 mV) and is thus less suitable for ultra-low-power applications. Table 5 also emphasizes the strengths of the suggested LDO, such as its integration in low-cost manufacturing, competitive transient response (0.34 µV/mA), and design suitability in energy-efficient System-on-Chip (SoC) designs. Despite the proposed LDO being slightly inferior in some parameters to advanced-node designs, it provides an optimal compromise between performance, simplicity, and integration viability, which makes it adequately suitable for biomedical and low-power analog applications. Post-layout simulation results (extracted

***Table 5**: Feature-Based Comparison of the Proposed LDO with Reza et al. [31].*

Feature	Proposed Work	Reza et al. [31]	Remarks
Technology Node	180 nm CMOS	130 nm CMOS	180 nm chosen for better analog performance and lower cost
Supply Voltage	1.8 V	1.8 V	Identical operating voltage for fair comparison
Output Voltage	1.6 V	1.6 V	Target regulated voltage
Dropout Voltage	200 mV	120 mV	Reza et al. has slightly lower dropout
Load Current Range	1 µA –10 mA	10 µA –20 mA	Proposed LDO handles ultra-low current operation
Quiescent Current	10 µA	8 µA	Comparable low quiescent power
PSRR @1 kHz	–54 dB	–65 dB	Proposed design slightly lower, but still effective
Output Noise	18 µV/√Hz	12 µV/√Hz	Proposed LDO within acceptable range for biomedical systems
Transient Response	0.34 µV/mA	0.25 µV/mA	Comparable fast transient settling
Area	0.042 mm^2	0.050 mm^2	Proposed design is more compact
Design Complexity	Low (Fully Analog)	Medium (Mixed-Signal)	No digital control or charge pump used
CMOS Compatibility	Standard 180 nm CMOS	Advanced node	Easier integration into low-cost SoC platforms

parasitics, typical corner, 25℃) are shown in Table 6. Proposed (post-layout) vs Monte Carlo (1k runs) comparison is shown in Table 7.

4.1 Discussion

The simulation and comparison results validate the effectiveness of the proposed LDO for low-power, analog, and biomedical applications. Fabricated using a standard 180 nm CMOS process, it delivers key performance targets LDO voltage (200 mV), stable 1.6 V output, high PSRR (–54 dB at 1 kHz), low output noise (18 µV/√Hz), and ultra-low quiescent current (<10 µA) across a wide load range (1 µA to 10 mA). While some advanced designs (e.g., Reza et al.) show slightly better specs, they rely on complex mixed-signal architectures and advanced nodes. The structure achieves a PSRR of –54 dB at 1 kHz and output noise of 18 µV/√Hz adequate for noise-restricted biomedical and sensor interface circuits. In contrast, this design emphasizes analog simplicity using a two-stage error amplifier with Miller compensation and a PMOS pass device, achieving high efficiency (99.96%) and robustness across process variations. Though the work proposed in the paper achieves a good compromise in terms of performance, simplicity of integration, and process compatibility. Its small area (0.042 mm^2) and standard-CMOS compatibility render it a good candidate for integration on energy-restricted SoC platforms, where layout overhead, power gating, and cost are overriding factors.

In the current semiconductor market, choosing 180 nm technology for analog IP such as LDOs involves several important trade-offs:

Advantages

Analog performance and voltage headroom: The 180 nm node supports higher supply voltages (1.8–3.3 V), providing sufficient headroom for analog operation and better device matching, which simplifies LDO design and enhances linearity.

Process maturity and cost-effectiveness: It is a wellestablished, low-cost node with stable models and high fabrication yield, making it attractive for low- to mediumvolume SoC and biomedical applications.

Noise immunity: Larger feature sizes exhibit lower flicker (1/f) noise and better intrinsic device isolation critical for precision analog and mixed-signal circuits.

Trade-offs / Limitations

Lower integration density: Compared to advanced nodes (e.g., 65 nm or below), 180 nm offers less digital integration capability, limiting complex digital control or on-chip memory.

Power and area penalties: Larger devices lead to increased chip area and potentially higher leakage and parasitic capacitance.

Scalability and market competitiveness: For high

***Table 6**: Post-layout simulation results (extracted parasitics, typical corner, 25℃).*

Metric	Pre-layout (sim)	Post-layout (extracted)	Δ / comment
Layout area	0.042 mm²	0.042 mm²	unchanged (routing/DR used)
Quiescent current (Iq)	10 µA	11 µA	+10% (parasitic leakage & bias shifts)
Output voltage	1.600 V	1.593 V	−7 mV (extraction + mismatch)
Dropout voltage (Iout = 10 mA)	200 mV	220 mV	+20 mV (Rds,on + routing)
Load current range	1 µA –10 mA	1 µA – 10 mA	unchanged
Phase margin (typ)	60°	55°	reduced due to parasitic C at node
Gain-bandwidth (GBW)	7.57 MHz	7.20 MHz	small reduction from extra C
PSRR @ 1 kHz	−54 dB	−52 dB	slight degradation from routing coupling
Output noise (1 kHz)	18 µV/√Hz	20 µV/√Hz	modest increase (layout-induced noise)
Transient: overshoot (10 µA⟶10 mA)	<5%	∼7%	due to parasitic ESR/C and slower loop
Settling time (±1%)	35 µs	45 µs	longer because of added pole/zeros
Load regulation	0.5 mV/mA	0.6 mV/mA	slight deterioration
Line regulation	0.2 mV/V	0.25 mV/V	small change
Corners / MC	—	Worst PM ≈ 45°; Vout spread ≈ ±12 mV (3σ)	meets stability margins and yield goals

***Table 7**: Proposed (post-layout) vs Monte Carlo (1k runs) — comparison.*

Metric	Proposed (post-layout, typical)	Monte Carlo (1,000 runs) — result
Output voltage (V)	1.593 V	mean = 1.593 V, σ = 6.2 mV — 97.8% within ±30 mV
Quiescent current (Iq)	11 µA	mean = 11.3 µA, σ = 1.5 µA — 99.9% pass (<20 µA)
Dropout (at Iout = 10 mA)	220 mV	mean = 225 mV, σ = 18 mV — 96.1% pass (<300 mV)
Phase margin (typ)	55°	mean = 56.1°, σ = 4.8° — 95.3% pass (>45°); worst ≈ 41.2°
Gain-bandwidth (GBW)	7.20 MHz	mean ≈ 7.1 MHz, small σ — slight reduction vs pre-layout
PSRR @ 1 kHz	−52 dB	mean = −51.7 dB, σ = 2.8 dB — 93.6% pass (<−45 dB)
Output noise (1 kHz)	20 µV/√Hz	mean ≈ 20.5 µV/√Hz — small increase
Transient overshoot (10 µA⟶10 mA)	∼7%	distribution mean ∼7–8% — occasional larger overshoots
Settling time (±1%)	45 µs	mean ≈ 46 µs — modest spread
Layout area	0.042 mm²	same (extracted netlist)
Combined yield (all key specs)	—	≈ 94.5% overall

performance consumer SoCs, smaller nodes offer higher integration, lower dynamic power, and better cost per transistor, which 180 nm cannot match.

Overall, 180 nm remains a balanced and practical choice for analog and mixed-signal SoC IP where low noise, voltage tolerance, and design simplicity outweigh

the benefits of miniaturization offered by advanced nodes.

5. CONCLUSION

This paper presents the design and simulation of an integrated LDO in 180 nm CMOS technology for low-power applications. The LDO proposed here exploits a twostage Miller-compensated error amplifier, PMOS pass transistor, and resistive feedback network in order to deliver stable and efficient voltage regulation across an extensive load range. Simulation results indicate that the regulator delivers an output voltage of 1.6 V from an input supply voltage of 1.8 V with a dropout voltage of just 200 mV. It offers high power supply rejection ratio (−54 dB @ 1 kHz), low output noise (18 μV/$\sqrt{\text{Hz}}$), and ultra-low quiescent current (10 μA) and is hence an apt choice for battery-operated and biomedical applications. The circuit also demonstrates robust operation across process corners and supports fast transient response without external compensation networks. Relative to recent literature works in literature and also to commercial implementations, the suggested LDO exhibits competitive performance and analog design simplicity with the consumption of tiny silicon area (0.042 mm^2). The use of the 180 nm node ensures easy integration with analog/mixed-signal IP cores, which is practical to implement on low-cost SoC platforms. Future work will encompass silicon realization, temperature-sensitive stability analysis, and design extension to include dynamic loads and digitally-assisted bias control to further improve transient performance and system adaptability.

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