

Low-Latency Dual-MCU Hardware-in-the-Loop Platform Using Analog-Domain Communication for Electric Drive Applications

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ABSTRACT

Real-time validation of electric-vehicle (EV) motor-drive controllers is limited by the cost and latency of current hardware-in-the-loop (HIL) systems. This paper proposes a low-cost dual-microcontroller HIL platform that enables deterministic, low-latency testing with off-the-shelf components. Two Texas Instruments TMS320F28379D digital signal controllers partition the control and plant domains: one runs cascaded PI speed and current regulators, and the other numerically simulates the DC-motor-chopper-vehicle dynamics with a 10 μ s step size. A key feature is analog-domain signal exchange: the controller's PWM duty is low-pass filtered and sampled by the plant MCU, while armature current and speed feedback return via DAC-ADC links. This removes SPI/serial protocol overhead and delivers a measured 4.21 μ s round-trip latency, ensuring deterministic real-time coupling. Experiments with step and mixed drive-cycle profiles show tracking comparable to a single-MCU benchmark, with lower current ripple and improved modularity. The workflow uses Simulink auto-code generation with no manual driver coding. The platform thus offers a cost-effective, transparent, and reproducible framework for EV drive-control research and education, demonstrating that analog-coupled dual-MCU architectures can achieve sub-10 μ s responsiveness and structural realism for next-generation EV HIL development.

Keywords: Hardware-in-the-Loop (HIL), Dual-MCU Architecture, Analog-Domain Communication, Real-Time Embedded Control, Electric Drive Systems, Motor-Drive Validation

1. INTRODUCTION

The rapid expansion of electric-vehicle (EV) technology has created an urgent need for reliable and repeatable validation of motor-drive control systems. Direct testing

on physical prototypes is costly and may endanger equipment during transient or fault conditions, motivating the widespread use of hardware-in-the-loop (HIL) simulation for controller verification [1]-[4]. HIL simulation enables a real embedded controller to interact in real time with a numerically simulated plant, allowing control algorithms to be tested under realistic operating conditions while maintaining a safe laboratory environment [5]-[7]. This approach is particularly valuable in motor-drive and power-electronics systems where control loops operate at high sampling rates and timing determinism strongly influences closed-loop performance [8]. HIL environments allow the embedded controller to operate with a numerically emulated plant in real time, bridging the gap between software simulation and field testing.

Commercial HIL systems—such as dSPACE, OPAL-RT, and Typhoon HIL offer high fidelity but remain prohibitively expensive for many research and educational laboratories [9]. However, these platforms often require specialized hardware and proprietary software frameworks, resulting in high acquisition costs that limit accessibility for many research and educational laboratories. To reduce cost, several studies have investigated microcontroller-based HIL platforms [10]-[14]. Most of these rely on digital communication protocols such as SPI, UART, or CAN to exchange data between control and plant processors. While convenient, these interfaces introduce non-deterministic latency and protocol overhead that limit achievable update rates, especially when the control period falls below 100 μ s.

To overcome these constraints, this paper introduces a dual-microcontroller HIL architecture that employs analog-domain signal exchange instead of packet-based communication. Two Texas Instruments TMS320F28379D digital-signal controllers are used: one executes cascaded PI-based speed and current regulators, and the other performs real-time simulation of the DC-motor-chopper-vehicle dynamics. The controller transmits its duty-ratio command via a filtered PWM signal that reconstructs an analog control voltage, while the plant MCU returns feedback through DAC-ADC links representing measured current and speed signals. By avoiding packet-based communication protocols, the proposed architecture minimizes communication overhead and enables deterministic real-time interaction between the controller and the simulated plant.

The resulting system achieves sub-10 μ s round-trip latency without protocol overhead, closely replicating

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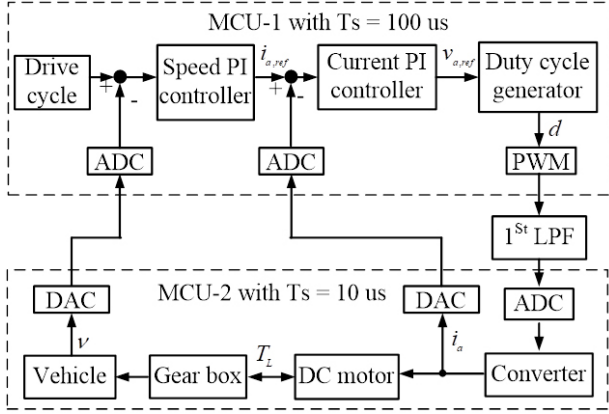


Fig. 1: Dual-MCU HIL Architecture. MCU-1 Runs Cascaded PI Control at $T_s = 100\mu s$; MCU-2 Simulates the Plant at $T_s = 10\mu s$. Analog PWM-LPF and DAC-ADC Links Enable Sub-10- μs Closed-Loop Latency without Protocol Overhead.

the analog signal interface typically present between a controller and a physical motor drive plant.

The main contributions of this work are as follows:

1. Development of a low-latency dual-MCU HIL platform using analog-domain coupling.
2. Quantitative characterization of communication latency, jitter, and control performance.
3. Demonstration of a reproducible, Simulink-based workflow suitable for education and research in electric-drive systems.

These contributions establish a practical and scalable framework for low-cost, high-fidelity HIL experimentation in embedded motor-drive control.

2. SYSTEM ARCHITECTURE AND METHODOLOGY

The proposed hardware-in-the-loop (HIL) platform partitions computation across two Texas Instruments TMS320F28379D digital-signal controllers (200 MHz, dual cores, 12-bit ADC/DAC). This dual-MCU arrangement emulates the natural separation between a vehicle's control ECU and its powertrain hardware, as illustrated in Fig.1.

The control-plant interaction workflow of the proposed dual-MCU HIL system is illustrated in Fig.2. MCU-1 executes the embedded control algorithm and generates a PWM duty-ratio command. The PWM signal is converted into an analog control voltage using a low-pass filter. This signal is then sampled by MCU-2 through its ADC interface. MCU-2 computes the plant dynamics of the motor-drive model and outputs simulated feedback signals via DAC channels. These signals represent the measured current and speed and are sampled by the ADC of MCU-1 to close the control loop.

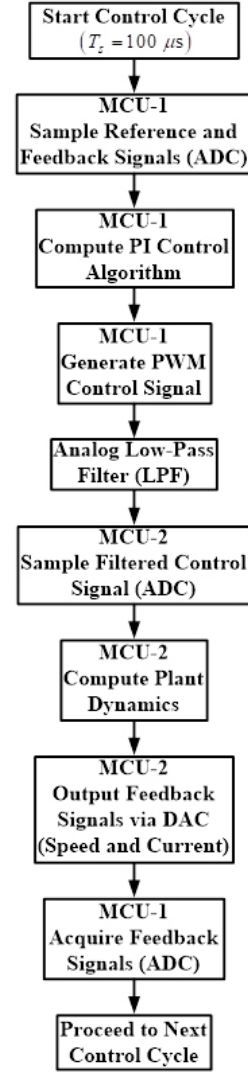


Fig. 2: Control-Plant Interaction Workflow of the Proposed Dual-MCU HIL Architecture.

2.1 Controller (MCU-1)

MCU-1 executes cascaded PI controllers for speed and current regulation. The outer loop computes the armature-current reference $i_{a,ref}$ from the speed error, and the inner loop determines the duty ratio d from the current error using the incremental PI form:

$$i_{a,ref}[k] = i_{a,ref}[k-1] + K_{ps}[e_v[k] - e_v[k-1]] + K_{is}T_s e_v[k] \quad (1)$$

$$d[k] = d[k-1] + K_{pc}[e_i[k] - e_i[k-1]] + K_{ic}T_s e_i[k] \quad (2)$$

Control tasks are triggered every $T_s = 100\mu s$. Duty ratio d is output through the ePWM module and filtered by an external RC network to reconstruct an analog command voltage.

The proportional and integral gains for both speed and current PI controllers were tuned empirically to achieve fast response with negligible overshoot under nominal

Table 1: Controller Parameter (MCU-1).

Parameter	Value
K_{ps}	0.3142
K_{is}	13.823
K_{pc}	300.00
K_{ic}	6.00
T_s for MCU-1 control	100 μ s
T_s for speed control loop	1 ms
T_s for current control loop	100 μ s
Saturation $i_{a,ref}$ control	± 100 A

load. The complete set of controller parameters and sampling periods used in MCU-1 are summarized in Table 1.

2.2 Plant Simulation (MCU-2)

The plant-side microcontroller (MCU-2) numerically simulates the EV drivetrain, discretized for real-time integration with a fixed time step of $T_s = 10\mu s$. The model consists of a DC chopper, a separately excited DC motor, a gearbox, and the vehicle longitudinal dynamics.

The average voltage applied to the motor terminals is computed from the controller's duty ratio:

$$V_a[k] = d[k] \cdot V_{dc} \quad (3)$$

This voltage drives the electrical dynamics of the motor:

$$i_a[k] = i_a[k-1] + \frac{T_s}{L_a} \begin{pmatrix} V_a[k-1] - R_a i_a[k-1] \\ -k_e \omega[k-1] \end{pmatrix} \quad (4)$$

$$\omega[k] = \omega[k-1] + \frac{T_s}{J} \begin{pmatrix} k_t i_a[k-1] - B \omega[k-1] \\ -T_L[k-1] \end{pmatrix} \quad (5)$$

Motor torque is obtained as

$$T_m[k] = k_t \cdot i_a[k] \quad (6)$$

and the gearbox converts it into wheel torque through

$$T_{out}[k] = \eta_g \cdot GR \cdot T_m[k] \quad (7)$$

Vehicle longitudinal motion is integrated from the net tractive force:

$$v[k] = v[k-1] + \frac{T_s}{m} \left[\frac{T_{out}[k-1]}{r} - \begin{pmatrix} F_{rr} + F_d[k-1] \\ + F_{grade} \end{pmatrix} \right] \quad (8)$$

Resistive forces are modeled as $F_{rr} = C_{rr} \cdot m \cdot g$, $F_d[k] = \frac{1}{2} \rho \cdot C_d \cdot A_{front} \cdot v[k]^2$, $F_{grade} = m \cdot g \cdot \sin \theta$ (if road slope θ is included).

At the end of each simulation cycle, the plant feedback signals $i_a[k]$ and $v[k]$ are sent to MCU-1 through DAC channels (DACA and DACB) to maintain closed-loop operation with the controller executing at $T_s=100\mu s$. This model structure ensures that both electrical and mechanical vehicle dynamics are reproduced accurately in real time on the microcontroller platform.

The electrical, mechanical, and vehicle parameters used for the real-time plant simulation on MCU-2 are summarized in Table 2. These values correspond to a 48-V, 5-kW class DC drive representative of a small electric-vehicle drivetrain.

2.3 Analog-Domain Communication and Synchronization

The system employs fully analog coupling to avoid protocol latency. The PWM-to-LPF-to-ADC path provides continuous-time duty-ratio transfer, while DAC-to-ADC feedback ensures real-signal realism. Both MCUs are synchronized through hardware timers, guaranteeing deterministic updates. Oscilloscope verification confirmed that the analog path introduces less than 1 μ s additional delay and maintains full 0-3.3 V range fidelity.

Fig. 3 illustrates the analog communication interface between the controller processor (MCU-1) and the plant simulation processor (MCU-2). The duty-ratio command generated by the PWM module (EPWM1A) of MCU-1 is converted into an analog command signal using a first-order RC low-pass filter composed of a 2 k Ω resistor and a 0.1 μ F capacitor. The filtered voltage represents the command signal d , which is sampled by the ADC input of MCU-2. After computing the plant dynamics, MCU-2 outputs the simulated feedback variables through its DAC channels. These signals, including armature current I_a and vehicle speed v , are transmitted back to MCU-1 and sampled by its ADC inputs for closed-loop control.

2.4 Experimental Implementation

Two LaunchPad development kits are mounted on a custom backplane with shared ground and independent supplies. MATLAB/Simulink with the C2000 Support Package automatically generates C code, which is compiled in Code Composer Studio v10.1. No manual driver coding is required, ensuring reproducibility. Task execution times are measured via GPIO toggling and DAC markers, enabling accurate timing analysis of the control and plant tasks. This methodology provides a transparent workflow for replicating real-time embedded-drive behaviour and enables precise verification of task execution time and communication latency within the dual-MCU system.

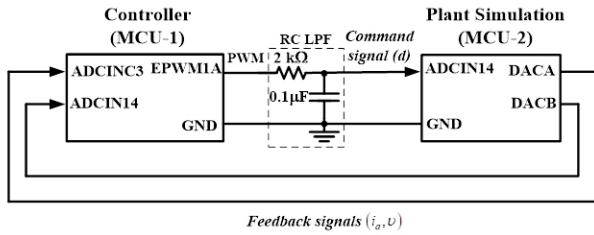
The detailed hardware configuration and communication setup used in the experimental platform are summarized in Table 3. These parameters define the real-time operating conditions of both MCUs, including control and simulation periods, analog interfaces, and signal-conditioning circuits that enable deterministic data exchange. The complete experimental setup, including the host computer, dual-MCU testbench, and oscilloscope interface, is shown in Fig. 4. Both MCUs are mounted on a shared baseboard with analog interconnections for PWM, LPF, DAC, and ADC channels. The photographs illustrate the overall configuration and detailed wiring used for latency and signal-verification tests.

Table 2: Plant and Vehicle Parameters Used in MCU-2 Simulation Model.

Converter		Base quantities	
Parameter	Value	Parameter	Value
V_{dc}	48 V	I_{base}	100 A
DC motor		V_{base}	48 V
Parameter	Value	v_{base}	40 km/h
R_a	0.01 Ω		
L_a	60 μ H	Vehicle	
		Parameter	Value
J	0.018 kg.m ²	η_g	0.95
B	6.25 x 10 ⁻³ Nms/rad	GR	1:10
k_e	0.0707 V/(rad/s)	r	0.25 m
k_t	0.0707 Nm/A	m	140 kg
I_{rated}	100 A	C_{rr}	0.011
V_{rated}	48 V	C_d	0.7
N_{rated}	6400 rpm	A_{front}	0.55 m ²
		ρ	1.225 kg.m ³
		g	9.81 m/s ²
		θ	0°

Table 3: Hardware and Communication Parameters.

Parameter	Value /Description
Microcontroller Units (MCUs)	2 x TI TMS320F28379D (200 MHz, 12-bit ADC/DAC, ePWM)
Control Loop Period T_s	100 μ s (MCU-1), 10 μ s (MCU-2)
PWM Output	ePWM module, 20 kHz, duty output to RC filter
RC Filter	$R = 2$ k Ω , $C = 0.1$ μ F (~ 800 Hz cutoff)
DAC Channels	DAC A for i_a , DAC B for v
ADC Channels	12-bit ADCs on both MCUs, synchronized sampling
Analog Voltage Ranges	0–3.3 V logic (DAC, ADC, PWM-compatible)
Signal Communication	Fully analog (PWM-RC, DAC-ADC), no SPI/UART
Code Generation Toolchain	MATLAB/Simulink with C2000 Support, CCS v10.1.0
Debug/Monitoring	MCU-1 DACs used for scope probing

**Fig. 3:** Analog-Domain Communication Interface Schematic between the Controller (MCU-1) and Plant Simulation (MCU-2) Using a PWM-RC Filter (2 k Ω , 0.1 μ F) for the Command Signal d and DAC-ADC Links for Feedback Signals (i_a , v).

3. IMPLEMENTATION AND EXPERIMENTAL SETUP

The control MCU (MCU-1) operates with a 100 μ s task period, while the plant MCU (MCU-2) executes at 10 μ s. Both are synchronized through hardware timer interrupts. PWM signals are generated at 20 kHz and filtered through an RC network ($R = 2$ k Ω , $C = 0.1$ μ F, ≈ 800 Hz cutoff) to create an analog control voltage. In the feedback path, MCU-2 outputs armature current and vehicle speed through DAC channels (DACA, DACB), which are sampled by MCU-1's ADC inputs.

All signals are within a 0–3.3 V analog range, ensuring full compatibility between DAC and ADC channels without additional signal conditioning. Oscilloscope measurements confirmed waveform integrity, low noise ($< 2\%$ of full scale), which is significantly below the control signal variation range, and consistent phase

alignment between transmitted and received signals.

The experiments include both step reference tests and a corner-mixed interpolated drive cycle with a maximum speed of 40 km/h. All key variables—speed, current, duty ratio, and latency markers—were logged for analysis. The main hardware and communication parameters are summarized in Table 3. The recorded data were exported in CSV format and post-processed in MATLAB to generate plots with clearly labeled axes and consistent scaling for analysis and presentation.

This setup ensures that results are fully reproducible using commercially available components and standard MATLAB/Simulink workflows, making the platform accessible for academic and research laboratories.

4. RESULTS AND ANALYSIS

4.1 Latency Characterization

A crucial indicator of real-time performance is the closed-loop delay between controller output and feedback acquisition. To characterize this latency, dual-channel oscilloscope instrumentation was used to simultaneously capture the rising edges of the controller's PWM duty output (at the DAC output of MCU-1) and the returned analog feedback (from the DAC output of MCU-2). Both signals represent the same duty-ratio command, enabling edge-aligned measurement.

The measured round-trip latency was 4.21 μ s (measured via oscilloscope histogram), encompassing PWM edge delay, RC-filter settling, DAC conversion, inter-MCU transport, plant model processing, and ADC sampling. This confirms that the analog signal path can sustain sub-10 μ s responsiveness, suitable for 100 μ s

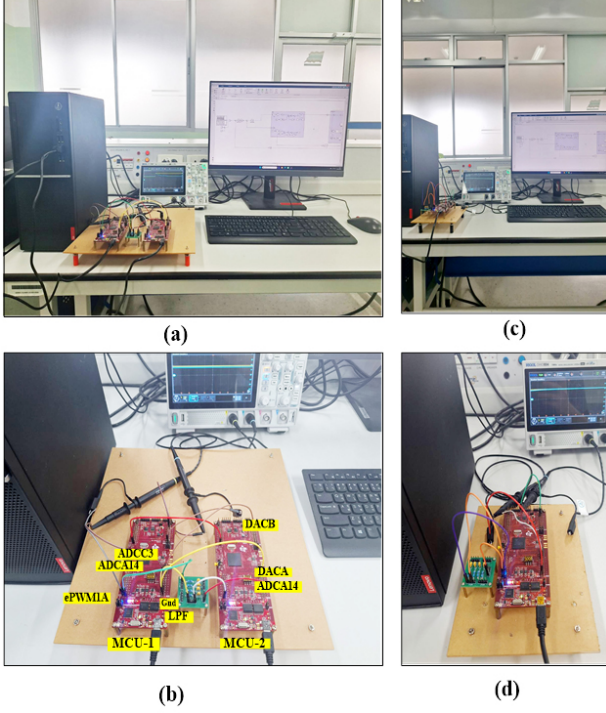


Fig. 4: Experimental HIL Testbench. (a) Dual-MCU Platform with Host PC and Oscilloscope; (b) Annotated Close-up of MCU-1 and MCU-2 with Analog Interconnects (ePWM1A, DACA/B, LPF, ADC Channels); (c) Single-MCU Test Configuration; (d) Close-up of Single-Board Setup.

control cycles and $10\mu\text{s}$ plant update intervals.

In contrast, SPI-based HIL platforms may exhibit $34\text{--}115\mu\text{s}$ round-trip latency at the system level [15], while raw SPI transfer latency is typically $10\text{--}30\mu\text{s}$ as shown in Table 8. The proposed analog-domain coupling achieves a $3\times\text{--}10\times$ faster and fully deterministic response, enabling high-speed real-time HIL loops without jitter or packet-processing delays. These results demonstrate that analog-domain signal exchange, when implemented carefully with proper filtering and sampling synchronization, can outperform digital protocols such as SPI or UART in latency-critical embedded HIL systems.

Fig. 5 shows the measurement configuration used to characterize the communication latency of the proposed HIL platform. GPIO marker signals are inserted in the MCU-1 control loop to indicate the instants when the command signal is issued and when the feedback signal is received. These markers are monitored using a two-channel oscilloscope, allowing the round-trip delay of the controller-plant interaction to be measured directly.

Fig. 6 shows the oscilloscope measurement of the round-trip communication latency of the proposed analog-coupled dual-MCU HIL platform. Channel 1 (blue) represents the GPIO marker indicating the command issuance event in MCU-1, while Channel 2 (red) indicates the marker corresponding to the feedback reception event after plant computation. The time difference between these two signals represents the

round-trip delay of the controller-plant interaction.

To statistically evaluate the timing performance, the oscilloscope histogram function was used to record delay measurements over 1000 samples. The results show an average latency of approximately $4.21\mu\text{s}$, with a standard deviation (jitter) of 68.9 ns , demonstrating deterministic low-latency communication suitable for high-speed control loops.

The statistical results of the measured round-trip latency are summarized in Table 4. The measurements were obtained using the oscilloscope delay-histogram function with 1000 samples. The results show an average communication latency of approximately $4.21\mu\text{s}$ with a standard deviation of 68.9 ns , demonstrating deterministic low-latency interaction between the controller and plant processors.

4.2 Closed-Loop Performance

Step-response experiments validated dynamic accuracy under three-level speed commands ($0.5\text{ p.u.} \rightarrow 1.0\text{ p.u.} \rightarrow 0.5\text{ p.u.}$). Both single- and dual-MCU configurations achieved negligible overshoot and $< 0.07\text{ V}$ steady-state error. The dual-MCU setup exhibited a slightly longer rise time (4.62 s vs 4.4 s) due to independent task scheduling but maintained identical speed-tracking RMSE (0.23 V). The current waveform showed a smoother profile with 6% lower RMS ripple, indicating improved damping from isolated computation domains.

The corresponding step-response waveforms for both single- and dual-MCU configurations are shown in Fig. 7. The plots illustrate the close agreement between reference and measured signals for speed and armature current, confirming that the proposed analog-domain coupling maintains dynamic fidelity while reducing current ripple and latency effects.

Since the proposed HIL platform employs analog-domain signal transmission, potential noise introduced by the PWM-LPF conversion and DAC-ADC interface may affect control accuracy. In practice, the impact of analog noise is mitigated by the low-pass filtering stage and the limited bandwidth of the control loop. The RC filter suppresses the PWM carrier components while preserving the low-frequency control signal. In addition, the ADC and DAC modules of the TMS320F28379D provide sufficient resolution to ensure accurate signal representation.

The experimental results in Table 5 indicate that the closed-loop control accuracy is not significantly affected by the analog communication link. The speed-tracking RMSE remains comparable between the single-MCU and dual-MCU configurations, and the steady-state error remains within a small voltage range. These results confirm that the analog-domain interface introduces negligible noise impact for the tested operating conditions.

In practical implementations, several non-ideal factors may influence control performance, including sensor noise, ADC/DAC quantization, actuator saturation, and

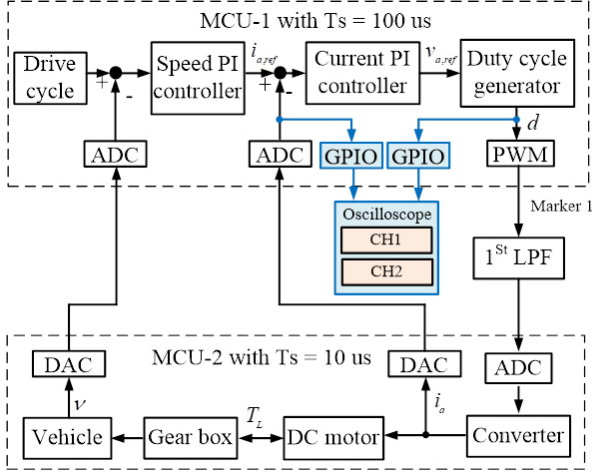


Fig. 5: Round-Trip Latency Measurement Using GPIO Markers and an Oscilloscope.

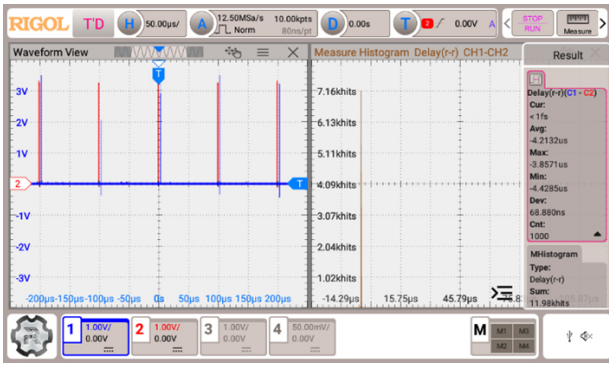


Fig. 6: Oscilloscope Measurement of Round-Trip Latency between CH1 (Command Issued) and CH2 (Feedback received), showing an Average Delay of $4.21 \mu\text{s}$ with 68.9 ns Jitter over 1000 Samples.

low-speed operation. In the proposed platform, the analog signals exchanged between the controller and plant processors are represented within a 0–3.3 V range using the on-chip 12-bit ADC and DAC modules of the TMS320F28379D. This resolution provides a voltage step size of approximately 0.8 mV, which is sufficiently small relative to the signal magnitude used in the control loop. As a result, quantization effects remain negligible for the tested operating conditions.

Sensor noise and switching ripple are partially attenuated by the RC low-pass filtering stage used in the PWM–LPF conversion, which removes high-frequency components of the PWM carrier while preserving the low-frequency control signal. In addition, actuator saturation limits are implemented in the controller to constrain the duty-cycle command within the allowable operating range.

The experimental results shown in Fig. 8 and Table 5 demonstrate stable closed-loop behavior under both step-reference tests and drive-cycle conditions, including low-speed operation. The small steady-state error and comparable RMSE values confirm that the proposed

Table 4: Measured Round-Trip Latency and Jitter of the Analog-Domain Communication Link.

Parameter	Value	Unit	Measurement Method
Average latency	4.21	μs	Oscilloscope delay histogram
Minimum latency	3.86	μs	Oscilloscope delay histogram
Maximum latency	4.43	μs	Oscilloscope delay histogram
Latency jitter (std. dev.)	68.9	ns	Oscilloscope delay histogram
Number of samples	1000	—	Histogram acquisition

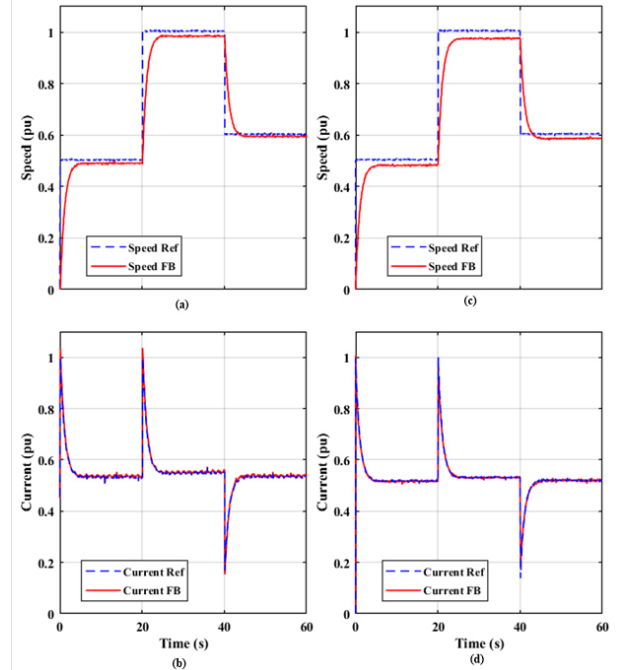


Fig. 7: Step responses of the single-MCU and dual-MCU HIL systems for a speed reference change from 0.5 p.u. to 1.0 p.u. and back to 0.5 p.u.. (a) Single-MCU speed response, (b) single-MCU armature current, (c) dual-MCU speed response, and (d) dual-MCU armature current.

analog-domain communication interface does not introduce noticeable degradation in control performance under these practical non-ideal conditions.

4.3 Drive-Cycle Tracking

Under the corner-mixed interpolated drive-cycle profile, both systems followed the 40 km/h velocity trajectory closely. The dual-MCU platform achieved RMSE = 0.16 V, nearly matching the single-MCU baseline (0.15 V). Notably, current ripple decreased by $\approx 5 \%$, demonstrating that analog-domain coupling does not compromise fidelity even during fast acceleration transients. These results validate the platform's ability to emulate realistic EV-drive dynamics with minimal

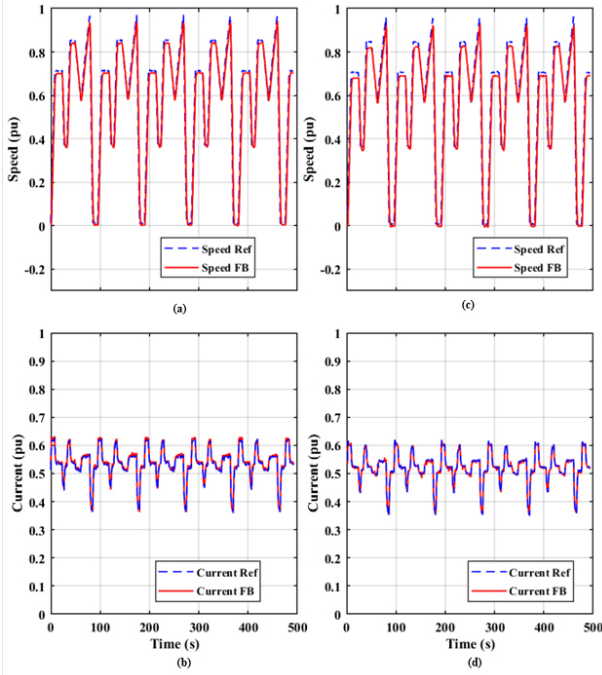


Fig. 8: Speed and armature current responses under the corner-mixed interpolated drive-cycle test. (a) Single-MCU speed response, (b) single-MCU armature current, (c) dual-MCU speed response, and (d) dual-MCU armature current.

latency and high stability.

The corresponding drive-cycle responses for both single- and dual-MCU configurations are shown in Fig. 8. The plots present the velocity and armature-current trajectories under the corner-mixed interpolated profile, confirming that the dual-MCU system reproduces the same transient behavior as the single-MCU setup while maintaining smoother current response and stable speed tracking.

4.4 Scalability and Resource Utilization

Oscilloscope-based CPU profiling revealed 10.64% total utilization in the single-MCU HIL configuration. In the dual-MCU setup, the controller MCU (MCU1) consumed only 3.87%, while the plant MCU (MCU2) used 10.59%. These results indicate substantial computational headroom on both processors, allowing for future extension to multi-motor, three-phase PMSM emulation, or the integration of more advanced control algorithms without requiring hardware modification.

Collectively, these results confirm that the proposed analog-linked dual-MCU HIL system delivers equivalent control accuracy to a monolithic configuration while achieving lower current ripple, deterministic timing, and better scalability.

Quantitative performance metrics for both configurations are summarized in Table 5. The dual-MCU implementation achieves comparable speed-tracking accuracy to the single-MCU configuration, with identical RMSE values of 0.23 V in the step test and similar performance

under the corner-mixed drive-cycle profile. In addition, the dual-MCU architecture significantly reduces the computational burden on the control processor, decreasing total CPU utilization from 10.64% in the single-MCU setup to 3.87% on MCU1 while distributing the plant computation to MCU2.

The corresponding waveform responses are illustrated in Figs. 7 and 8, which confirm stable transient behavior and consistent tracking performance for both architectures.

These results demonstrate that the proposed analog-linked dual-MCU HIL platform preserves control performance while improving timing determinism and computational scalability.

4.5 Comparison with Existing HIL Platforms

To better position the proposed platform within the landscape of real-time HIL solutions, Table 6 presents a qualitative comparison with representative commercial systems including dSPACE, Typhoon HIL, and OPAL-RT. While commercial HIL platforms provide extremely high computational performance and scalability, they typically require specialized hardware and significant cost. In contrast, the proposed dual-MCU architecture uses standard microcontroller boards and analog-domain signal coupling to achieve deterministic sub-10 μ s latency at a substantially lower hardware cost. This trade-off makes the proposed platform particularly attractive for academic laboratories and embedded-control research requiring accessible real-time experimentation.

In addition to latency and implementation complexity, hardware affordability is an important consideration for many academic laboratories. Table 7 provides a rough comparison of the hardware cost between the proposed dual-MCU HIL platform and several widely used commercial real-time simulation systems. The proposed system relies only on commercially available microcontroller development boards and simple analog interface circuitry, resulting in a total hardware cost on the order of a few hundred USD. In contrast, commercial HIL platforms such as dSPACE, Typhoon HIL, and OPAL-RT typically require specialized real-time simulation hardware whose system cost can exceed tens of thousands of USD. This cost difference highlights the practicality of the proposed approach for low-cost research and educational applications.

To further highlight the advantage of the proposed analog-domain communication method, Table 8 compares the latency characteristics of several commonly used microcontroller communication interfaces. Digital protocols such as UART, CAN, and SPI rely on packet-based data exchange and protocol handling, which introduces additional transmission and synchronization delays. Even with DMA-assisted SPI transfer, the latency typically remains in the order of several microseconds due to data framing and transfer scheduling.

In contrast, the proposed analog-domain interface directly transmits control signals through a PWM-LPF

Table 5: Performance Metrics of the Single-MCU and Proposed Dual-MCU HIL Configurations Evaluated under Step-Input and Corner-Mixed Drive-Cycle Tests.

Parameter		Single-MCU HIL			Dual-MCU HIL		
Control architecture		Speed PI controller	Current PI controller	Converter + DC motor + Vehicle	Speed PI controller	Current PI controller	Converter + DC motor + Vehicle
Sampling time (s)		1E-3	1E-4	1E-5	1E-3	1E-4	1E-5
Step input (0.5 to 1.0 to 0.5 pu.)	Rise time (s)	4.40	-	-	4.62	-	-
	Overshoot (V)	0.00	-	-	0.00	-	-
	Steady-state error (V)	0.05	-	-	0.07	-	-
	RMSE of speed tracking (v)	0.23	-	-	0.23	-	-
	Current peak (V)	-	3.01	-	-	3.02	-
	Current RMS (V)	-	1.66	-	-	1.61	-
Corner-mixed interpolated drive-cycle profile	Rise time (s)	12.10	-	-	12.00	-	-
	Overshoot (V)	0.00	-	-	0.00	-	-
	Steady-state error (V)	0.03	-	-	0.08	-	-
	RMSE of speed tracking (v)	0.15	-	-	0.16	-	-
	Current peak (V)	-	1.86	-	-	1.88	-
	Current RMS (V)	-	1.61	-	-	1.57	-
CPU load (%)		0.8501% (± 0.01)	10.99% (± 0.01)	2.803% (± 0.01)	0.82% (± 0.01)	3.05% (± 0.01)	10.59% (± 0.041)
		10.6431% (± 0.03)			3.87% (± 0.02)		10.59% (± 0.041)
System stability		Stable			Stable		
Data source		Oscilloscope (REGOL DHO 804)			Oscilloscope (REGOL DHO 804)		

Table 6: Qualitative Comparison of the Proposed dual-MCU Analog HIL Platform with Representative Real-Time HIL Systems. Vendor Specifications are Based on Publicly Available Documentation.

Comparison Aspect	Proposed Dual-MCU HIL (This Work)	dSPACE SCALEXIO [16]	Typhoon HIL 606 [17]	OPAL-RT [18]
Hardware architecture	Dual TI TMS320F28379D MCUs (control + plant)	Multi-core real-time CPU with FPGA I/O	ARM processor + Xilinx FPGA	Intel Xeon multi-core CPU + FPGA
Control-plant separation	Physical (dual MCU)	Physical (external controller)	Physical	Physical
Communication method	Analog-domain voltage signaling (PWM-LPF command + DAC-ADC feedback)	Proprietary digital backplane	Digital FPGA I/O	Digital high-speed I/O
Typical simulation step	10 μ s plant step	~ 1 –10 μ s	~ 200 ns – 1 μ s	~ 250 ns – 10 μ s
Measured latency	4.21 μ s (round-trip, measured)	Vendor-specified	Vendor-specified	Vendor-specified
Timing determinism	High (hardware-timer synchronized)	Very high	Very high	Very high
Jitter	68.9 ns (measured, std. dev.)	Very low	Very low	Very low
Signal observability	High (direct analog signals easily probed)	Limited (internal buses)	Limited	Limited
Scalability	Moderate (add MCU nodes)	High	High	Very high
Implementation complexity	Low–moderate	High	High	High
Accessibility	High (off-the-shelf MCU boards)	Low	Low	Low

conversion and DAC–ADC feedback path, eliminating protocol overhead and packet buffering. The measured round-trip latency of approximately 4.2 μ s, shown in

Fig. 6, demonstrates significantly faster and more deterministic communication compared with conventional digital interfaces. This characteristic makes the approach

Table 7: Hardware Cost Comparison of the Proposed Dual-MCU HIL Platform and Commercial HIL Systems (Estimated from Publicly Available Vendor Information).

Platform	Typical hardware configuration	Estimated hardware cost	Notes
Proposed Dual-MCU HIL (This work)	2 × TI TMS320F28379D LaunchPad + analog interface circuit	On the order of 100–300 USD	Commercial MCU development boards
dSPACE real-time simulator [16]	Dedicated real-time simulation hardware	Tens to over one hundred thousand USD	Industrial HIL system
Typhoon HIL [17]	FPGA-based power electronics HIL platform	Tens of thousands USD	Specialized real-time simulator
OPAL-RT [18]	Multi-core CPU / FPGA real-time simulator	Tens of thousands USD	High-performance HIL system

Table 8: Communication Interfaces Comparison (UART, CAN, SPI, SPI-DMA, and the Proposed Analog-Domain Link) in Terms of Latency, Determinism, and CPU Overhead.

Communication Interface	Typical Data Transfer Method	Latency Range*	Determinism	CPU Overhead	Remarks
UART	Asynchronous serial communication	50–200 μ s	Low	Medium	Protocol framing and baud-rate limitation
CAN	Packet-based bus	100–500 μ s	Medium	Medium	Arbitration delay and message scheduling
SPI (Polling)	Synchronous serial communication	10–30 μ s	Medium	High	CPU blocking during transfer
SPI-DMA	DMA-assisted transfer	5–15 μ s	Medium	Low	Reduced CPU load but still packet-based
Proposed Analog Link	PWM-LPF + DAC-ADC	$\approx$ 4.2 μ s	High	Low	No protocol overhead, deterministic timing

*Latency characteristics of conventional digital interfaces are derived from the device technical reference manual [19] under typical operating conditions.

suitable for high-speed real-time HIL applications where sub-10 μ s timing response is required.

5. DISCUSSION AND EXTENDIBILITY

5.1 Analog-Domain Coupling as a Timing Solution

Achieving a measured 4.21 μ s round-trip delay confirms that PWM-LPF and DAC-ADC signaling can replace digital buses in short-period control loops. This is significant because deterministic response below 10 μ s is generally attainable only on FPGA-based systems. The results therefore demonstrate that microcontroller-level HIL can meet industrial real-time requirements when analog communication is exploited.

5.2 Architectural Scalability

With CPU utilization below 11% on each MCU, more than 85% computational margin remains available for implementing higher-order models such as three-phase PMSM or BLDC drives. Since each MCU operates autonomously and communicates via analog-domain signals, additional nodes can be added without re-configuring digital protocols. This modular structure supports scalable co-simulation architectures and multi-drive coordination studies.

The entire workflow—from Simulink model to hardware deployment—is fully reproducible, enabling lab-

oratories to teach embedded control with observable real-time behaviour. Students can visualize controller states via DAC outputs, connecting theoretical control equations with physical signal response.

5.3 Limitations and Future Directions

Analog-domain coupling provides deterministic performance without protocol overhead, but it also introduces practical limitations. During implementation, the analog feedback path showed sensitivity to GND reference integrity between the two MCUs, occasionally introducing minor ripple or noise disturbances in the measured signal. Additionally, longer cable lengths may cause offset drift and attenuation, reducing feedback accuracy.

The system is also constrained by the 12-bit resolution of the DAC and ADC peripherals, which limits signal fidelity, especially in low-speed or low-current operating regions where quantization effects become more pronounced. The reconstruction of duty-cycle signals via PWM and low-pass filtering introduces inherent bandwidth and phase delay constraints, which may degrade responsiveness at high control frequencies.

These trade-offs should be considered in future system revisions. Potential enhancements include:

- Integrating hybrid analog-digital communication for

improved flexibility

- Implementing active filtering or dynamic offset calibration to mitigate signal degradation
- Exploring synchronization techniques for scaling to multi-node systems or distributed control architectures

These improvements can extend the platform's applicability to high-precision systems, while preserving its low-cost, modular structure.

This discussion confirms that the proposed analog-linked dual-MCU architecture is not merely a proof-of-concept, but a practical and extensible engineering framework. By bridging the gap between academic experimentation and real-world embedded drive validation, it offers a reproducible, cost-effective, and scalable alternative to commercial HIL systems.

6. CONCLUSION

This work has presented a dual-MCU hardware-in-the-loop platform that partitions embedded motor control and plant simulation across two TMS320F28379D microcontrollers interconnected through pure analog links. The system attains sub-10 μ s round-trip latency and reliable real-time performance, confirmed through step and drive-cycle experiments. Comparative analysis with a single-MCU reference showed equivalent tracking accuracy and slightly improved current ripple, validating the method's practicality for EV drive control studies.

The approach's novelty lies in combining analog-communication realism with auto-generated embedded code, providing a reproducible and low-cost alternative to commercial HIL simulators. Beyond DC-drive emulation, the modular design can extend to three-phase PMSM or BLDC systems, fault-injection testing, and adaptive-control algorithm validation.

Future work will integrate digital-bus coupling (SPI or EtherCAT) for hybrid analog-digital HIL comparison, explore automatic calibration of analog paths, and evaluate multi-node synchronization for distributed-drive applications. These extensions aim to establish a comprehensive, open, and affordable HIL environment for next-generation electric-drive education and research.

Nomenclature:

$i_{a,ref}$ - Armature Current Reference [A]
 d - Duty Ratio
 K_{ps} - Proportional Gain for Speed Controller
 K_{is} - Integral Gain for Speed Controller [1/s]
 e_v - Speed Error [rad/s]
 T_s - Sampling Time [s]
 K_{pc} - Proportional Gain for Current Controller
 K_{ic} - Integral Gain for Current Controller [1/s]
 e_i - Current Error [A]
 V_a - Motor Terminal Voltage [V]
 V_{dc} - DC Link Voltage [V]
 i_a - Armature Current [A]
 L_a - Armature Inductance [H]
 R_a - Armature Resistance Ω
 k_e - Back-EMF Constant V/(rad/s)

ω - Angular Speed rad/s
 J - Moment of Inertia kg·m²
 k_t - Torque Constant Nm/A
 B - Viscous Friction Coefficient Nms/rad
 T_L - Load Torque Nm
 T_m - Motor Torque Nm
 T_{out} - Wheel Torque Nm
 η_g - Gearbox Efficiency
 GR - Gear Ratio
 v - Vehicle Velocity [km/h]
 m - Vehicle Mass [kg]
 r - Wheel Radius [m]
 F_{rr} - Rolling Resistance Force [N]
 F_d - Aerodynamic Drag Force [N]
 F_{grade} - Grade Resistance Force [N]
 C_{rr} - Rolling Resistance Coefficient
 g - Gravitational Acceleration [m/s²]
 ρ - Air Density [kg/m³]
 C_d - Drag Coefficient
 A_{front} - Frontal Area [m²]
 θ - Road Slope Angle [deg]
 I_{rated} - Rated Current [A]
 V_{rated} - Rated Voltage [V]
 N_{rated} - Rated Speed [rpm]
 I_{base} - Base Current [A]
 V_{base} - Base Voltage [V]
 v_{base} - Base Velocity [km/h]
RMSE - Root Mean Square Error [V]
EV - Electric Vehicle
HIL - Hardware-in-the-Loop
PI controller - Proportional-Integral Controller
MCU - Microcontroller Unit
PWM - Pulse-Width Modulation
DAC - Digital-to-Analog Converter
ADC - Analog-to-Digital Converter
SPI - Serial Peripheral Interface
UART - Universal Asynchronous Receiver Transmitter
CAN - Controller Area Network
ECU - Electronic Control Unit8
LPF - Low-Pass Filter
ePWM module - Enhanced PWM
CPU - Central Processing Unit
GPIO - General Purpose Input/Output
FPGA - Field-Programmable Gate Array
BLDC - Brushless DC Motor
PMSM - Permanent Magnet Synchronous Motor

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