

A Simplified Analog Implementation of Cyclic Shift Chirp Encoding and Decoding for LoRa Communications

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ABSTRACT

Currently, LoRa wireless communication technology has become widely adopted in IoT systems due to its long-range capability and low power consumption. However, LoRa is a technology developed by Semtech, which does not disclose the details of the Cyclic Shift Chirp encoding process, a core component of LoRa signals. This lack of transparency prevents users from accessing the physical-layer structure of the signal or freely customizing key parameters such as bandwidth and spreading factor. Although such customization can enhance system flexibility, there is currently no officially disclosed method to achieve it. This research proposes a Cyclic Shift Chirp encoder/decoder circuit built from basic analog components, including adders, subtractors, comparators, and ramp generators, based on a Pulse Width Modulation (PWM) principle. This approach enables researchers and developers to generate LoRa-like signals independently and customize various parameters without introducing limitations. Moreover, the proposed circuit is simple, low-cost, and easy to understand, making it suitable for advanced research, educational experiments, and the design of communication systems that require high flexibility at the LoRa PHY layer.

Keywords: LoRa, Cyclic Shift Chirp, analog circuit, encoding, decoding, PWM, IoT communications

1. INTRODUCTION

The internet of things (IoT) has been significantly integrated into daily life, with widespread deployment of IoT devices primarily utilizing Wireless IoT technologies based on Wi-Fi. However, Wi-Fi technology presents limitations in terms of range and power consumption. Technological advancement has led to the development of Long Range Low Power (LRLP) technologies such as LoRaWAN, NB-IoT, and Sigfox, enabling transmission over several kilometres with minimal power consumption. Although these technologies offer low data rates,

they are well-suited for wide-area IoT applications, including LoRa-based deployments in smart cities, smart farming, smart parking, wireless sensor networks [1,2], wildlife monitoring [3], and healthcare systems [4,5].

Currently, LoRaWAN is predominantly used in LP-WAN applications due to its utilization of unlicensed frequency bands, eliminating spectrum licensing costs. In contrast, NB-IoT operates on cellular networks requiring service fees to mobile network operators. LoRaWAN is fundamentally based on LoRa modulation, which represents Semtech's proprietary physical layer technology.

LoRa modulation comprises essential components including the conversion of incoming digital data into Cyclic Shift Chirp (CSC) symbol signals, followed by Voltage Controlled Oscillator (VCO) processing to generate LoRa modulated signals. Previous attempts at reverse engineering LoRa circuits and modulation methods have primarily employed Software Defined Radio (SDR) for LoRa signal simulation. However, SDR implementations present common limitations including excessive processing time, high power consumption, and complexity.

Busacca et al. [6] utilized SDR for reverse engineering LoRa signal generation for both transmission and reception, conducting tests on the colosseum platform and publishing source code on GitHub. The primary limitation identified was clock signal accuracy in SDR systems.

Research in [7] employed the GNU Radio platform, demonstrating correct operation even at low SNR levels. The study presented efficient algorithms for estimating and compensating Sampling Time Offset (STO) and Carrier Frequency Offset (CFO) using the Rational Combination of Three Spectral Lines (RCTSL) method.

The GitHub platform [8] introduced the gr-lora project for GNU radio block diagrams for receiving LoRa modulated radio signals using SDR.

Research in [9] presented the use of open source SDR for LoRa modulation signal simulation.

Study [10] utilized National Instruments USRPs SDR for simulation and experimentation with demodulation methods using dechirp followed by DFT, analysing Carrier Frequency Offset (CFO) compensation techniques.

Sinchai et al. [11] presented analog circuitry for CSC symbol signal generation using analog circuits including adders, timed integrators, inverting amplifiers, sawtooth generators, and analog switches for controlling integrator timing.

Subsequently, Lerson et al. [12] proposed encoding

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and decoding circuits for single slope CSC symbol signals using analog devices such as op-amps, incorporating basic circuits including adders, multipliers, sawtooth generators, comparators, and inverting amplifiers.

This paper proposes an improved single slope CSC symbol signal encoding circuit based on work [12], specifically designed to eliminate the use of multiplication circuits, which are inherently complex. The proposed circuit utilizes only basic analog components including RAMP generators, adders, subtractors, and comparators.

This design reduces complexity, component count, and cost, while enabling independent generation of LoRa-modulated signals and flexible parameter customization. Users can easily adjust the bandwidth by changing the amplitude of the CSC symbol signal and modify the spreading factor by altering the period (T) of the sawtooth signal, providing practical flexibility for experimentation and research.

The main contributions of this work are summarized as follows:

1. Simplified analog CSC circuit design: The proposed single slope CSC encoder/decoder employs only basic analog components and avoids complex multipliers, significantly reducing circuit complexity, cost, and component count. Consequently, the reduced number of components results in lower overall power consumption.
2. Flexible parameter customization: The design allows easy adjustment of key LoRa modulation parameters, such as bandwidth (via signal amplitude) and spreading factor (via sawtooth period), without introducing limitations in practical usage.
3. Accessible and low-cost implementation: The circuit is suitable for researchers, educators, and developers who wish to study or experiment with LoRa PHY concepts without relying on SDR or proprietary hardware.
4. Practical utility for LoRa PHY studies: The design provides a platform for independent LoRa signal generation, enabling studies of signal behaviour, modulation parameter evaluation, and support for educational and experimental applications in wireless communications research.

In this work, the term “CSC symbol” refers to the implementation derived from the single slope CSC principle introduced in [12]. For consistency and simplicity, the terminology “CSC symbol” is used throughout the remainder of this paper.

2. CYCLIC SHIFT CHIRP SYMBOL

The CSC symbol signal serves as the fundamental signal for FM modulation to generate LoRa signal or chirp modulated signal, as illustrated in Fig. 1.

The CSC symbol signal exhibits RAMP characteristics where the signal’s phase position varies according to the incoming analog input voltage level. Fig. 2 demonstrates CSC symbol signals at four different analog input voltage levels.

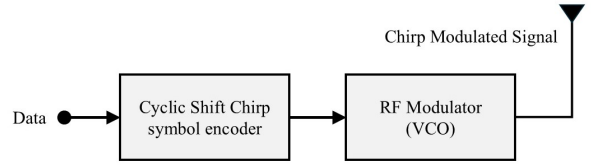


Fig. 1: Basic block diagram for LoRa signal generation.

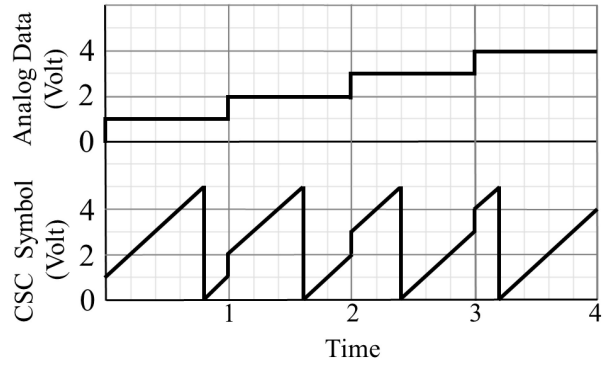


Fig. 2: Cyclic Shift Chirp symbol signal versus 4-level analog signal.

The CSC symbol signal equation $s(t)$ can be expressed as:

$$s(t) = \text{Ramp}(2\pi ft + \theta_n) \quad (1)$$

Where the signal phase varies according to the incoming analog input voltage:

$$\theta_n \propto m(t) \quad (2)$$

For 2-bit data processed through a Digital-to-Analog Converter, four voltage levels are generated, corresponding to four distinct phases separated by $2\pi/4$ equal to $\pi/2$.

3. LORA PHYSICAL LAYER

LoRa communication involves several key parameters including carrier frequency, bandwidth, spreading factor, and chip rate. Each parameter is briefly described below.

Carrier frequency represents the center frequency used for communication, where CSC symbol signals undergo FM modulation. This frequency is designated within ISM bands for specific geographical regions, such as 868 MHz for Europe and 915 MHz for North America.

Bandwidth defines the frequency span around the center frequency from minimum to maximum frequencies. In FM modulation using Voltage Controlled Oscillators (VCO), minimum input voltage produces the lowest frequency span from center frequency, while maximum input voltage generates the highest frequency span. In LoRa communication, the VCO input signal is the CSC symbol signal; therefore, LoRa signal bandwidth depends on the CSC symbol signal amplitude: $\Delta f = k_{vco} \bullet \text{Amplitude}$

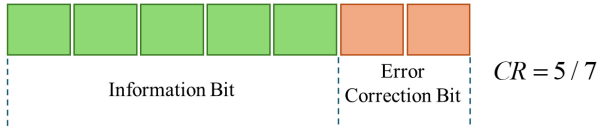


Fig. 3: Information bits to error correction bits ratio defining code rate.

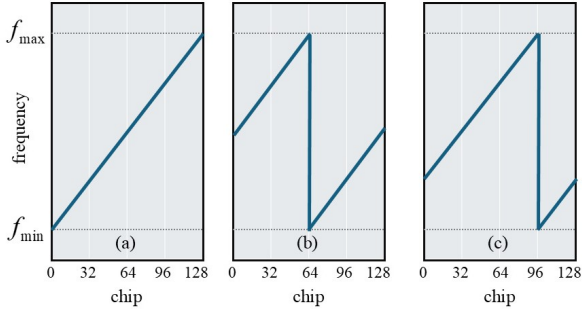


Fig. 4: Cyclic Shift Chirp signals for each chip. (a) Basic chirp signal representing data 0, comprising 128 chips sweeping from $f_{\min}$ to $f_{\max}$, (b) Chirp signal representing data 64, comprising 128 chips sweeping from $f_{\min}$ to $f_{\max}$, and (c) Chirp signal representing data 96, comprising 128 chips sweeping from $f_{\min}$ to $f_{\max}$

Code Rate (CR) represents the ratio between data bits and total bits including error correction bits (e.g., 4/5, 4/6, 5/7, 4/8), typically employing Hamming Code for forward error correction, as shown in Fig. 3.

Spreading Factor (SF) indicates the number of bits per symbol generation. For $SF = 7$, there are $2^7 = 128$ CSC signals (symbols), where each symbol represents 7 bits (0-127).

Each symbol comprises 2^{SF} chips, which are time-varying signals. One symbol period is divided into 2^{SF} small time intervals.

For $SF = 7$, some example symbols are presented in Fig. 4.

Chip Rate defines the chip change rate per second from minimum to maximum frequency. For 125 kHz bandwidth, up to 125,000 chips per second are possible. Therefore, one chip transmission time equals $1/(f_{\max} - f_{\min})$ or $1/\text{Bandwidth}$:

$$T_{\text{chip}} = \frac{1}{BW} \quad (3)$$

One symbol transmission time equals:

$$T_{\text{symbol}} = 2^{SF} \cdot T_{\text{chip}} = \frac{2^{SF}}{BW} \quad (4)$$

Symbol Rate (SR) represents symbols transmitted per second:

$$SR = \frac{1}{T_{\text{symbol}}} = \frac{BW}{2^{SF}} \quad (5)$$

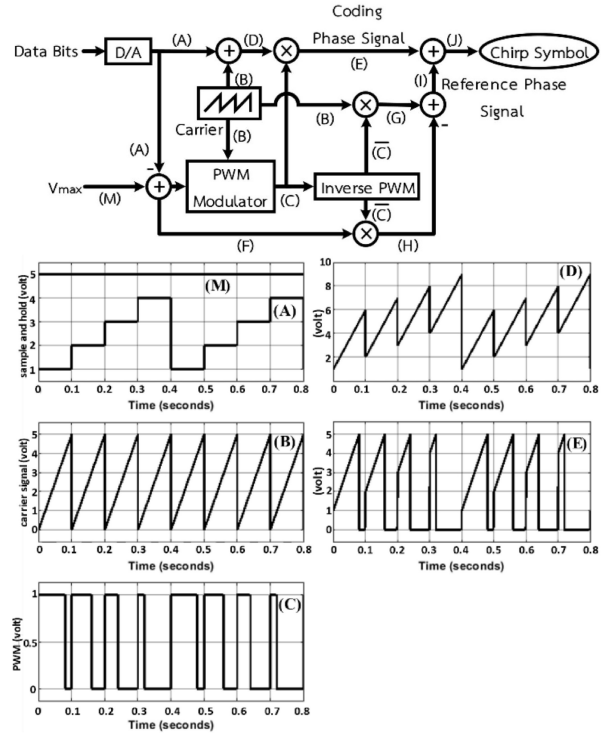


Fig. 5: Circuit proposed in research [12] and signal waveforms at various points.

Bit Rate indicates bits transmitted per second, where one symbol represents SF bits:

$$\text{Bit rate} = SF \cdot \frac{BW}{2^{SF}} \quad (6)$$

Data Rate (DR) represents actual data transmitted per second, incorporating code rate effects:

$$DR = SF \cdot \frac{BW}{2^{SF}} \cdot CR \quad (7)$$

4. PROPOSED CIRCUIT

4.1 Cyclic Shift Chirp Encoder Circuit

The proposed circuit improves upon Lerson et al.'s work [12] through mathematical analysis of the block diagram shown in Fig. 5.

From the mathematical analysis of the block diagram in Fig. 5, the following results are derived.

Position A: Analog voltage signal from Digital to Analog converter: $A = m(t)$

Position B: RAMP signal: $B = v_{\text{ramp}}(t)$

Position C: PWM signal: $C = v_{\text{PWM}}(t)$

Position D: Sum of RAMP and analog voltage signals:

$$D = m(t) + v_{\text{ramp}}(t) \quad (8)$$

Therefore, signal at position E:

$$E = (m(t) + v_{\text{ramp}}(t)) \cdot v_{\text{PWM}}(t) \quad (9)$$

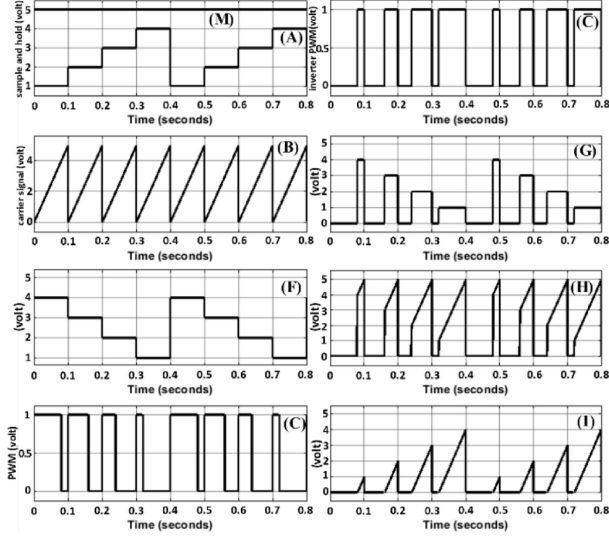


Fig. 6: Signal waveforms at various points in research [12].

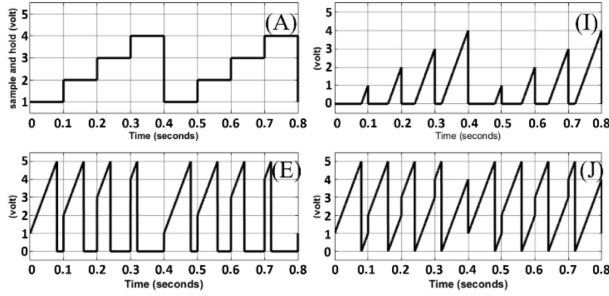


Fig. 7: Signal waveforms at various points in research [12].

Considering the next section, the signal waveform is shown in Fig. 6.,

Position B: RAMP signal: $B = v_{ramp}(t)$

Position $\bar{C}$: Inverse PWM signal:

$$\bar{C} = 1 - v_{PWM}(t) \quad (10)$$

Position F: Inverted analog voltage:

$$F = v_{max} - m(t) \quad (11)$$

Therefore: Signal at position G:

$$G = (1 - v_{PWM}(t)) \cdot v_{ramp}(t) \quad (12)$$

Signal at position H:

$$H = (1 - v_{PWM}(t)) \cdot (v_{max} - m(t)) \quad (13)$$

Signal at position I:

$$\begin{aligned} I &= G - HI \\ &= (1 - v_{PWM}(t)) \cdot v_{ramp}(t) \\ &\quad - (1 - v_{PWM}(t)) \cdot (v_{max} - m(t)) \end{aligned} \quad (14)$$

From the block diagram in Fig. 5, and signal wave from is depicted in Fig. 7, the CSC symbol signal equation

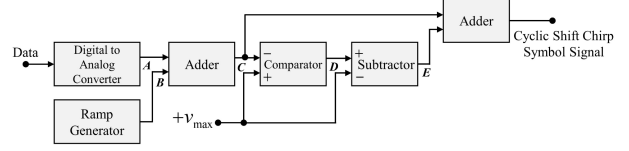


Fig. 8: Block diagram of Simplified Cyclic Shift Chirp symbol signal encoder.

(Position J) becomes:

$$\begin{aligned} v_{CSC}(t) &= J = E + I \\ v_{CSC}(t) &= (m(t) + v_{ramp}(t)) \cdot v_{PWM}(t) \\ &\quad + (1 - v_{PWM}(t)) \cdot v_{ramp}(t) \\ &\quad - (1 - v_{PWM}(t)) \cdot (v_{max} - m(t)) \end{aligned} \quad (15)$$

Rearranging the equation:

$$\begin{aligned} v_{CSC}(t) &= m(t) \cdot v_{PWM}(t) + v_{ramp}(t) \cdot v_{PWM}(t) \\ &\quad + v_{ramp}(t) - v_{PWM}(t) \cdot v_{ramp}(t) \\ &\quad - (v_{max} - v_{PWM}(t)) \cdot v_{max} \\ &\quad - m(t) + v_{PWM}(t) \cdot m(t) \end{aligned} \quad (16)$$

$$\begin{aligned} v_{CSC}(t) &= m(t) \cdot v_{PWM}(t) + v_{ramp}(t) \cdot v_{PWM}(t) \\ &\quad + v_{ramp}(t) - v_{PWM}(t) \cdot v_{ramp}(t) - v_{max} \\ &\quad + v_{PWM}(t) \cdot v_{max} + m(t) - v_{PWM}(t) \cdot m(t) \end{aligned} \quad (17)$$

$$v_{CSC}(t) = m(t) + v_{ramp}(t) + v_{PWM}(t) \cdot v_{max} - v_{max} \quad (18)$$

Since v_{max} is a DC voltage or mathematical constant, the term $v_{PWM}(t) \cdot v_{max}$ represents a PWM signal with output voltage equal to v_{max} . Therefore, CSC symbol signal generation can be simplified without multiplication circuits, using only RAMP generators, D-to-A converters, adders, comparators, and subtractors.

From Equation (18), the simplified CSC symbol signal generation block diagram is shown in Fig. 8.

Based on the analysis of the block diagram in Fig. 8, the results are obtained as follows.

Position A: Analog voltage signal from D-to-A converter: $A = m(t)$

Position B: RAMP signal: $B = v_{ramp}(t)$

Position C: Sum of RAMP and analog voltage signals:

$$C = m(t) + v_{ramp}(t)$$

Position D: PWM signal: $D = v_{PWM}(t) \cdot v_{max}$

Position E: Signal: $E = v_{PWM}(t) \cdot v_{max} - v_{max}$

Therefore: CSC symbol signal is

$$v_{CSC}(t) = C + E$$

$$v_{CSC}(t) = m(t) + v_{ramp}(t) + v_{PWM}(t) \cdot v_{max} - v_{max} \quad (19)$$

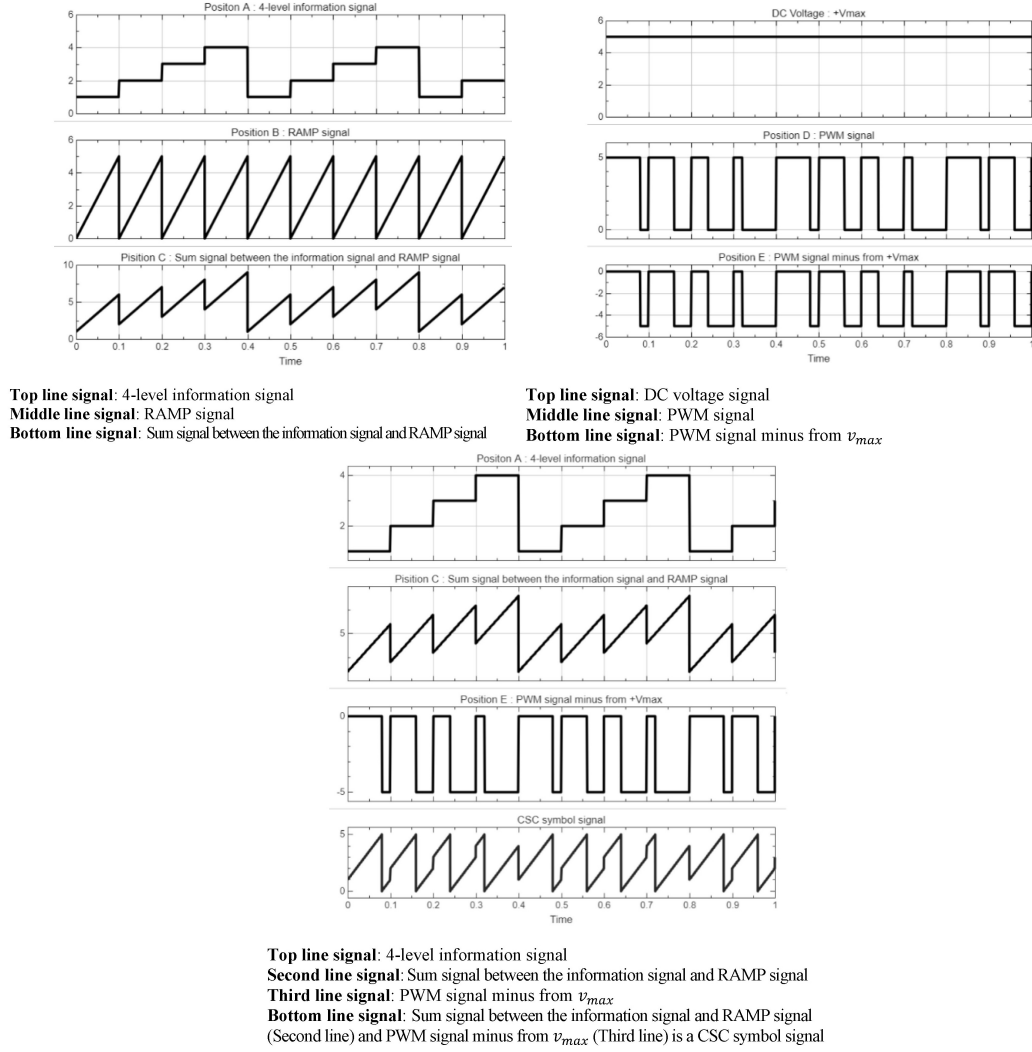


Fig. 9: Simulation results of CSC symbol signal generation at each position.

It can be observed that Equation (19), derived from the analysis of the block diagram in Fig. 8, is identical to the result obtained from Equation (18).

Simulation results showing signals at each position are presented in Fig. 9.

Circuit design and implementation results are shown in Fig. 10.

The simulation results in Fig. 9 are consistent with the experimental circuit results shown in Fig. 10.

4.2 Cyclic Shift Chirp Decoder Circuit

From the CSC symbol signal equation (19), the signal contains the message signal term $m(t)$. Therefore, message signal recovery can be achieved by:

$$m(t) = v_{CSC}(t) - v_{ramp}(t) - v_{PWM}(t) \bullet v_{max} + v_{max} \quad (20)$$

The simplified block diagram for message signal $m(t)$ recovery from CSC symbol signals is shown in Fig. 11.

Based on the analysis of the block diagram in Fig. 11, the results are obtained as follows.

Position A: CSC symbol signal

Position B: RAMP signal: $B = v_{ramp}(t)$

Position C: Difference between CSC symbol signal and RAMP signals:

$$C = v_{CSC}(t) - v_{ramp}(t) \quad (21)$$

Position D: Negative PWM signal:

$$D = -v_{PWM}(t) \bullet v_{max} \quad (22)$$

Position E: Difference signal:

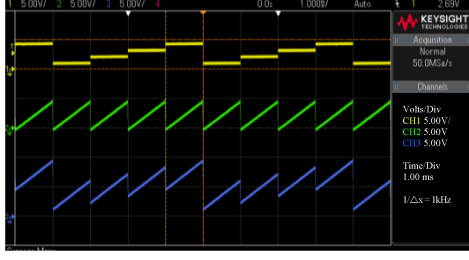
$$E = v_{CSC}(t) - v_{RAMP}(t) - v_{PWM}(t) \bullet v_{max} \quad (23)$$

And output signal:

$$m(t) = E + offset\ voltage \quad (24)$$

In General case, offset voltage is 0 Volt. It is evident that Equation (24), derived from the block diagram analysis in Fig. 11, yields the same result as Equation (20).

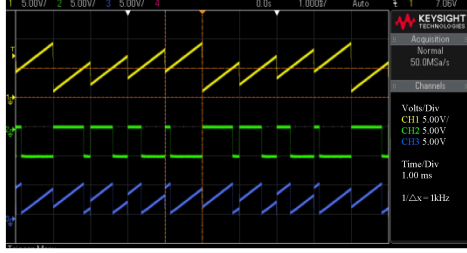
Simulation results showing signals at each position are presented in Fig. 12.



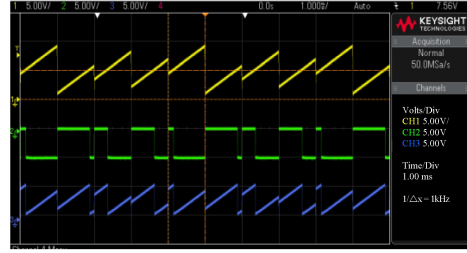
Top line signal: 4-level information signal
Middle line signal: RAMP signal
Bottom line signal: Sum signal between the information signal and RAMP signal



Top line signal: DC voltage signal
Middle line signal: Sum signal between the information signal and RAMP signal
Bottom line signal: PWM signal minus from v_{max}



Top line signal: Sum signal between the information signal and RAMP signal
Middle line signal: PWM signal minus from v_{max}
Bottom line signal: Sum signal between the information signal and RAMP signal (Top line) and PWM signal minus from v_{max} (Middle line) is a CSC signal



Top line signal: Sum signal between the information signal and RAMP signal
Middle line signal: PWM signal minus from v_{max}
Bottom line signal: Sum signal between the information signal and RAMP signal (Top line) and PWM signal minus from v_{max} (Middle line) is a CSC signal

Fig. 10: Experimental results from actual circuit implementation.

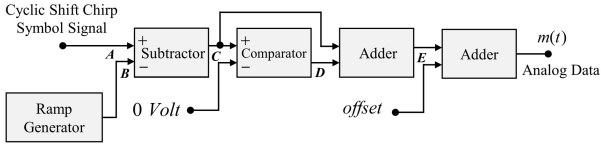


Fig. 11: Block diagram of Cyclic Shift Chirp symbol signal decoder.

The results of the circuit design and implementation are presented in Fig. 13.

The simulation results presented in Fig. 12 are in good agreement with the experimental circuit results shown in Fig. 13.

5. PERFORMANCE ANALYSIS

This section evaluates the performance of the proposed CSC architecture from both system-level and circuit-level perspectives. First, communication reliability is assessed through bit error rate (BER) simulations. Next, the robustness of the decoder against ramp synchronization mismatch is examined. The hardware efficiency of the proposed design is then evaluated by comparing its power consumption with that of the reference architecture. Finally, the thermal stability of the proposed ramp generator is analyzed to ensure reliable operation under varying temperature conditions.

A. Bit Error Rate (BER)

The performance of the proposed CSC symbol encoder/decoder was evaluated through simulation in Simulink. Chirp symbols were generated and mapped

to waveforms using the FM Passband Modulation block, while the receiver employed the corresponding FM Passband Demodulation block for signal recovery. An additive white Gaussian noise (AWGN) channel was used to model channel impairments.

Since the decoded Cyclic Shift Chirp symbols appear as a four-level analog signal, a ADC block was employed to convert them into discrete data symbols prior to BER computation. The quantized output was then compared with the small delay of original transmitted sequence using the Error Rate Calculation block from the Simulink Communications Toolbox. The complete Simulink block diagram is shown in Fig. 14.

To validate the proposed technique, the BER performance was compared with the method reported in [12]. The results as a function of signal-to-noise ratio (SNR) are presented in Fig. 15.

The BER results show that the proposed technique achieves performance comparable to the simulation reported in [12] and the theoretical prediction in [12]. The curves exhibit similar slopes across the evaluated SNR range, indicating comparable robustness to AWGN. These results demonstrate the effectiveness of the proposed approach in maintaining reliable BER performance.

B. Sensitivity to RAMP Synchronization Mismatch

The primary impact of CSC symbol signal encoding/decoding is RAMP signal synchronization between transmitter and receiver due to signal phase shift effects.

From equation (20), if the receiver generates RAMP signals with mismatched phases, the PWM signal will

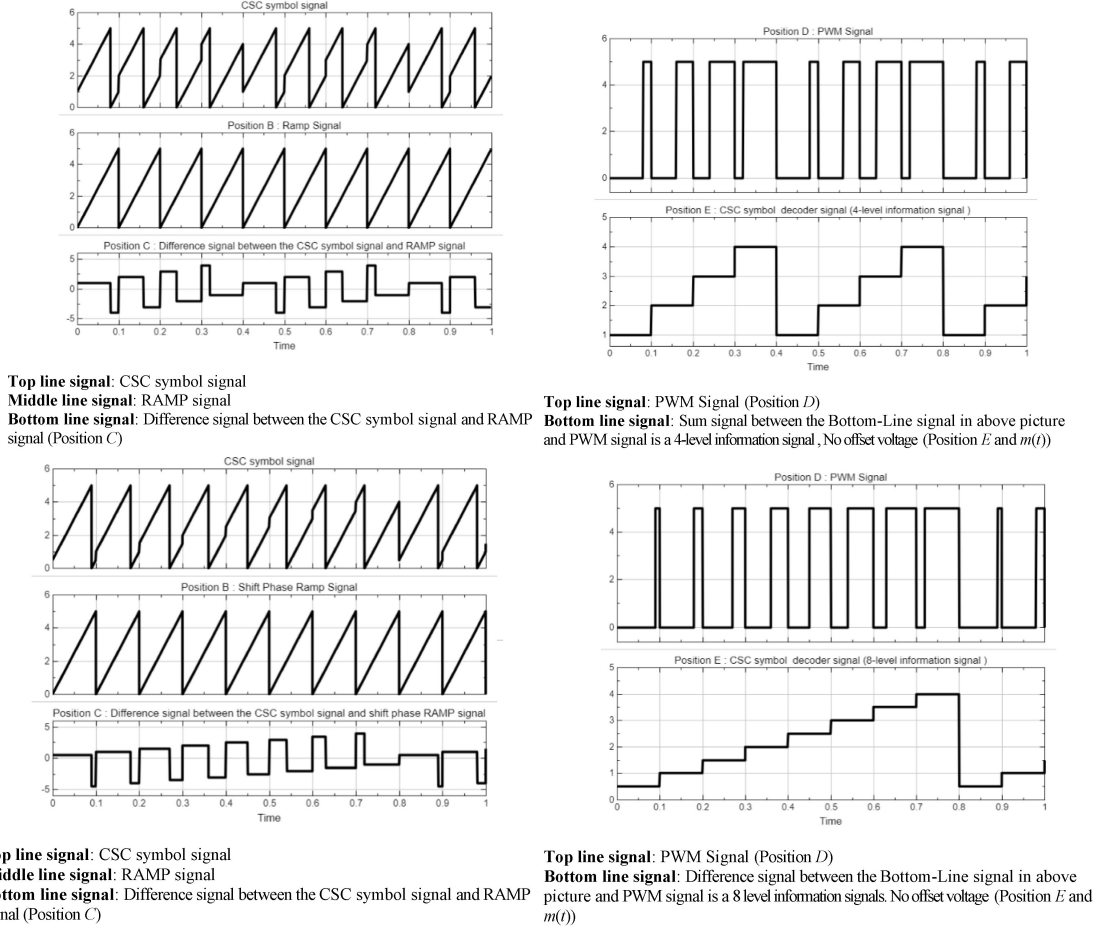


Fig. 12: Simulation results of CSC symbol decoder circuit.

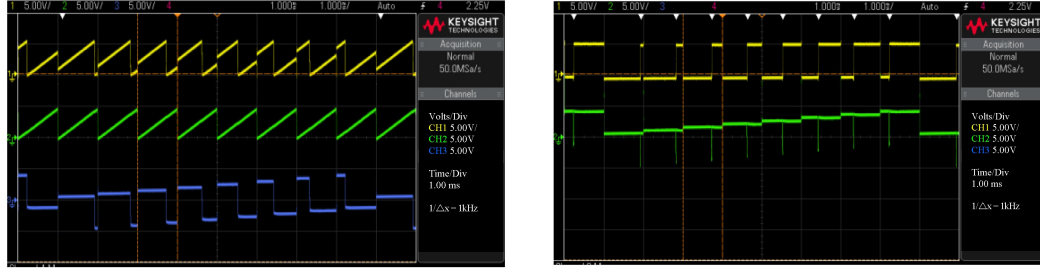


Fig. 13: Experimental results from actual circuit implementation.

experience similar phase shifts:

$$m(t) = v_{CSC}(t) - v_{ramp}(t + \theta) - v_{PWM}(t + \theta) \bullet v_{max} + v_{max} \quad (25)$$

Computer simulation results are shown in Fig. 16.

The analysis reveals that receiver-side signal phase shifts do not affect the $m(t)$ signal waveform, as comparator circuits clip noise generated by phase shifts. However, this results in DC offset in the output signal proportional to $\cos(\theta)$, which can be compensated using adder circuits with appropriate DC offset voltages.

To enable practical operation, the DC offset compen-

sation can be implemented automatically. One approach involves employing a low-bandwidth feedback loop that continuously estimates the mean value of the decoder output and adjusts the adder bias accordingly. Since the offset component varies slowly relative to the symbol dynamics, the loop bandwidth can be kept sufficiently small to avoid distorting the desired signal. Alternatively, a short calibration interval using a known reference symbol or preamble sequence may be used to measure the offset and update the compensation voltage periodically. Such automatic offset control enhances the robustness of the proposed decoder against phase mismatch and

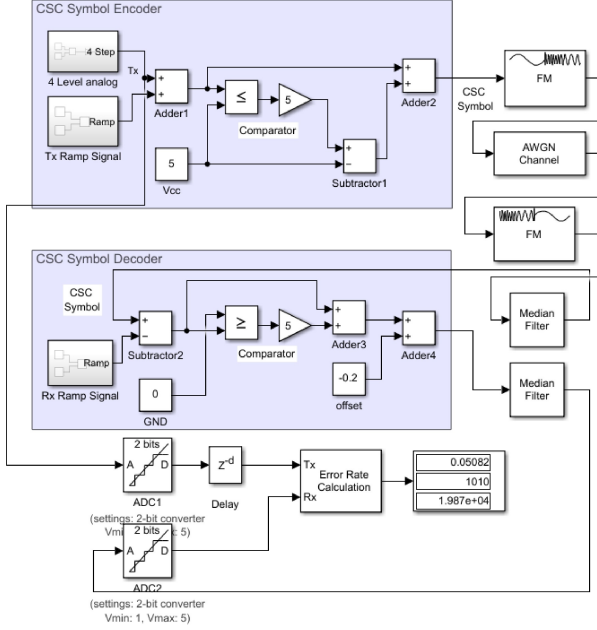


Fig. 14: Simulink block diagram of the proposed CSC symbol encoder/decoder communication system.

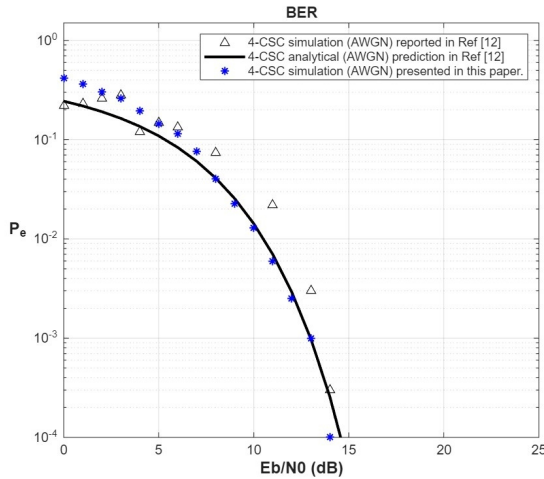


Fig. 15: BER performance comparison over an AWGN channel: simulation results from Ref. [12], theoretical predictions from Ref. [12], and simulation results from the present study.

component variations.

C. Power Consumption Comparison

For a fair comparison focused on CSC processing, the VCO stage in [12] is excluded. Based on the reported discrete implementation, the reference design employs 21 operational amplifiers and three LM13700 OTAs. Using typical datasheet values under a ± 6 V supply, the total power consumption of [12] is estimated at approximately 590 mW.

In contrast, the proposed implementation uses only ten LF351 operational amplifiers, yielding an estimated

power consumption of approximately 216 mW under the same supply conditions—a reduction of about 63% in static power. This improvement is primarily attributed to eliminating OTA-based multiplication and reducing the number of analog building blocks. All values are first-order estimates based on typical device parameters.

D. Thermal Stability of the Proposed Ramp Generator

The thermal stability of the proposed analog ramp generator is governed primarily by the temperature coefficients of the passive components in the RC network. The temperature-dependent variations of resistance and capacitance can be modelled as:

$$R(T) = R_0[1 + \alpha_R(T - T_0)] \quad (26)$$

$$C(T) = C_0[1 + \alpha_C(T - T_0)] \quad (27)$$

where R_0 and C_0 denote the nominal values at the reference temperature T_0 , while α_R and α_C represent the temperature coefficient of resistance and the temperature coefficient of capacitance, respectively.

For the proposed linear ramp generator, where the capacitor is charged by a constant current source defined as $I = V_{ref}/R$, the ramp slope is given by:

$$S(T) = \frac{dV}{dt} = \frac{V_{ref}}{R(T)C(T)} \quad (28)$$

Substituting the temperature-dependent expressions yields:

$$S(T) = \frac{V_{ref}}{R_0 C_0 [1 + \alpha_R \Delta T][1 + \alpha_C \Delta T]} \quad (29)$$

For small temperature coefficients ($\alpha_R, \alpha_C \ll 1$), the first-order approximation gives:

$$S(T) \approx S_0[1 - (\alpha_R + \alpha_C)\Delta T], \text{ where } S_0 = \frac{V_{ref}}{R_0 C_0} \quad (30)$$

Thus, the relative slope variation can be expressed as:

$$\frac{\Delta S}{S_0} \approx -(\alpha_R + \alpha_C)\Delta T \quad (31)$$

This indicates that an increase in temperature reduces the ramp slope proportionally to the sum of the temperature coefficients of the resistor and capacitor.

The ramp delay, defined as the time required for the ramp signal to reach a threshold voltage V_{th} , is given by:

$$t_d = \frac{R(T)C(T)V_{th}}{V_{ref}} \quad (32)$$

Accordingly, the relative delay variation becomes:

$$\frac{\Delta t_d}{t_{d0}} \approx (\alpha_R + \alpha_C)\Delta T \quad (33)$$

The timing shift Δt caused by thermal-induced ramp slope variation directly translates into symbol index

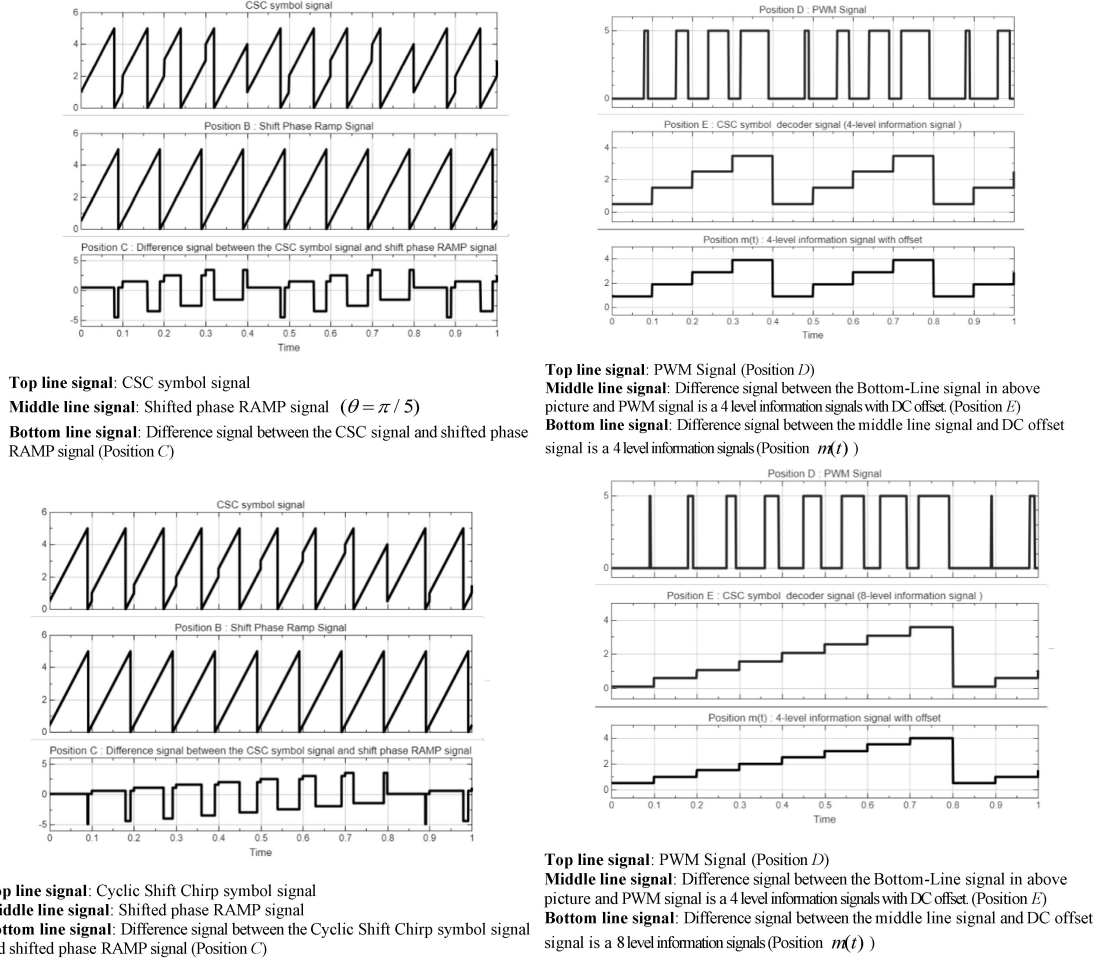


Fig. 16: Simulation results of Cyclic Shift Chirp symbol decoder circuit affected by phase shift.

misalignment in the CSC symbol decoder. Since one symbol step corresponds to a time resolution of $1/BW$, a timing deviation Δt produces a symbol index error of:

$$\Delta k = BW \cdot \Delta t \quad (34)$$

When $|\Delta t| > \frac{1}{2 \cdot BW}$, symbol decision errors occur. Consequently, temperature-dependent RC drift may degrade orthogonality between chirps, effectively reducing detection SNR and increasing BER.

This delay shift directly impacts symbol timing detection in the proposed CSC symbol decoder. Therefore, selecting components with low TCR and TCC values (e.g., metal film resistors and C0G/NP0 capacitors) is essential to minimize thermally induced ramp slope distortion and ensure reliable symbol timing alignment in the proposed analog decoder.

6. DISCUSSION AND LIMITATION

The proposed CSC symbol encoder/decoder architecture reduces hardware complexity by eliminating analog multipliers while maintaining reliable BER performance over an AWGN channel. Compared with [12], which still involves multiplication in the coherent detection process, the proposed formulation relies only on basic

analog building blocks such as adders, subtractors, and comparators. This simplification makes the architecture more suitable for low-cost and power-efficient analog implementations.

Nevertheless, several practical issues remain. The receiver requires accurate RAMP synchronization between the transmitter and receiver; phase mismatch introduces a DC offset that may require calibration. Moreover, the analysis assumes ideal analog components. In practical implementations, non-idealities such as limited op-amp bandwidth, comparator delay, noise, and ramp nonlinearity may degrade performance.

The BER results reported here are based on an AWGN channel. Performance under more realistic wireless impairments, including fading and frequency offset, remains for future investigation. In addition, operation at high spreading factors may impose stricter requirements on timing resolution and comparator speed, which will be examined in future hardware validation.

7. CONCLUSION

This research presents simplified circuitry for Cyclic Shift Chirp symbol signal encoding and decoding using basic analog circuits including RAMP generators, D-to-A

converters, adders, comparators, and subtractors. Both computer simulation and experimental results showed good agreement, confirming the validity of the proposed approach. BER simulations over an AWGN channel further demonstrated that the proposed technique achieves communication performance comparable to the reference method in [12].

The proposed circuit's use of basic analog components enables easy circuit construction and electronic parameter adjustment. Bandwidth adjustment can be achieved through Cyclic Shift Chirp signal amplitude modification, while Spreading Factor adjustment is possible through RAMP signal period adjustment. Additionally, the proposed circuit demonstrates good immunity to receiver-side signal phase shifts, with waveform preservation and only DC offset effects.

Overall, the multiplier-free structure provides a low-complexity and power-efficient alternative suitable for practical analog CSC symbol signal encoder/decoder implementations. Future work will include extended channel evaluations and hardware optimization.

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REFERENCES

- [1] K. Chokruay and A. Apavatjrut, "SNR Prediction Based on Environmental Sensing Data: An Approach Using Machine Learning," *ECTI Transactions on Electrical Engineering, Electronics, and Communications*, vol. 23, no. 2, pp. 1-9, Jun. 2025.
- [2] R. Ranjitha, B.C. Mallikarjun and P. Shivakumar, "Wireless Sensor Network Technologies in Precision Agriculture-A Survey," in *2023 Global Conference on Information Technologies and Communications (GCITC)*, Bangalore, India, 2023.
- [3] R. Khanna, S. Kumar, Y. Chanti, P. Malla and S. V. Akram "Role of IoT Technologies for Wildlife," in *2023 3rd International Conference on Advancement in Electronics and Communication Engineering (AECE)*, Ghaziabad, India, 2023, pp. 303-305.
- [4] W. Manatarinat, P. Tantatsanawong, S. Poomritigul, and S. Udomsiri, "eHealth Internet of Things on Low Power Wide Area Network of Hospital," *ECTI Transactions on Electrical Engineering Electronics and Communications*, vol. 21, no. 3, pp. 1-12, Oct. 2023.
- [5] P. Jain and P. Chawla, "A Novel Smart Healthcare System Design for Internet of Health Things," in *2021 International Conference on Innovative Computing Intelligent Communication and Smart Electrical Systems (ICES)*, Chennai, India, 2021, pp. 170-177.
- [6] F. Busacca, S. Mangione, S. Palazzo, F. Restuccia, and I. Tinnirello, "SDR-LoRa, an open-source, full-fledged implementation of LoRa on Software-Defined-Radios: Design and potential exploitation," *Computer Networks*, vol. 241, Mar. 2024.
- [7] J. Tapparel, O. Afisiadis, P. Mayoraz, A. Balatsoukas-Stimming, and A. Burg, "An open-source LoRa physical layer prototype on GNU radio," in *2020 IEEE 21st International Workshop on Signal Processing Advances in Wireless Communications (SPAWC)*, Atlanta, United States, 2020.
- [8] P. Robyns, P. Quax, W. Lamotte, and W. Thenaers, "gr-lora: An efficient LoRa decoder for GNU Radio," Available online: <https://github.com/rpp0/gr-lora> (accessed on 10 June 2025).
- [9] A. Marquet, N. Montavont, and G. Z. Papadopoulos, "Towards an SDR implementation of LoRa: Reverse-engineering, demodulation strategies and assessment over Rayleigh channel," *Computer Communications*, vol. 153, pp. 595-605, Mar. 2020.
- [10] R. Ghanaatian, O. Afisiadis, M. Cotting, and A. Burg, "LoRa Digital Receiver Analysis and Implementation," in *2019 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, Brighton, UK, 2019, pp. 1498-1502.
- [11] A. Sinchai, N. Saelim, C. Pornavalai, P. Wardkein, and P. Tuwanut, "A Practical Circuit of Cyclic Chirp Spread Spectrum Modulation for Long Range Communication," in *2022 37th International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC)*, Phuket, Thailand, 2022, pp. 526-529.
- [12] L. Kirasamuthranon, P. Wardkein, and J. Koseeyaporn, "Coding and Coherent Decoding Techniques for Continuous Single Slope Cyclic Shift Chirp Signal," *Radioengineering*, vol. 32, no. 2, pp. 273-286, Jun. 2023.



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