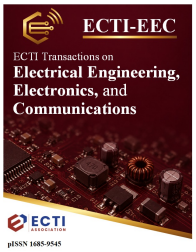
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Energy-Efficient 16-bit RCA and CSLA Design Using MTCMOS with Sleep Transistor Optimization

Ravi Raj[1], Mrinal Ranjan[2] and Utkarsh Raj[3]

Abstract

Leakage power has become a major concern in deep submicron CMOS technologies, particularly in arithmetic circuits where performance and energy efficiency must be balanced. This work presents the transistor-level design and analysis of 16-bit Ripple Carry Adder (RCA) and Carry Select Adder (CSLA) architectures implemented in 90 nm CMOS technology. A variable block CSLA structure is employed to reduce carry propagation delay, and MTCMOS-based power gating is integrated using a high-threshold PMOS header sleep transistor to suppress leakage power. Simulation results obtained using Cadence Virtuoso demonstrate that the CSLA achieves lower propagation delay compared to RCA, while MTCMOS integration significantly reduces standby leakage power from the micro-watt range to the pico-watt range. In addition, a parametric study of sleep transistor sizing is performed to identify the optimal trade-off between leakage reduction and performance degradation. The results indicate that combining architectural optimization with power-gating techniques enables efficient low-power adder design, making the proposed approach suitable for energy-constrained VLSI applications.

Keywords: Ripple Carry Adder (RCA), Carry Select Adder (CSLA), Low Power VLSI design, MTCMOS (Multi-Threshold CMOS), Power Gating.

I. Introduction

The enhanced development of portable and high-performance digital system has heightened the need to develop arithmetic circuits that require less energy. Adders are the basic components of digital signal processors (DSPs), microprocessors and arithmetic logic units (ALUs). Given that addition is the most commonly carried out arithmetic computation in computing systems, maximization of adder architecture is a major factor influencing the overall system performance, power usage and silicon area.

The most common adder design includes the Ripple Carry Adder (RCA), which has simple design and takes less area [1]. Its main weakness, however, is the linear dependence of propagation delay on bit width because to propagate the carry signal each stage has to ripple through it sequentially. This feature renders the RCAs less applicable in situations involving fast applications where timing is an important consideration [2]. To address the limitation of the delay of the RCTA, a number of alternative architectures have been offered. One of such structures is the Carry Select Adder (CSLA) which enhances the performance by precomputing the sum and carry outputs given the two possible values of carry-in (0 and 1) [3]. CSLA minimizes the effective carry propagation delay of RCA since the choice of the correct output is made using multiplexers when the actual carry is made available. This speed gain is however achieved with the disadvantage of increased complexity in hardware and the consumption of more power as there are duplicated adder blocks [4].

As CMOS technology has been continually scaled to deep-submicron scale, leakage power has emerged as a significant design issue to dynamic power. At technology of 90 nm or lower, leakage currents generate significant power consumption in the form of both statical leakage current and total leakage current [5]. Thus, methods of power-reduction where both dynamic and leakage contribution are considered play a critical role in the present-day VLSI design.

MTCMOS (Multi-Threshold CMOS) is a promising circuit level leakage power minimization method. MTCMOS is able to greatly reduce idle leakage by using high-threshold sleep transistors to isolate the logic block in active mode, but disconnect it to the power supply when idle [6]. MTCMOS

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is now integrated with arithmetic architectures (ie., RCA and CSLA) so that a balance is achieved between speed and power consumption [7].

Detailed design and performance comparison of both 16-bit Ripple Carry Adder and 16-bit Carry Select Adder architecture based on 90 nm CMOS technology are shown in this work. Moreover, power-gated versions of these adders are established on the MTCMOS to assess the capability of reducing the leaked powers [8]. The designs are executed at transistor level and studied with respect to average power, leakage power, propagation delay and power-delay product (PDP).

II. RELATED WORKS

Design has been a major concern in the field of VLSI because efficient design of adders affects directly performance of a system, consumption of power, and its area. Ripple Carry Adder (RCA) is considered to be one of the simplest and most popular architectures due to its compact design and simple implementation [9], [10]. Nevertheless, its prominent weakness is that propagation delay increases linearly with bit-width and thereby limits it to use in high-speed applications.

In order to beat this constraint, a number of high-performance adder designs have been designed. One of them, the Carry Select Adder (CSLA), provides a good tradeoff between speed and hardware complexity [4]. The CSLA enhances performance as it performs the calculation of partial results of multiple carry inputs simultaneously and the appropriate output is chosen with multiple multiplexers. Though such a scheme minimises delay, the extra hardware load and power consumption is created by duplicated adder blocks.

The recent developments have been directed toward the optimization of the CSLA architecture in order to enhance efficiency [11]. Proposed square-root CSLA and non-uniform grouping structures have shown to balance delay across various stages to reduce the critical path and be configured as variable block size CSLA structures [7], [12]. Even more to the point hybrid adder designs that use CSLA with other techniques like carry look-ahead logic were investigated too [7], [13]. Also, designs of approximate adders have been explored with a goal of minimizing the amount of energy used but at the expense of accuracy.

The circuit level of optimization of core components like full adders and multiplexers is important to overall performance [14]. The use of transmission-gate-based multiplexers is very common as it offers complete voltage swing and enhanced noise margins which is especially valuable in deep submicron technologies [3].

As the CMOS technology is continually scaled up, leakage power is an increasing factor of concern in the design of digital circuits. Such methods as Multi-threshold CMOS (MTCMOS) have been widely used to reduce the leakage currents [15]. MTCMOS takes advantage of the high-threshold sleep transistors to break the logic block off the power supply even when in the standby mode, and thus in the process, save the power used in the statics considerably [16].

Research has been done on using MTCMOS in arithmetic circuits, showing a significant leakage reduction at reasonable delay overhead [17]. Nevertheless, the majority of current literature is aimed at either optimization of adder architectures or leakage reduction practices on their own [18]. The architectural optimization combined with power gating on the transistor has not been severely explored.

Thus, it is evident that there is a gap requiring an inclusive strategy that incorporates optimized adder schemes coupled with viability leakage minimisation strategies [6]. This drives the current work that aims at the designing and evaluating the RCA and variable block CSLA architectures using MTCMOS to realize a trade-off of delay, power consumption, and energy efficiency [19].

III. RESEARCH GAP AND MOTIVATION

Although much has changed with respect to adder design and low-power techniques, there are still some limitations present in the existing literature.

First, much of the work that has been carried out deals with the optimization of an adders architecture, including modified Carry Select Adders (CSLA), hybrid adders, and square-root CSLA architectures, mostly aimed at minimizing delay [20]. These design methods raise speed, however at the cost of higher power consumption and complexity in the hardware and are not capable of sufficiently dealing with leakage power problems at very deep submicron process technology.

Secondly, there are a number of studies which investigated leakage reduction methods, such as Multi-Threshold CMOS (MTCMOS) that are more mainly at the circuit level. Nevertheless, these works are typically confined to simple blocks of logic or small-scale unit-based arithmetic and frequently fail to take into account optimized adder designs [21].

Although Ripple Carry Adders (RCA), Carry Select Adders (CSLA), and MTCMOS power gating are well-established techniques, most existing studies investigate either architectural optimization or leakage reduction independently. In contrast, this work presents a unified transistor-level implementation of variable-block CSLA integrated with MTCMOS power gating, together with analytical and simulation-based optimization of PMOS sleep transistor sizing under identical operating conditions.

Also, traditional CSLA designs typically propose uniform block partitioning, which is not able to take full advantage of delay balancing possibilities. Whereas some variable block CSLA structures have been suggested, no one has fully explored their implementation, including power-gating like MTCMOS, with a medium-scale design like a 16-bit adder.
Thus, there is a strong necessity of a detailed research which:

- Transistor-level implementation of 16-bit RCA and variable-block CSLA.
- Integration of MTCMOS power gating.
- Development of an analytical sleep transistor sizing model.
- Parametric optimization of PMOS header width.
- Comprehensive comparison using Power, Delay, Leakage and PDP.

The paper fills these gaps by introducing a more elaborate design and comparative analysis of 16-bit RCA architecture and variable block CSLA (2-2-3-4-5) architecture with an integrated MTCMOS of 90 nm CMOS technology with priority

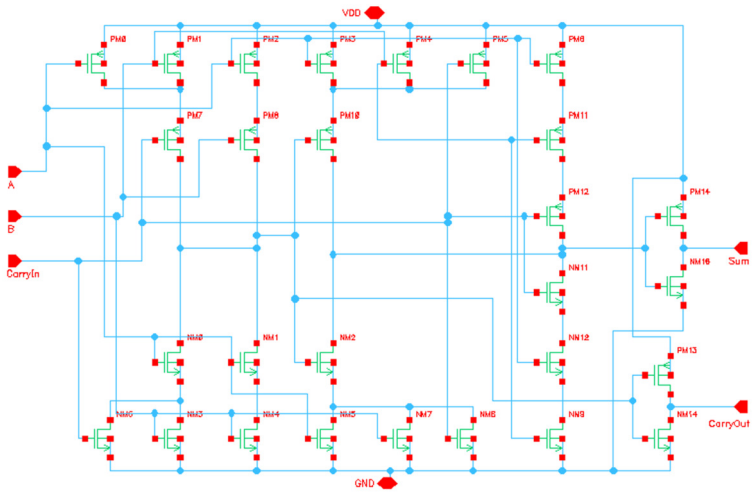


Fig. 1. Schematic of 28-Transistor 1-bit Full Adder.

on the attainment of a balanced trade-off with delay, power consumption, and energy efficiency.

IV. DESIGN METHODOLOGY

In this section, the methodology of implementation at the transistor level of the proposed 16-bit Ripple Carry Adder (RCA) and 16-bit Carry Select Adder (CSLA) architectures will be discussed using the 90 nm CMOS technology. The design process involves circuit-based design, architectural design, MTCMOS design and performance verification design.

A. Fundamental building blocks

The design starts by the implementation of a 1-bit static CMOS full adder shown in Fig. 1, which is the smallest unit of computation. It is followed with the use of 28 transistors. The validated 1-bit cell applies to hierarchical design of 4-bit and 8-bit RCA designs to be validated and analyzed during the intermediate validation and scaling stage.

A 2:1 multiplexer selects one of two input signals (A or B) and directs it to a single output (Y) based on a control signal (S) as shown in Fig. 2. Using transmission gates is a common way to implement this efficiently because it uses fewer transistors and provides better performance than standard static CMOS logic. So, transmitter-gate based 2:1 multiplexer is also designed and tested at transistor level. This type of MUX is applied when constructing CSLA architecture.

B. 16-bit Ripple Carry Adder

The 16-bit RCA is constructed by cascading sixteen 1-bit full adders in Fig. 3. Each stage also has the carry output which is linked to the carry input of the subsequent stage creating a serial carry propagation path.

Even though this architecture has a low area and easy implementation, its worst-case delay is a linear function of bit-width since it is operated by sequential propagation of carry.

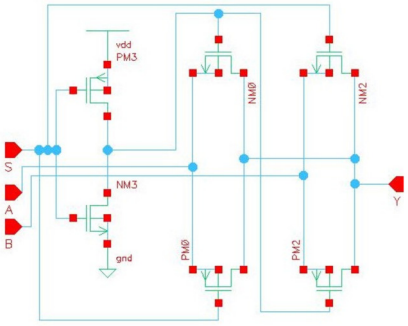


Fig. 2. Schematic of 2:1 Multiplexer using TG.

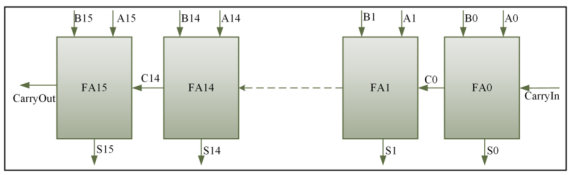


Fig. 3. 16-bit Ripple Carry Adder.

C. 16-bit Carry Select Adder

The CSLA 16 bit is implemented in a variable block (2-2-3-4-5) grouping structure to ensure equal delay distribution among the stages as shown in Fig. 4.

- Block 1 (bits 0–1): Implemented as a 2-bit RCA using the actual carry input (Cin).
- Block 2 (bits 2–3): Contains two 2-bit RCAs operating in parallel, assuming carry-in = 0 and carry-in = 1.
- Block 3 (bits 4–6): Contains two 3-bit RCAs precomputing outputs for both possible carry-in values.
- Block 4 (bits 7–10): Contains two 4-bit RCAs operating in parallel.
- Block 5 (bits 11–15): Contains two 5-bit RCAs precomputing outputs for both carry conditions.

In Blocks 2 to 5, the appropriate sum and carry outputs are chosen by using a 2:1 transmission-gate based multiplexer

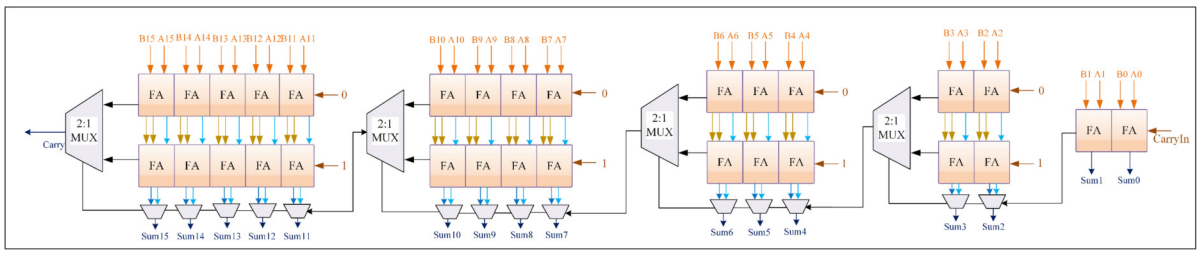


Fig. 4. 16-bit Carry Select Adder.

to choose the appropriate output which depends on the carry produced by the previous block.

The multiplexer select signal is driven by the carry output of the previous stage, enabling dynamic selection of the appropriate precomputed result.

To achieve complete voltage swing, enhanced signal noise and reliability of signal transmission, a transmission-gate construction is embraced at the expense of single pass-transistor-based multiplexers.

The block size used is progressively increasing, to reduce the carry generation delay at the very beginning and minimize the amount of multiplexer stages in the critical path. This type of variable block design has a better delay balancing between the adder stages and faster speed than the homogeneous block CSLA designs.

D. Mathematical Modeling of Sleep Transistor Optimization

The sleep transistor width significantly influences the trade-off between propagation delay and leakage power. A wider sleep transistor reduces the effective ON resistance, improving the virtual supply voltage and reducing propagation delay. However, the larger device width also increases leakage current. Therefore, an optimum width exists that balances these conflicting requirements.

The ON resistance of the sleep transistor can be approximated as

$$R_{ON} \approx \frac{1}{\mu_p C_{ox} \left(\frac{W}{L}\right) (V_{SG} - |V_{TH}|)} \tag{1}$$

where W and L are the sleep-transistor width and channel length, respectively, V_{SG} is the source-to-gate voltage, and V_{TH} is the threshold voltage. This relation shows that increasing transistor width reduces the ON resistance, while a higher threshold voltage reduces the available gate overdrive and consequently increases the effective ON resistance.

The propagation delay of the MTCMOS-based circuit is expressed as

$$t_{pd} = 0.69(R_{logic} + R_{ON})C_L \tag{2}$$

where R_{logic} is the equivalent logic resistance and C_L is the load capacitance.

According to Equation (2), the propagation delay is directly proportional to the equivalent resistance of the power path. Therefore, reducing the ON resistance through a wider sleep transistor lowers the propagation delay. The dependence of the sleep transistor ON resistance on its width and threshold voltage is evident from (1), since both the device width and the overdrive voltage ($V_{SG} - |V_{TH}$) affect the effective resistance of the header device.

$$PDP(W) = P_{avg}(W) \times t_{pd}(W) \tag{3}$$

where $P_{avg}(W)$ and $t_{pd}(W)$ denote the average power and propagation delay corresponding to the sleep transistor width W, respectively.

$$W_{opt} = \arg\min\{PDP(W)\} \tag{4}$$

where W_{opt} is the optimum PMOS sleep transistor width.

However, increasing transistor width also increases leakage current due to the larger conduction channel. Therefore, the optimum sleep transistor width is determined by minimizing the Power–Delay Product (PDP), which balances the trade-off between leakage power and propagation delay. The analytical model provides the theoretical basis for this optimization, while circuit-level simulations identify the optimum width under the specified operating conditions. The simulation results in Section V validate the analytical trend, and a sleep transistor width of 250 μm is identified as the optimum design point.

E. MTCMOS Power Gating Integration in Adder Architectures

MTCMOS is employed in both RCA and CSLA architectures to reduce leakage power by introducing a high-threshold PMOS sleep transistor between the supply and the logic block. During standby mode, the sleep transistor disconnects the circuit from the power supply, effectively suppressing leakage currents, while in active mode, it restores normal operation.

In this work, a high-V_T PMOS header sleep transistor with a single global sleep-control signal is adopted for both RCA and CSLA. A header configuration is selected because it provides supply-side isolation of the logic block with a simple control structure. The single global-control implementation also avoids the additional routing and control overhead associated with multiple distributed sleep devices, while providing a consistent basis for evaluating the effect of sleep transistor width. The choice of a high-V_T device improves standby leakage suppression, although its higher threshold voltage also affects the available gate overdrive and hence the ON resistance and active-mode performance.

1) MTCMOS Integration in RCA: In the RCA architecture, the sleep transistor is connected in a header configuration between VDD and the adder circuit. Due to the simple structure

and single carry propagation path, the impact of MTCMOS on delay and IR drop is relatively moderately illustrated in Fig. 5.

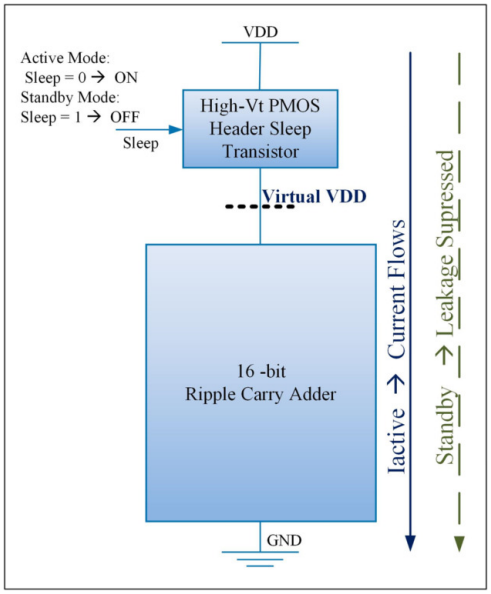


Fig. 5. MTCMOS-based power-gated architecture of the proposed 16-bit Ripple Carry Adder.

2) MTCMOS integration in CSLA: In CSLA architecture, MTCMOS integration affects a more complex structure consisting of multiple RCA blocks and multiplexers. Due to parallel computation and increased switching activity, the CSLA is more sensitive to IR drop and delay variations introduced by the sleep transistor. Therefore, careful sizing of the sleep transistor is required to maintain performance while achieving leakage reduction as shown in Fig. 6

F. Sleep Transistor Design and Control Considerations

Sleep transistor design involves a trade-off among leakage suppression, propagation delay, area overhead, and control complexity. Common power-gating approaches include header-only, footer-only, and combined header–footer configurations. Multiple sleep devices can also be distributed across different logic blocks to reduce local IR drop and control the power-gating behavior of large circuits. The present work adopts a single high-V_T PMOS header with a global sleep-control signal for both the RCA and CSLA. This choice provides a simple supply-side power-gating structure and avoids additional control and routing overhead, while allowing the effect of sleep transistor width to be evaluated under identical conditions.

The sleep-control signal also experiences capacitive loading from the transistor gate, interconnect, and parasitic components. The effective loading can be approximated as:

$$C_{sleep} = C_g + C_{int} + C_{par} \tag{5}$$

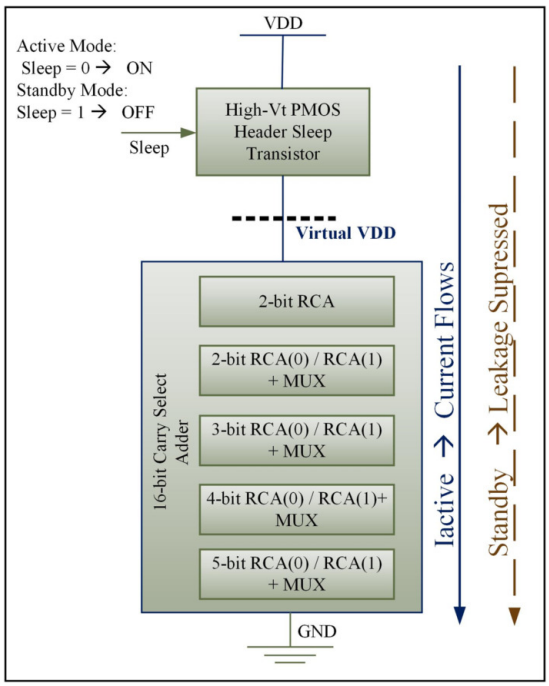


Fig. 6. Power-gated construction on MTCMOS of the proposed 16-bit Carry Select Adder in variable block construction (2-2-3-4-5).

where C_g, C_{int}, and C_{par} denote the sleep-transistor gate, interconnect, and parasitic capacitances, respectively.

$$t_{sleep} \approx 0.69 R_{drv} C_{sleep} \tag{6}$$

where R_{drv} is the effective resistance of the circuit driving the sleep-control signal. Thus, increasing the sleep-transistor width increases the gate capacitance and consequently the capacitive loading of the sleep-control signal. This can increase the control-signal transition time and introduce additional switching overhead.

Consequently, increasing the total sleep-transistor width increases the gate-related loading and may increase the control overhead. The associated control power can be conceptually expressed as:

$$P_{ctrl} = \alpha C_{sleep} V_{DD}^2 f_{sleep} \tag{7}$$

where α is the switching activity factor and f_{sleep} is the sleep-control switching frequency. Therefore, the sleep transistor cannot be sized only to minimize R_{ON}; the resulting leakage, propagation delay, and sleep-control loading must also be considered.

For physical implementation, the selected PMOS header width of 250 μm is realized using 100 parallel fingers, with a width of 2.5 μm per finger. The total effective width is therefore

$$W_{total} = N_f W_f = 100 \times 2.5\mu\text{m} = 250\mu\text{m} \tag{8}$$

where N_f is the number of fingers and W_f is the width of each finger. The multi-finger implementation distributes the large effective device width across parallel fingers and provides a

practical physical realization of the selected sleep transistor described in Fig. 7.

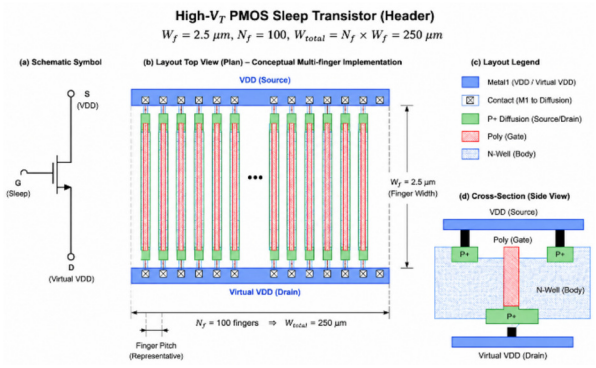


Fig. 7. Conceptual multi-finger implementation of the high-V_T PMOS sleep transistor.

V. RESULTS AND DISCUSSION

The design adder architectures were simulated and modeled with 90 nm CMOS with Cadence Virtuoso. Functionality was checked using transient simulations and performance measures such as propagation delay, average power consumption, leakage power, dynamic power, and power-delays product (PDP) were tested. The supply voltage was set to 1 V and a load capacitance of 5 fF was connected at the nodes of the output to simulate real world situations.

TABLE I
SETUP FOR SIMULATION.

Parameter	Value
Technology Node	90 nm CMOS
Process Corner	TT (Typical – Typical)
Design Tool	Cadence Virtuoso
Simulation Tool	Cadence Spectre
Simulation Type	Transient
Supply Voltage	1.0 V
Input Delay	0 ps
Rise / Fall Time	100 ps
Load Capacitance	5 fF
Temperature	27°C
Input Pattern	Worst-case carry propagation

All measurements are performed under identical simulation conditions to ensure fair comparison.

A. Functional Verification

The adders were designed and transient simulations were conducted to ensure that the design was correct. Pulse voltage sources to the circuits with different combinations of inputs were imposed. The Ripple Carry Adder (RCA) and Carry Select Adder (CSLA) architecture were tested with the simulation waveforms by ensuring that they worked appropriately. Fig. 8and Fig. 9 illustrate the transient response of the basic building blocks, namely 1-bit full adder and 2:1 multiplexer respectively.

In case of the RCA architecture, the carry signal flows in a serial manner starting with the least significant bit to the most significant one. This progressive propagation causes delays to increase with increase in the size of the adder. Conversely, the CSLA architecture arithmetically calculates the sum and carry values of two possible carry inputs (0 and 1) and picks the appropriate output with the help of a multiplexer and minimizes the carry propagation delay.

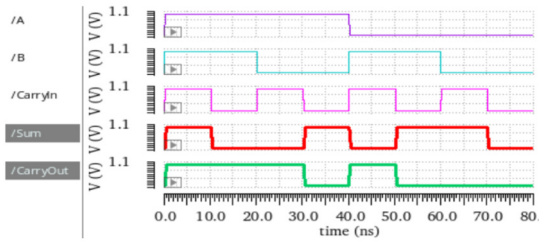


Fig. 8. Transient response of 1-bit FA.

The waveforms transients show that both conventional and MTCMOS-based adders are correct in the values of the output to all the combinations of inputs tested.

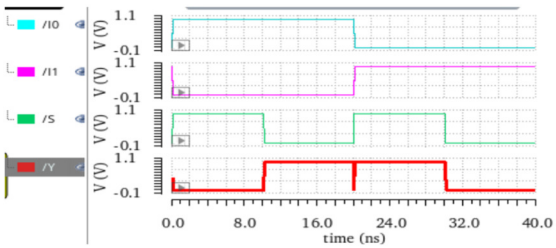


Fig. 9. Transient response of 2:1 MUX.

B. Power Consumption Analysis

To determine the average power consumption, the mean value of the current supply was measured during transient simulation and was multiplied by supply voltage.

The findings indicate that the power rate rises with the expansion of adder bit-width because of the very high quantity of switching transistors. Indicatively, the design power improved by 1.512 μW per average when 16-bit was used compared to 4-bit in the design to the 16-bit implementation of 6.422 μW when used on the RCA.

On the same note, the CSLA architecture has demonstrated a little more power consumption than that of RCA since it had duplicated adder blocks to enable parallelity in carrying out the computation.

TABLE II
POWER CONSUMPTION.

Architecture	Total Power (μW)
1 bit FA	0.709
4-bit RCA	1.512
8-bit RCA	3.003
16-bit RCA	6.422
1-bit CSLA	1.366
2-bit CSLA	3.366
4-bit CSLA	4.333
8-bit CSLA	5.996
16-bit CSLA	7.248

The leakage power is greatly cut down with integration of the MTCMOS technique that adds a high-threshold sleep transistor between the supply voltage and the logic block. In entering the state of standby, the sleep transistor will shut the logic block off of the supply line, thus eliminating leakage current.

C. Leakage and Dynamic Power Analysis

The analysis of leakage power and dynamic power was done individually in order to gain a better insight into the power characteristics of the circuits. The larger the circuit, the greater is the leakage power because of increased number of transistors. In the case of the conventional RCA leakage power doubled with the 4-bit design and 16-bit design to 214.9 nW and 870.5 nW respectively.

TABLE III
LEAKAGE AND DYNAMIC POWER CONSUMPTION.

Architecture	Leakage Power (nW)	Dynamic Power (μW)
4-bit RCA	214.9	1.297
8-bit RCA	429.9	2.573
16-bit RCA	870.5	5.552
4-bit CSLA	633.3	3.6997
8-bit CSLA	1260	4.736
16-bit CSLA	2070	5.178

Through the incorporation of MTCMOS power gating, leakage part of power consumption is able to be drastically lowered when operated in the standby mode without sacrificing the performance of the circuits to a considerable degree.

D. Delay Analysis

The propagation delay was taken as the difference between the 50% transition point of the output signal and 50% transition point of the input signal. The maximum delay was calculated by using input combinations that cause maximum carry propagation.

The data obtained during the simulation indicates the delay increases as the adder size increases in the RCA architecture as a result of propagation of carry signals through a serial manner. As an example, the 4-bit RCA took 296.6 ps to pass through the delay but the 16-bit RCA took 1.43 nanoseconds.

TABLE IV
DELAY ANALYSIS.

Architecture	Delay (ps)
4-bit RCA	297
8-bit RCA	735
16-bit RCA	1435
4-bit CSLA	108
8-bit CSLA	466
16-bit CSLA	872

Conversely, CSLA architecture minimizes delay greatly because part results are calculated in parallel and appropriate output is selected with the help of multiplexers. The efficiency of the carry propagation path is minimized by this parallel functioning.

E. Trade-off Analysis and Optimization of Sleep Transistor Width

To investigate the effect of sleep transistor sizing, a number of width values were tested for the high-threshold PMOS header transistor of the RCA and CSLA structures with 16-bit precision. As shown in Tables V and VI , and Fig. 10(a)) and Fig. 10(b) there is a definite compromise between the two measures. On one hand, narrower transistors provide lower leakage current since the corresponding resistor is higher and the logic block is better isolated; on the other hand, there is more delay as the IR drop of the virtual supply voltage becomes larger. If the sleep transistor becomes wider, then the resistor of the power path will be lower, and therefore, the virtual VDD voltage will be brought closer to the nominal value. This will result in faster operation but somewhat higher leakage power dissipation.

The sleep transistor sizing optimization presented in this work was performed under a fixed simulation environment comprising 90 nm CMOS technology, a 1.0 V supply voltage, 27°C operating temperature, and a 5 fF output load capacitance. These conditions were intentionally maintained constant to enable a fair and consistent comparison among different sleep transistor widths. The selected width of 250 μm represents the optimum design point for the adopted 90 nm CMOS simulation environment. The selection is based on the observed leakage–delay trade-off while maintaining the same supply voltage, temperature, load capacitance, process condition, and input pattern for all width configurations. The width is therefore not claimed as a universal optimum; changes in technology node, threshold-voltage option, supply voltage, load, temperature, or process conditions may shift the optimum point.

TABLE V
LEAKAGE POWER AND PROPAGATION DELAY CHARACTERIZATION OF 16-BIT RIPPLE CARRY ADDER (RCA) WITH VARYING SLEEP TRANSISTOR WIDTHS IN 90NM MTCMOS TECHNOLOGY.

Configuration (Width in μm)	Leakage Power (pW)	Comparison with Baseline (%)	Delay (ps)
Without MTCMOS (Baseline)	8.705×10^5	100	1431
5	2.69	0.00031	2280
10	4.36	0.00050	1940
25	9.590	0.0011	1710
50	17.96	0.00206	1580
100	34.25	0.00353	1495
150	49.48	0.00568	1475
250	**80.1**	**0.00920**	**1455**
500	156.4	0.01796	1442
1000	302.2	0.03540	1437

It can be noted that the behavior of the CSLA structure resembles the one of the RCA architectures. In this case, the influence of the sleep transistor width on the delay/leakage trade-off is even more pronounced, owing to the presence of parallel computation blocks and higher switching activity.

Based on the sizing analysis, a sleep transistor width of 250 μm is selected as the optimal point, where the propagation delay is close to the baseline value while achieving substantial leakage power reduction, ensuring an efficient balance between

TABLE VI
LEAKAGE POWER AND PROPAGATION DELAY CHARACTERIZATION OF 16-BIT CARRY SELECT ADDER (CSLA) WITH VARYING SLEEP TRANSISTOR WIDTHS IN 90NM MTCMOS TECHNOLOGY.

Configuration (Width in μm)	Leakage Power (pW)	Comparison with Baseline (%)	Delay (ps)
Without MTCMOS (Baseline)	2.071 $\times 10^5$	100	872
5	2.74	0.00013	1450
10	4.48	0.00021	1220
25	9.67	0.00046	1050
50	18.2	0.00081	980
100	35	0.00169	920
150	50.88	0.00245	905
250	**82**	**0.00395**	**890**
500	157.2	0.00759	882
1000	301.1	0.01453	875

performance and power. The optimum PMOS sleep transistor width of 250 μm was obtained through circuit-level optimization under the adopted simulation conditions.

The trend observed in Tables V and VI is consistent with Eq. (2) and Eq. (3), where increasing sleep transistor width reduces the effective ON resistance and propagation delay, while excessive width increases leakage power. Therefore, a width of 250 μm provides the best leakage-delay trade-off.

A trade-off is observed between leakage power and propagation delay with varying sleep transistor widths. Smaller widths significantly reduce leakage but degrade delay due to increased resistance, whereas larger widths restore delay performance at the cost of increased leakage. An optimal width region is identified where both leakage and delay are balanced.

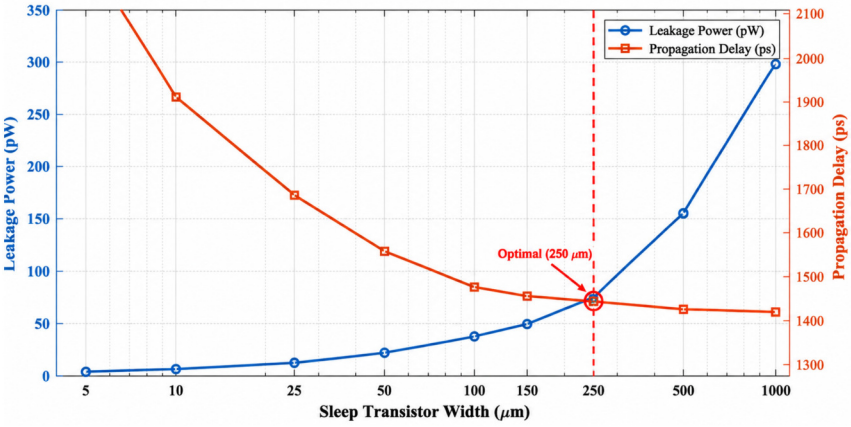
F. Power Delay Product (PDP)

One of these most important key performance metrics is the Power–Delay Product (PDP) which is used to analyze the energy consumption of digital circuits. It is stated to be as follows

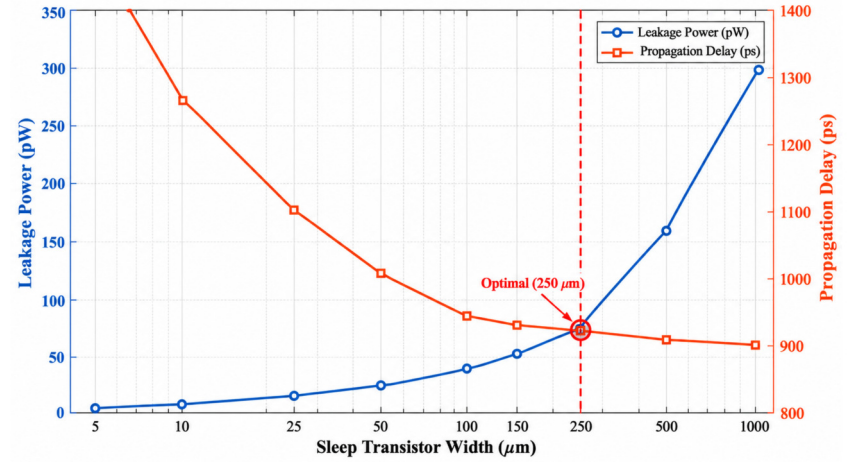
$$PDP = P_{total} \times t_{pd} \tag{9}$$

where P_{avg} is the average power consumption and t_{pd} is the propagation delay.

Tables VII presents the PDP comparison of RCA and CSLA architectures. It is observed that CSLA achieves lower delay but at the cost of higher power consumption, resulting in comparable PDP values for lower bit-widths. However, for higher bit-widths, CSLA demonstrates improved energy efficiency due to reduced propagation delay.



(a)



(b)

Fig. 10. (a) Leakage Power and Propagation Delay Variation with Sleep Transistor Width in RCA and (b) Leakage Power and Propagation Delay Variation with Sleep Transistor Width in CSLA.

TABLE VII
PDP ANALYSIS.

Architecture	Power (μW)	Delay (ps)	PDP (fJ)
4-bit RCA	1.512	297	0.449
8-bit RCA	3.003	735	2.207
16-bit RCA	6.422	1435	9.216
4-bit CSLA	4.333	108	0.468
8-bit CSLA	5.996	466	2.795
16-bit CSLA	7.148	872	6.311

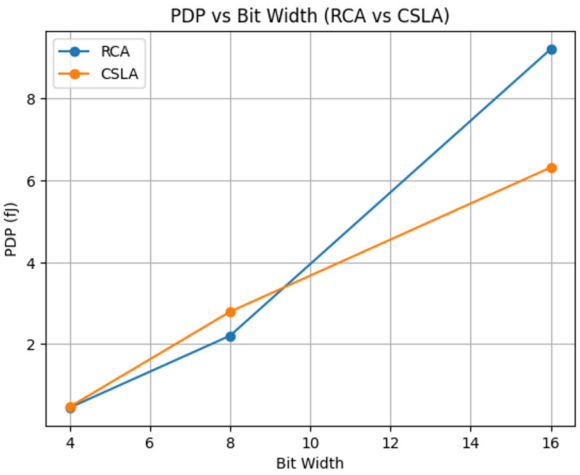


Fig. 11. PDP vs Bit Width (RCA vs CSLA).

Fig. 11 shows the variation of PDP with respect to bit-width for RCA and CSLA architectures. It is observed that for lower bit-widths (4-bit and 8-bit), RCA exhibits lower PDP due to reduced power consumption. However, as bit-width increases, the PDP of RCA increases sharply due to longer carry propagation delay. In contrast, CSLA demonstrates a more gradual increase in PDP owing to its parallel carry computation. A crossover point is observed near 16-bit, beyond which CSLA becomes more energy-efficient than RCA.

G. Performance Comparison

1) Leakage Reduction: The proposed and conventional adders were compared and analyzed in terms of delay, power consumption and PDP. The outcomes show that:

- RCA is the easiest to implement and has minimal area requirements but has a huge propagation delay because of sequential propagation of carries.
- CSLA accelerates speed by minimizing the carry propagation distance by parallel calculation.
- In MTCMOS integration, leakage power is efficiently decreased, and this design is therefore more compatible in low-power applications.

The leakage power is reduced from 2070 nW to 82 pW using MTCMOS during sleep mode operation, achieving a 99.9% reduction compared to active mode. This highlights the strong capability of the proposed design in suppressing standby leakage.

2) Area and Transistor Count Analysis: Layout area and number of transistors were considered for the analysis of the size and complexity of the proposed architectures. The 16-bit RCA utilizes an area of around 5.376 , while the CSLA uses a larger area of 11.376 μm^2 because of the existence of duplicated adder cells and multiplexers.

As for MTCMOS, adding the high-threshold PMOS header transistor of total width 250 μm to it causes increase in area, and the total area for 16-bit RCA is around 20.4 μm^2. and 16-bit CSLA is around 26.5 μm^2. And the total number of transistors goes up to around 448 for RCA and 948 for CSLA.

It can be seen from the analysis above that despite its advantages, MTCMOS involves extra transistor usage and area therefore makes the circuit more complex.

3) Impact on Performance: The addition of the sleep transistor causes extra resistance to be added to the supply line, which influences the operation of the circuit. The IR drop before MTCMOS integration is about 1 mV, which suggests no voltage loss. In contrast, the incorporation of the sleep transistor results in an increase in the IR drop to approximately 10–15 mV, based on the width of the transistor.

Also, the effect of ground bounce is experienced during transition phases. The basic design experiences ground bounce of about 7%. On the other hand, the MTCMOS design experiences ground bounce of about 10–18% because of the changes in virtual ground.

The delay during wake-up from the sleep transistor is seen to vary between 50–120 ps, based on the load and transistor size. The addition of the PMOS header introduces parasitic resistance and capacitance into the power-gating path and sleep-control node, which can affect switching speed and active-mode performance.

4) Sleep Transistor Sizing Optimization: The sleep transistor width critically influences the performance of the MTCMOS-based design. A parametric sweep of the high-V_T PMOS header width was performed, and the corresponding leakage power and propagation delay are summarized in Tables V and VI . For smaller widths, the higher ON resistance produces a larger voltage drop across the sleep transistor, resulting in increased propagation delay. As the width increases, the ON resistance decreases and the virtual supply voltage approaches the nominal supply voltage, thereby reducing the delay. However, further increasing the width also increases leakage power and provides only marginal delay improvement. As observed from the simulation results, a width of 250 μm provides a favorable balance between leakage reduction and delay under the adopted simulation conditions.

5) Design Challenges and Sizing Considerations in MTCMOS: The sizing of MTCMOS circuitry needs to be done meticulously considering the impact of the size of the sleep transistor on the resistance, leakage, delay, area, and sleep-control loading. The smaller the sleep transistor used, the better the isolation effect, though at the cost of increased ON resistance and IR drop that may slow down circuitry performance. Increasing the width of the sleep transistor decreases the ON resistance and improves active mode performance at the expense of higher leakage, area overhead, and sleep-control loading. The sleep transistor must be sized in such a way as to optimize between leakage power, delay, area, and control overhead. The header width of 250 μm for PMOS was chosen after the parametric analysis performed under 90 nm CMOS simulation conditions.

6) Comparison with Carry Look-Ahead Adder (CLA): In addition to RCA and CSLA, the Carry Look-Ahead Adder (CLA) is a well-known high-speed adder architecture that reduces propagation delay by computing carry signals in parallel using generate and propagate logic. Compared to RCA, CLA offers significantly lower delay, especially for large bit-widths, due to its logarithmic carry computation. However, this advantage comes at the cost of increased circuit complexity, higher transistor count, and larger area overhead.

When compared to CSLA, CLA generally achieves better delay performance for higher bit-widths, but requires complex logic implementation and additional wiring resources. In contrast, CSLA provides a simpler structure with moderate speed improvement by precomputing outputs for multiple carry inputs, making it more suitable for designs where a balance between performance and implementation complexity is required.

Furthermore, the integration of MTCMOS in CLA-based designs becomes more challenging due to its complex carry generation network and increased switching activity. The presence of multiple parallel paths in CLA may lead to higher susceptibility to IR drop and noise during power gating transitions. In comparison, the relatively modular structure of CSLA allows more efficient integration of MTCMOS with manageable overhead.

Therefore, while CLA offers superior delay performance, the proposed MTCMOS-based CSLA design provides a more practical trade-off among delay, power, leakage reduction, and implementation complexity, particularly for medium to high bit-width applications.

TABLE VIII
COMPARATIVE ANALYSIS WITH EXISTING RESEARCH (16-BIT CSLA).

Architecture	Tech. Node	Delay (ns)	Total Power	Refe rence
Conventional CSLA	90 nm	5.517	15.42	[22]
BEC-based CSLA	90 nm	5.015	12.85	[22]
CSLA-MUX (FIR)	250 nm	0.820	52.44	[23]
Proposed Design	90 nm	0.890	7.248	This work

7) Comparative Analysis with Existing Research (16-bit CSLA):

VI. CONCLUSION

This work presented the transistor-level design and comparative analysis of 16-bit RCA and variable block CSLA architectures in 90 nm CMOS technology. The CSLA architecture demonstrated improved delay performance due to parallel carry computation, while the RCA offered lower structural complexity and reduced power consumption.

To address leakage power challenges in scaled technologies, MTCMOS-based power gating was integrated into both architectures. The results confirmed that MTCMOS significantly reduces standby leakage power, with only moderate impact on delay due to the introduction of the sleep transistor.

An extensive parametric study of sleep transistor sizing was performed, indicating that width optimization is essential in finding the right balance between minimizing leakage and degrading performance. Results have shown that by proper sizing of the sleep transistor, significant leakage reduction can be achieved without significant degradation in active-mode performance.

In general, CSLA with MTCMOS gives improved results as far as delay vs. leakage is concerned compared to RCA especially for high-bit-width implementations, while RCA is still a good choice for systems emphasizing simplicity and low-power consumption.

From the presented results, we can conclude that the use of architectural optimization together with power gating constitutes an effective way of designing energy-efficient arithmetic blocks. Possible directions for future work include investigating more efficient adder architectures like CLA or prefix adders.

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