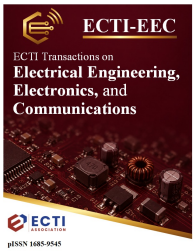
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A Nanopower Biopotential Low-Pass Filter with 450 mVP Input Linear Range Using Self-Cascode Enhanced Source-Coupled Pairs

Napath Thipbanjong, Tatcha Chulajata, Pongsatorn Sedtheetorn, Phattanard Phattanasri, and Prajuab Pawarangkoon

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A Nanopower Biopotential Low-Pass Filter with 450 mV_P Input Linear Range Using Self-Cascode Enhanced Source-Coupled Pairs

Napath Thipbanjong[1], Tatcha Chulajata[2], Pongsatorn Sedtheetorn[3], Phattanard Phattanasri[4] and Prajuab Pawarangkoon[5†]

Abstract

This paper presents an ultra-low-power highly linear second-order continuous-time low-pass filter (LPF) for wearable biopotential acquisition systems. In conventional subthreshold source-coupled-pair (SCP) filters, the input linear range is fundamentally limited to approximately 400 mVP, which restricts the maximum allowable gain of the preceding instrumentation amplifier and consequently, limits system-level power optimization in the digital backend. To overcome this limitation, a self-cascode-enhanced SCP transconductor is proposed. The self-cascode structure increases the output resistance and intrinsic loop gain of the transconductor and extends the input linear range without increasing bias current. The filter is implemented in a 0.18 μm CMOS process and operates at a 1.2 V supply with an 8 nA bias current per branch. Simulation results demonstrate a cutoff frequency of 250 Hz, an input linear range of 450 mVP while maintaining total harmonic distortion (THD) below 1%, and an input-referred noise of 73.78 μVrms. By exceeding the conventional 400 mVP linearity limit without additional power consumption, this work enables higher-gain analog front-ends and facilitates improved energy efficiency in wearable biomedical systems.

Keywords: Analog Front-end (AFE), Biopotential, Continuous-time Filter, Electrocardiogram (ECG), Low-pass Filter (LPF), Subthreshold.

I. Introduction

Biopotential acquisition systems for wearable electrocardiogram (ECG) monitoring typically consist of an analog front-end (AFE) followed by a digital backend. As illustrated in Fig., the signal chain includes an instrumentation amplifier (IA) to amplify low-amplitude physiological signals, a continuous-time low-pass filter (LPF) to suppress out-of-band interference and prevent aliasing, and a driver stage that interfaces with an analog-to-digital converter (ADC) [1].

For ECG biopotential acquisition systems, stringent signal integrity requirements must be satisfied, including a total input-referred noise below 5 μVrms and total harmonic distortion (THD) below 1% at the maximum input signal level ($v_{in,max}$) [2]. To achieve these requirements under strict power constraints, careful noise allocation across the signal chain is essential. Since the noise contributions of circuit blocks following the IA are attenuated by the amplifier gain when referred to the input, their requirements can be proportionally relaxed. Based on this system-level consideration, the allowable input-referred noise of the LPF (IRN_{LPF}) and the combined noise of the driver and ADC (IRN_{DA}) can be

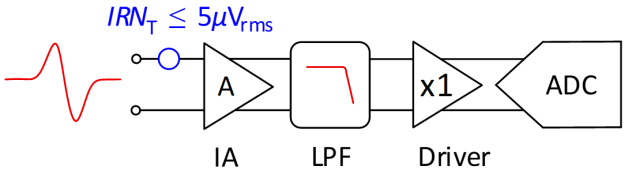


Fig. 1. Biopotential Acquisition System for ECG.

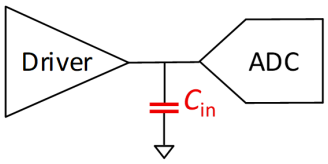


Fig. 2. Driver to drive C_{in} of an ADC.

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TABLE I
SYSTEM NOISE BUDGETS AND FILTER LINEAR RANGE REQUIREMENTS VS. AMPLIFIER GAIN.

Amplifier Gain (V/V)	$v_{in,max}$ (mV_P)	$v_{in,LPF}$ (mV_P)	IRN(μV_{rms})	
			LPF	DA
20	4	80	19.0	57.1
50		200	47.4	142.3
100		400	94.9	284.6
>110		>440	>104.4	>313.1

IRN: Input-Referred Noise, DA: Driver & ADC combined noise

expressed as

$$IRN_{\text{LPF}} = \sqrt{\frac{A^2(IRN_{\text{T}}^2 - IRN_{IA}^2)}{10}}, \quad (1)$$

$$IRN_{\text{DA}} \approx 3 \cdot IRN_{\text{LPF}}, \quad (2)$$

where A is the IA gain, IRN_{T} is the total system input-referred noise, and IRN_{IA} represents the noise contribution of the instrumentation amplifier [3]. These relationships are summarized in Table I, which highlights the trade-off between amplifier gain, allowable noise, and required input signal range.

Increasing the IA gain relaxes the noise requirements of the LPF and ADC, enabling significant power reduction in the digital backend. In wearable systems, the ADC is commonly implemented using a successive approximation register (SAR) architecture, where sampling noise is dominated by the kT/C mechanism. By relaxing the allowable noise through higher IA gain, the required sampling capacitance can be reduced. Since the dynamic power consumption of an SAR ADC is approximately proportional to $P \approx V_{\text{DD}}^2 \cdot C \cdot f_s$, reducing the sampling capacitance directly lowers power consumption.

Moreover, a smaller sampling capacitor reduces the input capacitive load seen by the preceding driver stage, as illustrated in Fig. , enabling further reduction in bias current. These factors collectively lead to significant system-level power savings.

However, increasing the IA gain introduces a critical limitation at the LPF stage. As the signal amplitude scales proportionally with gain, the filter must process a correspondingly larger input swing while maintaining low distortion. As summarized in the Table , an IA gain of 100 V/V requires the LPF to support an input range of at least 400 mV_P, while gains exceeding 110 V/V demand input swings greater than 440 mV_P. Designing a nanopower filter capable of sustaining such large signal swings under subthreshold operation remains a significant challenge.

Numerous continuous-time filter architectures have been proposed and can be broadly categorized into transistorized and explicitly linearized designs [4-14]. Transistorized filters, such as flipped-voltage follower (FVF) biquads [4], source-follower biquads [5], subthreshold buffer-based circuits [6], complementary source-follower filters [7], and band-to-band-tunneling-based filters [8], achieve ultra-low-power operation but typically exhibit limited linear input range. Linearized approaches, including low-voltage OTA-C filters [10], computer-optimized hextuple-diffusor quadruple-differential-pair (HDQDP) architectures [11], folded-cascode OTAs [12], current-sharing vertical source-coupled pairs (VSCP) [3], inverse hyperbolic tangent pre-distortion methods [13], and modular transconductance approaches [14], improve signal handling capability at the expense of increased circuit complexity.

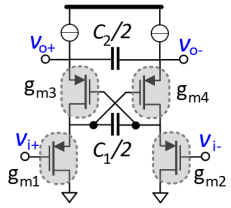


Fig. 3. Source Follower Based Biquadratic cell [19].

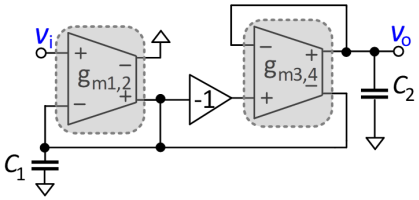


Fig. 4. Equivalent Half-circuit where each transistor represented by a g_m-Cell [17].

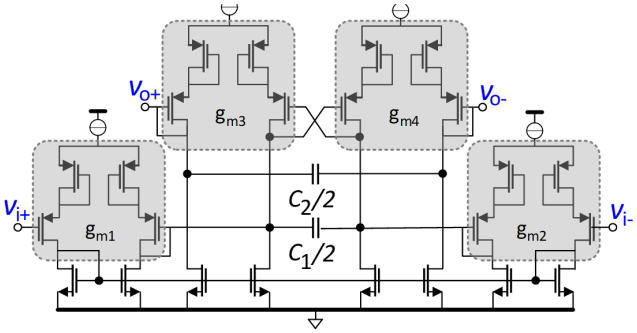


Fig. 5. SCP g_m-C Biquad LPF.

Architectures based on nanopower OTA circuits and current-mode signal processing have also been reported. [15] presented a nano-power OTA-based third-order LPF for ultra-low-energy biomedical signal processing, achieving wide bandwidth tunability and ECG signal conditioning while maintaining extremely low power consumption. Likewise, [16] proposed a 0.3-V current-mode third-order LPF based on a current differencing buffered amplifier (CDBA), demonstrating ultra-low-voltage operation for biomedical applications. These approaches provide attractive solutions for low-voltage and low-power filter design; however, they rely on fundamentally different active-building-block architectures and do not specifically address the large-signal linearity limitation of SCP-based nanopower filters.

Among these, the degenerative source-coupled-pair (SCP) transconductor [17] , shown in Fig. , represents the most

effective baseline, achieving a linear input range close to 400 mVP. However, this value represents the highest input range reported for conventional SCP-based filters to date.

This limitation introduces a practical system-level bottleneck, as it constrains the IA gain to approximately 100 V/V and prevents further reduction in the power consumption of the digital backend. To enable higher-gain AFEs and unlock additional system-level energy savings, the LPF must support input swings beyond 440 mV_P without increasing bias current.

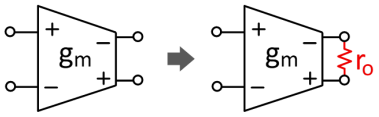


Fig. 6. g_m-cell modelled with r_{ds}.

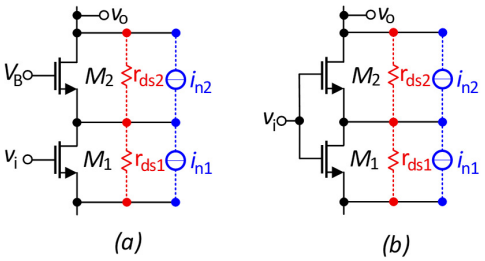


Fig. 7. (a) Regular cascode transistor and (b) Self-cascode transistor.

Although SCP-based LPFs provide excellent power efficiency, their practical input linear range has remained limited to approximately 400 mV_P, which restricts the allowable instrumentation-amplifier gain and prevents further reduction of backend power consumption. Overcoming this linearity limitation without increasing bias current remains an important challenge for wearable biomedical systems.

Recently, [18] proposed a second-order subthreshold g_m-C low-pass filter employing self-cascode composite transistors within an SCP-based transconductor architecture. By incorporating self-cascode devices, the filter achieved a dynamic range of 63.88 dB while consuming only 4.6 nW from a 1.2-V supply. Although the use of self-cascode structures demonstrated improved linearity and dynamic range, the underlying mechanism responsible for the improvement was primarily validated through overall filter-level performance metrics. A detailed investigation of the relationships among transconductance, output resistance, and intrinsic loop gain was not presented for SCP-based filters.

Despite the substantial progress achieved by OTA-based and current-mode biomedical filters, the practical large-signal linearity limitation of SCP-based nanopower filters remains largely unexplored. Existing SCP implementations typically exhibit an input linear range close to 400 mV_P, which effectively restricts the maximum instrumentation-amplifier gain that can be employed in wearable ECG acquisition systems. Consequently, further system-level reduction of ADC and driver power consumption becomes difficult without overcoming this SCP linearity bottleneck.

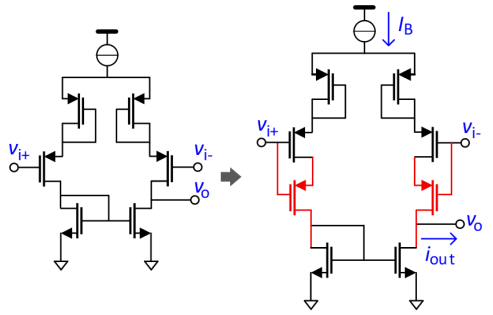


Fig. 8. Self-cascode input pair of the g_m-cell.

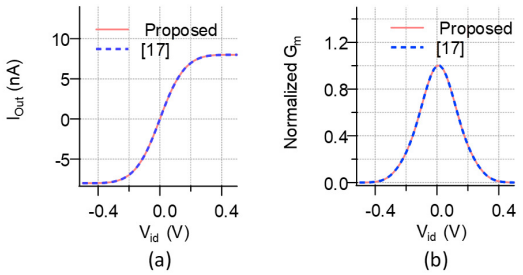


Fig. 9. Small- and large-signal characteristics of the transconductance cell:(a) output current (I_{out}) versus differential input voltage (V_{id}), (b) transconductance (g_m) versus V_{id}.

In this work, a self-cascode enhanced SCP transconductor is proposed to overcome the practical linearity limitation of nanopower SCP filters. By structurally increasing the effective output resistance an intrinsic loop gain without increasing bias current, the proposed architecture extends the achievable large-signal operating range beyond the practical limit reported for conventional SCP implementations. Unlike recent OTA-based and current-mode biomedical filters, the proposed work specifically targets the SCP linearity bottleneck while preserving the ultra-low-power characteristics that make SCP transconductors attractive for wearable ECG acquisition systems. This work extends the practical linear operating range of SCP-based nanopower LPFs beyond the approximately 400-mV_P limit while maintaining the original bias-current budget and preserving the energy efficiency of the SCP architecture.

II. SCP SECOND ORDER FILTER

To realize continuous-time filtering with high linearity, source-follower (SF)-based biquadratic cells, as shown in Fig., have traditionally been employed. The primary advantage of the SF topology lies in its intrinsic local negative feedback, which effectively reduces distortion and improves linearity under large-signal operation. As demonstrated in prior work, SF-based filters can achieve high dynamic range and excellent harmonic performance [19].

However, these structures rely on strong-inversion operation and require relatively large bias currents to maintain sufficient transconductance and accurately implement complex pole locations. As a result, their power consumption is typically on the order of milliwatts, making them unsuitable for energy-constrained wearable ECG acquisition systems.

TABLE II
SIMULATED OUTPUT RESISTANCE AND DC GAIN.

Design	R_{out} (low freq.) (GΩ)	$g_m \cdot R_{out}$	DC gain (mdB)
SCP [17]	19.5	1×10^3	-148.3
Proposed	168	8.7×10^3	-1.63

Simulate at I_B = 8 nA; R_{out} is at 0.1 Hz; both filters were simulated in the same testbench.

To overcome the limitations of high-power SF-based designs, the degenerative source-coupled-pair (SCP) topology has emerged as an energy-efficient solution for nanopower continuous-time filtering [17]. In this approach, the transconductance is realized using the g_m-cell shown in Fig., where the effective transconductance is generated by a source-coupled differential pair with source degeneration. The design of such nanopower transconductors is strongly influenced by energy-efficient analog circuit techniques. Prior work on compact analog building blocks and low-noise biomedical front-end circuits [20-23] highlights the challenges of achieving high linearity and low power under subthreshold operation.

By operating the $\boldsymbol{g_m}$-cell in the subthreshold region and employing techniques such as dynamic element matching, the SCP architecture significantly reduces the required bias current while maintaining acceptable linearity [17]. The resulting second-order SCP $\boldsymbol{g_m}$-C filter, illustrated in Fig., achieves ultra-low power consumption in the nanowatt range while supporting an input linear range of approximately 400 mV_P.

Despite its high energy efficiency, the SCP topology exhibits an inherent limitation in large-signal linearity. For a typical analog front-end employing an IA gain of 100 V/V, the LPF is required to process an input swing of approximately 400 mV_P, which coincides with the maximum linear range achievable by conventional SCP filters. Consequently, the filter operates at the boundary of acceptable distortion performance.

This limitation becomes more critical when higher IA gains are required. As discussed in Section I, increasing the IA gain beyond 110 V/V requires the LPF to handle input swings exceeding 440 mV_P. Under these conditions, conventional SCP filters exhibit significant nonlinear distortion, causing the total harmonic distortion (THD) to exceed the 1% limit [17].

Therefore, while the SCP filter provides an effective solution for ultra-low-power operation, its limited linear input range introduces a fundamental bottleneck at the system level. This restricts the achievable IA gain and, consequently, limits further reduction in the power consumption of the digital backend. Overcoming this limitation requires an architectural enhancement that extends the linear range of the SCP transconductor without increasing bias current.

Fig. 10(b) presents the circuit-theory representation of the proposed SCP filter. The transistor-level implementation shown in Fig. 10(a) can be represented by four transconductance elements and two floating capacitors. This equivalent representation facilitates comparison with previously reported $\boldsymbol{g_m}$-C filter realizations [24], [25] and highlights the correspondence between the SCP implementation and its underlying transconductance-capacitance structure.

III. PROPOSED ENHANCED SCP LPF

A. Transconductor Model and R_{out} Enhancement

The g_m-cell of Fig. 8 is a source-coupled pair with diode degeneration [17]. Due to source degeneration, only half of the applied differential input voltage appears across the SCP input pair. Consequently, the effective differential voltage controlling the weak-inversion current distribution becomes $v_{id}/2$, where $v_{id} = v_{i+} - v_{i-}$, yielding

$$i_{out} = I_B \cdot \tanh\left(\frac{v_{id}}{4nU_T}\right), \tag{3}$$

$$g_m = \frac{I_B}{4nU_T}, \tag{4}$$

where n is the subthreshold slope factor and U_T the thermal voltage. Equation (3) describes the saturating characteristic of Fig. 9(a) and is identical for the baseline [17] and the proposed cell, because the self-cascode does not alter the input-pair transfer characteristic.

Considering the finite output resistance of the transconductor, an output conductance term $g_o = 1/R_{out}$ appears in parallel with the ideal transconductance element. Accordingly,

$$i_{out} = I_B \cdot \tanh\left(\frac{v_{id}}{4nU_T}\right) + v_o g_o. \tag{5}$$

The intrinsic loop gain is given by $LG = g_m \cdot R_{out}$. An increase in the intrinsic loop gain reduces the gain error caused by finite output resistance. This effect is confirmed by the simulation results summarized in Table II .

In the proposed transconductor, each input transistor (M3,4 in Fig. 10) is replaced by a self-cascode structure consisting of an input device and a cascode device (M1,2 in Fig. 10). Under the assumption of weak-inversion operation, the output resistance of the self-cascode branch can be approximated as

$$R_{out} \approx g_{m,cas} \cdot r_{ds,cas} \cdot r_{ds,in}, \tag{6}$$

where $r_{ds} = 1/g_{ds}$. Accordingly, the output resistance is enhanced by the intrinsic gain factor $g_{m,cas} \cdot r_{ds,cas}$ of the cascode device.

From the simulated operating point $g_{m,cas}$ = 127 nS, $g_{ds,cas}$ = 1.4 nS, yielding $g_{m,cas} \cdot r_{ds,cas} = \frac{g_{m,cas}}{g_{ds,cas}}$ = 90.7.

This large intrinsic gain substantially boosts the output resistance of the stacked branch. Furthermore, owing to the low-threshold cascode device, the available input-voltage headroom can be shared between the input and cascode transistors without requiring additional bias circuitry. Consequently, all devices remain in weak inversion while maintaining a cascode-device saturation voltage of approximately 168 mV, which exceeds $4nU_T \approx 104$ mV.

As summarized in Table II, the proposed self-cascode structure increases the transconductor output resistance from 19.5 GΩ to 168 GΩ, corresponding to an improvement of approximately 8.6×. As a result, the static DC gain error of the filter is reduced from 148.3 mdB to 1.63 mdB.

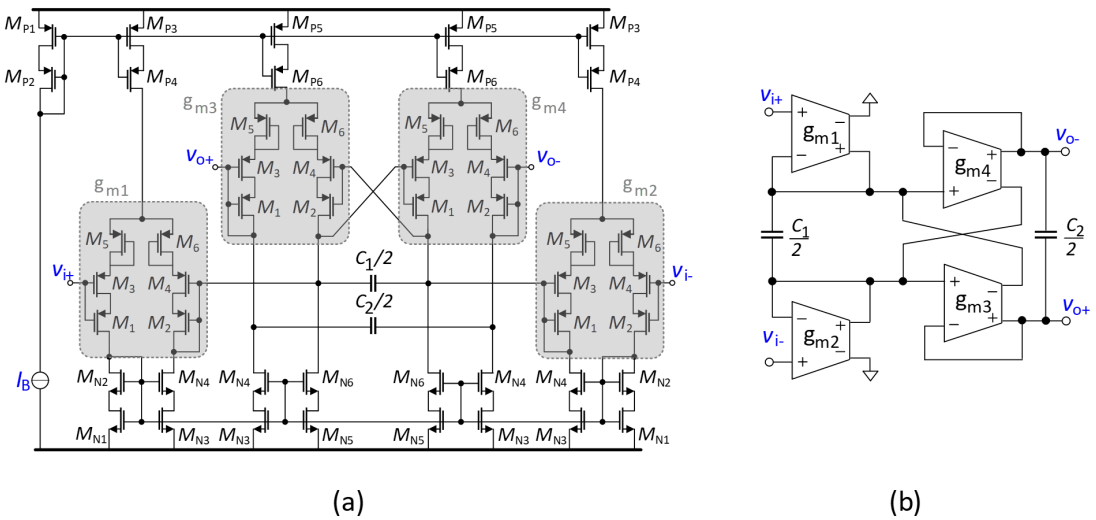


Fig. 10. Proposed SCP filter: (a) transistor-level implementation using self-cascode transconductors, (b) equivalent transconductance-capacitance representation.

B. Self-Cascode g_m-Cell Implementation

Based on the comparison in Fig., the self-cascode configuration is selected to enhance the output resistance of the SCP transconductance cell.

Fig. illustrates the implementation of the self-cascode structure in the g_m-cell. In this configuration, each transistor in the original g_m-cell is replaced by a stacked self-cascode pair. This modification effectively increases the output resistance of the transconductor.

Under nominal operating conditions, all transistors in the self-cascode branch remain in weak-inversion saturation. The input transistor provides the dominant transconductance contribution, whereas the cascode transistor operates primarily as an output-resistance enhancement element. Since both devices carry the same bias current, no additional current branches are introduced, and the power consumption remains unchanged compared with the conventional SCP transconductor.

By increasing the effective output resistance beyond that achievable with a single transistor, the self-cascode structure alleviates the finite r_{ds} limitation shown in Fig. and improves the intrinsic loop gain without additional power consumption.

C. Small- and Large-Signal Characteristics of the Proposed g_m-Cell

Although the stand-alone transconductor exhibits the nonlinear hyperbolic tangent characteristic described by (3), the overall filter demonstrates significantly improved linearity because the transconductors are not operated in an open-loop manner.

As in [17] , each SCP cell is embedded within the source-follower biquad feedback network and therefore processes only the residual differential voltage rather than the full filter input voltage. Consequently, two complementary feedback mechanisms contribute to the linearization of the overall filter response.

The first mechanism is the local negative feedback introduced by the source-degeneration structure within each SCP transconductor. This feedback reduces the effective differential input voltage applied to the weak-inversion input pair and mitigates the nonlinear current redistribution associated with the tanh characteristic.

The second mechanism is the global negative feedback established by the SCP filter architecture. In closed-loop operation, each transconductor processes only the residual differential voltage, $v_{\mathrm{id}} = v_{\mathrm{i}} v_{\mathrm{o}}$, rather than the full filter input signal. Consequently, the actual voltage swing across the nonlinear transconductor is significantly smaller than the externally applied input signal. For a filter input of 450 mV$_p$, transient simulations indicate that the residual differential voltage is approximately 145 mV$_p$ for $g_{\mathrm{m1,2}}$ and 95 mV$_p$ for $g_{\mathrm{m3,4}}$, which are substantially lower than the applied input amplitude.

The proposed self-cascode implementation further enhances this feedback action. As demonstrated in Fig. 10, the self-cascode structure substantially increases the output resistance while preserving nearly the same transconductance characteristic shown in Fig. 9(b). Consequently, the intrinsic gain of the transconductor, $LG = g_{\mathrm{m}} \cdot R_{\mathrm{out}}$, is significantly increased. The resulting higher loop gain reduces the residual differential voltage across the g_m-cell and suppresses the influence of the nonlinear tanh characteristic on the overall filter response.

Therefore, the observed linearity improvement does not arise from a modification of the intrinsic voltage-to-current conversion characteristic of the weak-inversion transconductor. Instead, it originates from the combined action of local source-degeneration feedback, global SCP feedback, and the increased intrinsic gain provided by the self-cascode structure. As a result, the onset of harmonic distortion is delayed, allowing the proposed filter to accommodate a larger input signal while maintaining the same THD criterion.

TABLE III
TRANSISTOR DIMENSIONS AND g_m/I_D VALUES OF THE PROPOSED SELF-CASCODE SCP TRANSCONDUCTOR.

Devices	W/L (μm/μm)	g_m/I_D(V$-$1)
M1, M2	2.5/10	31.72
M3, M4	2/8	27.96
M5, M6	0.4/9	29.41
MP1, MP3, MP5	1/8	28.86
MP2, MP4, MP6	15/0.5	25.46
MN1, MN3, MN5	1/8	22.74
MN2, MN4, MN6	1/8	29.46

D. Output-Resistance Verification

The low-frequency output resistance of the complete g_m-cell, including the current mirror, was extracted with a small-signal ac analysis at the output node, with the inputs held at their dc values in the filter. As listed in Table 2, the self-cascode raises R_{out} from 19.5 GΩ to 168 GΩ (8.6×), and the intrinsic loop gain $G_{\text{m}} \cdot R_{\text{out}}$ from about 1.0×10^3 to 8.7×10^3. The gain increase of the stacked branch alone is about $g_{\text{m,cas}} \cdot r_{\text{ds,cas}} \approx 90.7$ by (6), which is larger than the measured $8.6\times$, because the cell's R_{out} is further limited by other paths in parallel, such as the current mirror. Consistent with the higher loop gain, the static dc gain error of the complete biquad decreases from 148.3 mdB to 1.63 mdB (Table II).

E. Proposed SCP Filter Architecture

The complete second-order filter is shown in Fig. 10(a). All $\boldsymbol{g_m}$-cells of the SCP filter [17] are replaced by the self-cascode cells of Fig. 8. Since the intrinsic voltage-to-current conversion characteristic remains essentially unchanged, the overall filter topology and transfer function are preserved.

The primary effect of self-cascode implementation is the enhancement of the transconductor output resistance and, consequently, the intrinsic loop gain. As summarized in Table II, the low-frequency output resistance increases from 19.5 GΩ to 168 GΩ, while the intrinsic loop gain increases from approximately 1.0×10^3 to 8.7×10^3. The higher loop gain reduces the gain error associated with finite output resistance and improves large-signal operation without increasing bias current.

TABLE IV
VOLTAGE-HEADROOM VERIFICATION ACROSS PROCESS, VOLTAGE, AND TEMPERATURE CORNERS.

Corner	V_{DD}	Temp	Min. V_{DS}
SS	1.08 V	60 °C	133.2 mV
TT	1.20 V	27 °C	120.6 mV
FF	1.32 V	0 °C	111.4 mV

TABLE V
ESTIMATED SILICON-AREA COMPARISON BETWEEN THE BASELINE SCP FILTER AND THE PROPOSED SELF-CASCODE SCP FILTER.

Parameter	SCP [17]	Proposed
Transistor Count	32	48
Active Area (μm2)	512	768
Capacitor Area (μm2)	5647	5647
Total Area (μm2)	6159	6415
Total Area Increase (%)	-	4.16

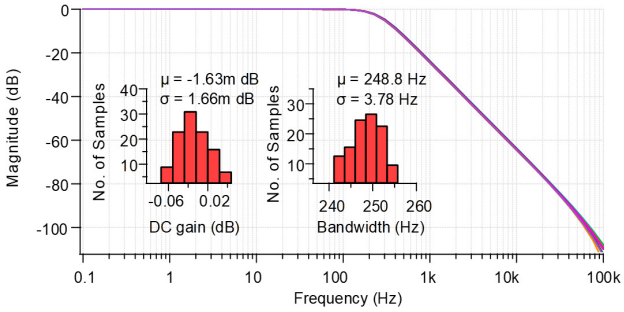


Fig. 11. Frequency response simulation result and statistical information for bandwidth and dc gain.

As discussed in Section 3.c, the increased loop gain reduces the residual differential voltage across the nonlinear transconductors and suppresses the influence of the intrinsic tanh characteristic on the overall filter response. Consequently, the proposed architecture extends the achievable input linear range while preserving the ultra-low-power operation of the original SCP filter.

The resulting filter supports input amplitudes up to 450 mV_{P} while maintaining THD below 1%, exceeding the approximately 400 mV_{P} limit reported for the conventional SCP implementation [17], without additional bias circuitry or power consumption.

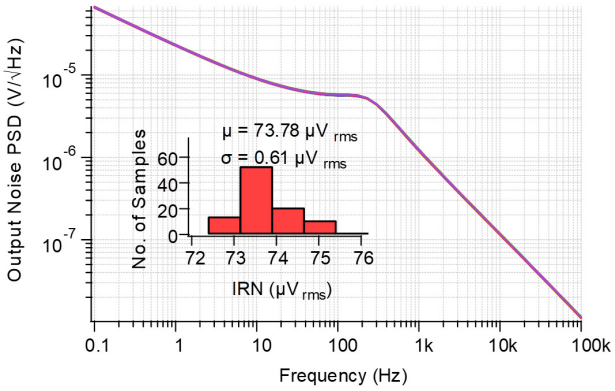


Fig. 12. Output noise spectral density simulation result and statistical information for IRN.

F. Design Consideration

The implementation of the proposed self-cascode SCP filter requires balancing voltage headroom, power consumption, and noise performance under subthreshold operating conditions.

As illustrated in the complete circuit schematic in Fig. 10, the vertically stacked nature of the self-cascode architecture requires careful analysis of the voltage headroom. The minimum supply voltage ($V_{\text{DD,min}}$) required to ensure that all transistors remain in the subthreshold region is determined by the voltage drops across the stacked devices.

$$V_{\text{DD,min}} = 4V_{\text{DS,min}} + 2V_{\text{SG}}, \tag{7}$$

where $V_{DS,min}$ represents the minimum drain-source voltage required to maintain forward-active operation in weak inversion for the tail current sources ($M_{P1\text{-}4}$&$M_{N1\text{-}6}$), and V_{SG} is the source-to-gate voltage of the primary input and source degeneration (M_{1-6}),

In the utilized 0.18 μm standard CMOS process, the nominal threshold voltage (V_{TH}) for these devices is approximately 0.4 V. Because the filter operates entirely in the weak-inversion region, the drain current approaches its saturation value when the drain-to-source voltage exceeds several thermal voltages. A commonly used practical criterion is $V_{DS,SAT} \approx 4U_T$, where U_T is the thermal voltage [26] ($\approx$ 26 mV at room temperature). Consequently, the total required voltage drop across the stack is well below 1 V ($\sim$0.9 V). Therefore, utilizing a standard supply voltage of V_{DD} = 1.2 V provides more than enough headroom to maintain robust operation.

To further verify sufficient voltage headroom, Table 4 shows the simulations performed across process, voltage, and temperature corners. In all the conditions investigated, each transistor remained in weak-inversion saturation and maintained the required drain-to-source voltage. These results confirm that the stacked self-cascode structure can operate reliably from a 1.2-V supply.

The minimum drain-to-source voltage of all devices remained greater than the required weak-inversion saturation voltage under all investigated PVT corners. Therefore, both transistors in each self-cascode branch remain in forward-active weak-inversion operation, validating the assumptions used in the output-resistance analysis in Section 3.a.

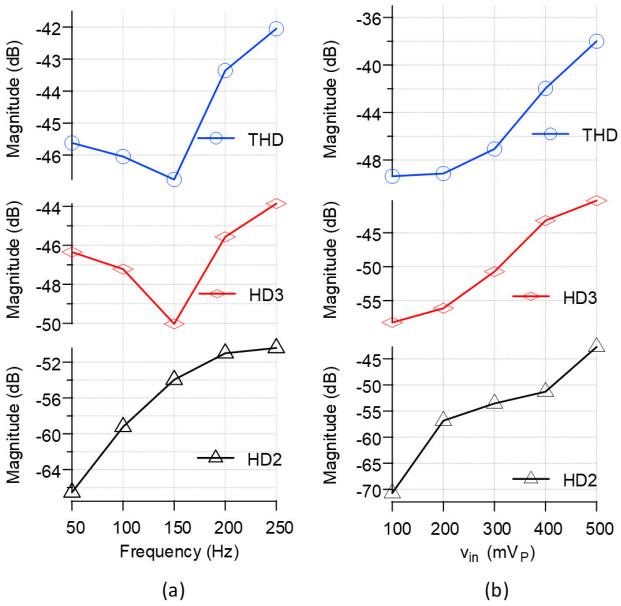


Fig. 13. Monte Carlo distortion results versus (a) input frequency at 450 mV$_P$, and (b) input amplitude at 150 Hz.

To strictly adhere to the nanowatt power constraints of wearable applications while satisfying the clinical noise limits, the core bias current for each transconductor branch is set to a minimal 8 nA. Operating at this ultra-low bias current directly influences the sizing of the passive components required to set the filter's bandwidth and establish the noise floor. In a subthreshold continuous-time g_m-C filter, the noise is fundamentally bound by the physical size of the integrating capacitors. Following established noise analysis for this topology [17], the total output noise power (v_n^2) can be expressed as

$$v_n^2 = \frac{11nkT}{C_1} + \frac{2nkT}{C_2}, \tag{8}$$

where k is the Boltzmann constant, T is the absolute temperature, n is the ideality factor, and C_1 and C_2 are the filter's integrating capacitors. This mathematical relationship highlights a strict physical trade-off between silicon area and thermal noise. The filter must be sized to achieve a specific target cutoff frequency of 250 Hz, which is standard for capturing the full diagnostic bandwidth of an ECG signal. To accurately set this 250 Hz bandwidth while utilizing the 8 nA transconductance, the integrating capacitors are sized as $0.5C_1$ = 11.3 pF and $0.5C_2$ = 5.65 pF. Substituting these specific capacitor values back into the noise equation verifies that the architecture successfully suppresses thermal fluctuations.

These specific values represent the optimal design point; they are small enough to ensure a compact layout footprint, yet sufficiently large to guarantee that the filter's integrated noise remains well within the allocated backend budget required to achieve the stringent 5 μVrms total system noise target.

Table III summarizes the transistor dimensions and extracted g_m/I_D values of the proposed self-cascode SCP transconductor. All devices exhibit g_m/I_D values ranging from approximately 22 to 32 V-1, which is consistent with operation in the weak-inversion region. According to the weak-inversion MOS current model, $g_m/I_D = 1/(nU_T)$, yielding values typically between 25 and 32 V-1 at room temperature depending on the subthreshold slope factor n [26]. The extracted values therefore confirm that the transistors operate in weak inversion under the nominal 8-nA branch current.

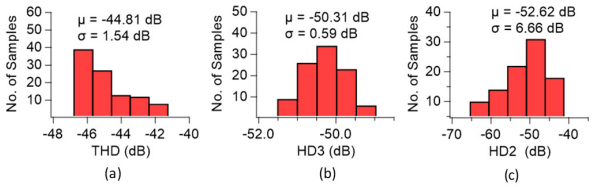


Fig. 14. statistical information for distortion with input voltage of 315 mV$_P$ for (a) THD, (b) HD3 and (c) HD2.

The 8-nA branch current employed in this work can be generated using conventional weak-inversion CMOS bias circuits. Ultra-low-power CMOS reference circuits operating with currents from the picoampere range up to several nanoamperes have been widely reported in the literature. In particular, weak-inversion self-cascode and two-transistor CMOS reference architectures can generate stable ultra-low currents while consuming negligible power overhead. Therefore, the required 8-nA bias current is practical for implementation in low-power biomedical systems.

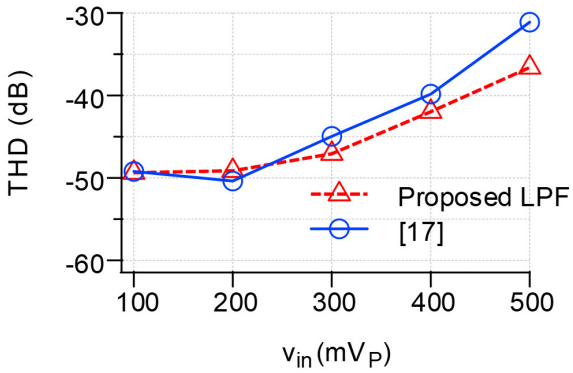


Fig. 15. THD comparison of the baseline and proposed SCP at 150 Hz.

IV. SIMULATION RESULTS

A. Simulation Setup

The proposed second-order SCP g_m-C low-pass filter was designed using Cadence Virtuoso and simulated with the Spectre simulator in a standard TSMC 0.18-µm CMOS process. Device models provided by the process design kit (PDK) were used for all nominal, corner, and Monte Carlo simulations. The filter operates from a 1.2-V supply voltage with an 8-nA bias current per branch.

Monte Carlo (MC) simulations with 100 runs were performed to evaluate the impact of process variations and device mismatch on circuit performance.

B. Frequency Response and Stability

Fig. 11 shows the simulated frequency response, with a cutoff frequency of about 250 Hz and near-unity passband gain. Monte Carlo runs give a mean bandwidth of 248.8 Hz (σ = 3.78 Hz), indicating stable frequency characteristics under mismatch.

C. Noise Performance

The output noise spectral density and its statistical distribution are shown in Fig. 12. The integrated input-referred noise (IRN) across 100 MC runs yields a mean value of 73.78 μV_{rms} with a standard deviation of 0.61 μV_{rms}.

This result is consistent with the theoretical prediction in (8), where the noise is primarily determined by the integrating capacitors. The measured IRN remains below the relaxed noise budget of 104.4 μV_{rms} derived in Section 1 for a 110 V/V AFE.

Furthermore, the results confirm that the introduction of the self-cascode structure does not degrade noise performance. The IRN is set mainly by the integrating capacitors, and the self-cascode adds no measurable noise penalty at the same bias current.

D. Linearity Performance

The linearity of the proposed filter is evaluated using total harmonic distortion (THD), along with the second- and third-order harmonic components (HD2 and HD3).

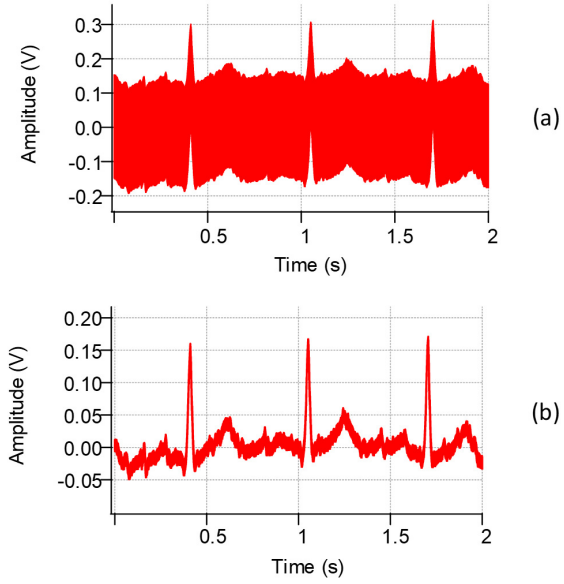


Fig. 16. ECG filtering demonstration: (a) input ECG signal corrupted by high-frequency interference, (b) filtered ECG output obtained using the proposed LPF.

Fig. 13(a) shows the distortion behavior as a function of input frequency at a constant input amplitude of 450 mVP. The THD remains below -40 dB (1%) across the entire passband. The dominant distortion component is HD3, while HD2 remains below -50 dB, indicating good pseudo-differential balance.

Fig. 13(b) shows the distortion components as a function of input amplitude at a constant input frequency of 150 Hz. As the input amplitude increases, the distortion gradually rises, as expected from the tanh characteristic of the cells. However, the THD remains below -40 dB until the input amplitude reaches approximately 450 mV_p.

Compared to conventional SCP filters limited to approximately 400 mV_p [17], the proposed design achieves an approximate 12.5% extension in the linear input range.

E. Comparison with Conventional SCP Filter

Fig. 15 compares the simulated THD of the proposed filter with the baseline SCP design [17] at 150 Hz. The conventional SCP filter exceeds the 1% distortion limit at approximately 400 mV_p, whereas the proposed design extends this limit to 450 mV_p without increasing the bias current. This coincides with the higher output resistance and loop gain in Table II .

F. ECG Signal Demonstration

To verify the suitability of the proposed LPF for wearable ECG acquisition systems, an ECG signal contaminated by high-frequency interference was applied to the filter. The resulting waveforms are shown on Fig. 16 .

As illustrated in Fig. 16(a) , the input signal contains significant out-of-band noise components that can degrade signal quality and increase the burden on subsequent processing stages. After filtering, the high-frequency interference is

TABLE VI
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART LPFS.

Parameter	TCSII 2021 [13]	TBCAS 2023 [9]	TCSII 2024 [17]	TVLSI 2025 [3]	Electron. Lett. 2025 [18]	Appl. Sci. 2025 [16]	Sensors 2025 [15]	This Work*
V_{DD} (V)	1	0.5/1.2	1.2	1.2	1.2	0.3	0.5/1.2	**1.2**
Tech (µm)	0.18	0.04	0.18	0.18	0.055	0.18	0.065	**0.18**
Order	2	2	2	3	2	3	3	**2**
f_0 (Hz)	180	260	250	150	100	110	37 - 668	**250**
IRN (μV_{rms})	N/A	46	82.1	43	104	N/A	N/A	**73.7**
Power (nW)	880	126	38.4	16.3	4.6	170	1.75	**40**
v_{in} (mV_P) @HD3 (dB) & f_{in} (Hz)	250 @< −40 & 10	100 @ -40 & 60	270.5 @-50 & 150	110 @-51.6 & 40	N/A	N/A	N/A	**315 @-50 & 150**
DR (dB)	N/A	63.73	67.34	65.15	63.88	57.2	65.3	**69.6**
FoM ($\times 10^{-17}$ W/Hz)	N/A	10.3	1.42	1.11	0.94	98.15	0.026[i]	**0.88**

*Simulation result,
[i]Calculated from the reported OTA power and bandwidth. Direct comparison may not be strictly equivalent to LPF-level FoM values reported elsewhere.

effectively suppressed while the essential ECG morphology is preserved, as shown in Fig. 16(b) .

The filtered signal maintains the clinically relevant P-wave, QRS complex, and T-wave components while significantly attenuating unwanted high-frequency content. These results confirm that the proposed self-cascode SCP filter satisfies the bandwidth and linearity requirements of wearable ECG acquisition systems and can be used as an effective anti-aliasing and signal-conditioning stage in low-power biomedical front-ends.

G. Performance Summary

Table V summarizes the estimated silicon-area overhead of the proposed self-cascode SCP filter. Although the self-cascode implementation increases the transistor count from 32 to 48, the total area increases by only 4.16% (6159 μm^2 to 6415 μm^2). This is because the filter area is dominated by the integrated capacitors, whose area remains unchanged. Therefore, the proposed approach achieves improved linearity with minimal silicon-area overhead.

Table VI summarizes the performance of the proposed second-order SCP g_m–C low-pass filter and compares it with previously reported continuous-time filters for biomedical applications. Key performance metrics, including IRN, power consumption, dynamic range (DR), and input linear range, are considered to evaluate the effectiveness of the proposed architecture.

The proposed design achieves a power consumption of 40 nW, which is comparable to state-of-the-art SCP-based filters such as [17], while remaining significantly lower than many linearized OTA-based implementations that typically require substantially higher power. This indicates that the incorporation of the self-cascode structure does not compromise the intrinsic energy efficiency of the SCP topology.

In terms of noise performance, the filter exhibits an input-referred noise of 73.7 μV_{rms}, which satisfies the relaxed system-level noise requirements for high-gain analog front-ends discussed in Section 1. Although lower noise values have been reported in some prior works, these are generally achieved with increased power consumption or reduced signal swing capability, highlighting the trade-off between noise, power, and linearity.

The proposed filter also achieves a dynamic range of 69.6 dB, which is among the highest reported for nanopower SCP-based LPFs. This demonstrates that the design effectively balances noise performance and large-signal handling capability under stringent power constraints.

To provide a normalized comparison across different designs, the figure of merit (FoM), defined as

$$\text{FoM} = \frac{P}{DR \cdot BW \cdot N}, \tag{9}$$

where P is the power consumption, DR is the dynamic range, BW is the filter bandwidth, and N denotes the filter order.

Using this definition, the proposed filter achieves a FoM of 0.88×10^{-17} W/Hz, indicating an efficient trade-off between power consumption, signal dynamic range, and bandwidth when compared to prior designs.

Compared to conventional SCP-based filters [17], the proposed architecture achieves a 12.5% extension in input linear range without increasing bias current, supply voltage, or filter order, while the cell's output resistance and loop gain increase (Table II).

V. CONCLUSION

A self-cascode enhanced SCP transconductor has been proposed to improve the linearity of nanopower continuous-time g_m-C filters for wearable biopotential acquisition systems. The proposed architecture increases the effective output resistance and intrinsic loop gain of the SCP transconductance cell without additional power consumption, enabling improved large-signal operation under subthreshold biasing.

Designed in a 0.18 μm CMOS process, the resulting second-order LPF achieves a 250 Hz cutoff frequency, 73.78 μV_{rms} input-referred noise, and a 450-mV_P input linear range while consuming only 40 nW from a 1.2 V supply. The proposed filter extends the practical linearity limit of conventional SCP filters by approximately 12.5% while maintaining THD below 1%.

The demonstrated linearity enhancement provides additional headroom for high-gain analog front-ends and supports more energy-efficient biomedical sensing systems. The

proposed self-cascode technique can be readily applied to other nanopower SCP-based analog building blocks requiring improved large-signal performance.

Fig. 14 shows the Monte Carlo distribution of distortion at 315 mVP. As shown in Fig. 14(a) , the mean THD is 44.81 dB (σ = 1.54 dB), so the filter stays below the 1% limit. Fig. 14(b) shows that HD3 is the dominant component, with a mean of 50.31 dB (σ = 0.59 dB). Fig. 14(c) shows that HD2 is lower, with a mean of 52.62 dB (σ = 6.66 dB). Together these results indicate consistent linearity under process variation.

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