Single-Ended Output Class-AB Current Multiplier

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ABSTRACT—

A new current-mode single-ended output four-quadrant analogue multiplier, for analogue signal processing applications, is proposed. The multiplier is designed by based on the use of the class-AB amplifier and the dual output second generation current conveyor. The multiplier performance is demonstrated through PSPICE circuit simulation using 0.25-µm CMOS technology with ±1.5 V power supply voltages. The total harmonic distortion of about 1% for the input signal range of ±10 µA is achieved. The quiescent power consumption is 342 µW and the -3dB bandwidth of the proposed multiplier circuit is 5.8 MHz.

Keywords: *analogue multiplier, current-mode circuit, class-AB amplifier, CMOS square-law circuit, single-ended output multiplier, current conveyor.*

1. INTRODUCTION

It is well accepted that a Class-AB amplifier is a useful basic circuit building blocks in the design of analogue signal processing systems. Usually, as an output stage, it is employ to generate the output current that is much greater than its bias current. In addition, the class-AB amplifiers can find applications in audio amplifiers, motor drivers, input and output stages of operational amplifiers [1] – [5], current conveyers [6] – [8], rectifier/squarer circuit and analogue multipliers [9] – [10]. The multiplier circuit topologies can be implemented in the both of BJT and CMOS technologies. For the bipolar technology, the Gilbert's multiplier which is designed by based on Gilbert's translinear principle is widely used. For CMOS technology, many analogue multipliers have been recently reported, by using square-law and sub-threshold behavior of CMOS transistor in the week inversion [11] – [13]. However, these circuits provide the output in the differential voltages form. Consequently, in order to produce single-ended output voltage that reference to ground, an external differential to single-ended output, such as difference amplifier that designed by using op-amp and resistors, may be used [14]. The multiplier presented in this article also uses the square-law characteristic of the CMOS transistor. However, the proposed circuit structure is based on the modified class-AB amplifier by including the parallel output transistors to apply multiple input current terminals. Therefore, the single-ended output voltage of the multiplier can directly be achieved without the requirement of an external differential to single-end voltage converter.

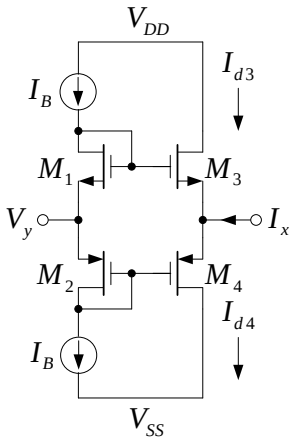
2. CIRCUIT DESCRIPTION

2.1 BASIC OPERATION

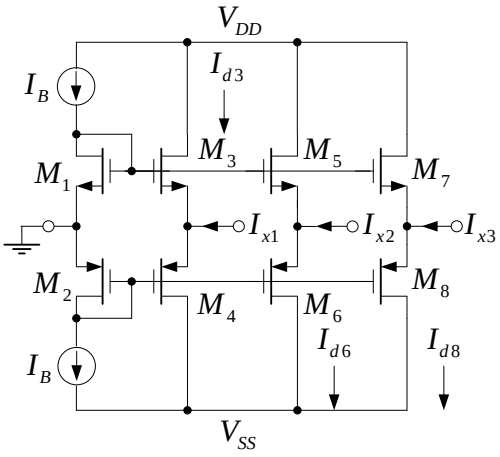
Fig. 1 (a) shows a CMOS class AB circuit configuration formed by the complementary matched pair of NMOS and PMOS transistors where M_1-M_4 connected in such a way that are conducted simultaneously. The current sources I_B provide the bias currents for all transistors to be operated in the saturation region with their individual wells are connected to their sources. The drain current of CMOS transistor is characterized by a square law model as

$$I_d = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{gs} - V_{th}\right)^2 \qquad (1)$$

where $\mu_n C_{ox} W/2L$ is transconductance parameter, μ_n is electron mobility, C_{ox} is oxide capacitance per unit area, W and L are the channel width and length, V_{th} is the threshold voltage of the MOS transistor, respectively.

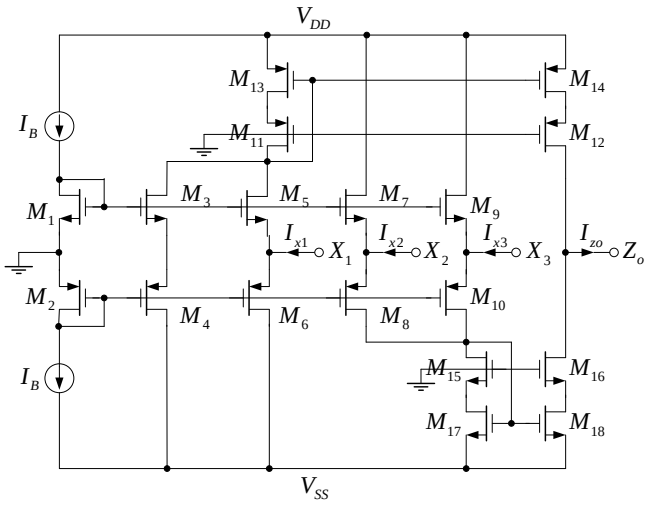


(a) *Class AB amplifier.*

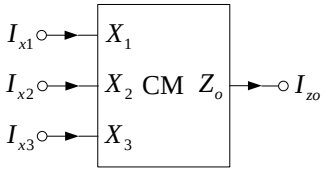


(b) *Multiple input current class AB amplifier.*

Fig. 1. *CMOS class AB amplifier circuits.*



(a) *Multiplier circuit core.*



(b) *Circuit symbol of the multiplier circuit core.*

Fig. 2. *Current multiplier circuit core.*

From Fig.1 (a), if a constant voltage V_y = 0 is connecting to node *Y*, then the loop voltage of the gate-to-source of M_1 - M_4 (V_{gs}) can be expressed as $V_{gs1}+V_{gs2} = V_{gs3}+V_{gs4}$. By applying the input current I_x for $|I_x| \le 4I_B$, the drain currents I_{d3} of the transistors M_3 and I_{d4} of M_4 can be expressed as

$$I_{d3} = \frac{\left(4I_B - I_x\right)^2}{16I_B} \qquad (2)$$

$$I_{d4} = \frac{\left(4I_B + I_x\right)^2}{16I_B} \qquad (3)$$

Fig. 1 (b) shows the basic principle of the proposed multiplier. By considering from Fig. 1 (a), four CMOS transistors M_5 - M_8 are connected to the class AB amplifier. Assuming that all transistors M_1 - M_8 are matched and biased in the saturation region and by applying three input currents I_{x1}, I_{x2}, and I_{x3}, the drain currents I_{d3}, I_{d6}, and I_{d8} of the transistors M_3, M_6 and M_8, can be respectively given by

$$I_{d3} = \frac{\left(4I_B - I_{x1}\right)^2}{16I_B} \tag{4}$$

$$I_{d6} = \frac{\left(4I_B + I_{x2}\right)^2}{16I_B} \tag{5}$$

$$I_{d8} = \frac{\left(4I_B + I_{x3}\right)^2}{16I_B} \tag{6}$$

If the output current I_o is the sum of the drain currents of the transistors M_3, M_6, and M_8. Therefore, the output current I_o in the form of the summing current between I_{d3}, I_{d6}, and I_{d8} can be expressed as

$$I_o = I_{d3} - \left(I_{d6} + I_{d8}\right) \tag{7}$$

By substituting (4), (5), and (6) into (7), and let I_{x1} = (I_1+I_2), I_{x2} = $-I_1$, I_{x3} = $-I_2$, then the output current I_o can be written as

$$I_o = \frac{1}{16I_B}\left\{-\left(4I_B\right)^2 + 2I_1I_2\right\}$$

$$= -I_B + \frac{I_1I_2}{8I_B} \tag{8}$$

Equation (8) shows that the multiplication function of the input currents I_1 and I_2 can be achieved, however, with the dc offset current of ($-I_B$). It should be noted that from the characteristic of the class-AB amplifier as shown in Fig. 1 (a) that the maximum value of the summing input current should be limited to $|I_1+I_2| \le 4I_B$. This means that the maximum value of the input currents $|I_1|$ and $|I_2|$ should be less than $2I_B$.

Fig. 2 shows the proposed multiplier circuit core CM based on the CMOS class AB circuit that is shown in Fig. 1 (b). The transistors M_3-M_4 have been added for generating the dc current I_B in order to compensate the dc offset current ($-I_B$). The unity gain current mirrors M_{11} - M_{14} and M_{15} - M_{18} are employed to sum the drain currents of the transistors M_3, M_5, M_8, and M_{10}. Finally, the output current I_o of the current multiplier circuit core can be rewritten as

$$I_o = \frac{I_1I_2}{8I_B} \tag{9}$$

2.2 FULLY DIFFERENTIAL CURRENT GENERATOR

From the circuit structure of the multiplier circuit core of the Fig. 2, this circuit requires the fully differential input currents $\pm I_1$ or $\pm I_2$. This can be created by using the second generation dual output class-AB current conveyor (CCII) as shown in Fig. 3. From the characteristics of CCII [15], if port Y is connected to ground and by applying the input current I_i to port X, then the fully differential output current can be generated at the ports Z_1 and Z_2 as

$$I_{z1} = +I_i, \text{ and } I_{z2} = -I_i \tag{10}$$

where $|I_i| \le 4I_B$.

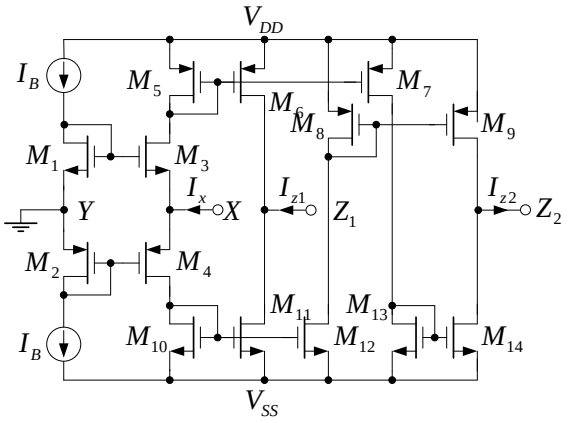


Fig. 3. *CMOS current conveyer (CCII).*

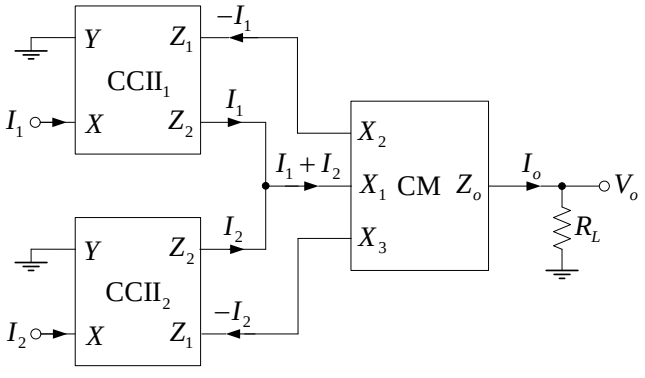


Fig. 4 *CMOS single-end output current multiplier*

2.3 CURRENT MULTIPLIER WITH SINGLE-ENDED OUTPUT

Fig. 4 shows the proposed current-mode single-ended output four-quadrant analogue multiplier. The circuit structure consists of the fully differential current generator $CCII_1$-$CCII_2$ and the current multiplier circuit core CM that are shown in Fig. 2 and Fig. 3, respectively. When the input currents I_1 and I_2 are applied, the fully differential currents $\pm I_1$ and $\pm I_2$ are created. The sum of the input current (I_1+I_2) is fed to the terminal X_1, and the negative currents $(-I_1, -I_2)$ are applied to the terminals X_2 and X_3 of the current multiplier circuit core CM, respectively. Thus, the output current I_o can be achieved as shown in (9) and are in the form of the output voltage V_o with the resistor R_L as

$$V_o = \frac{R_L}{8I_B} I_1 I_2 \tag{11}$$

which is in the form of a complete multiplier function. Then, the proposed circuit functions as a current-mode single-ended output four-quadrant analogue multiplier. It should be noted that the multiplication factor of the multiplier is independent from the design and process parameter of the CMOS transistor, and can be controlled by the bias current I_B and the resistor R_L.

3. SIMULATION RESULTS

The performance of the proposed single-ended output current multiplier as shown in Fig. 4 has been studied by using a 0.25-μm level 3 CMOS technology parameters with the nominal threshold voltages and transconductance parameters approximately of V_{THN} = 0.42 V and $\mu_n C_{ox}$=250 μA/V^2 for NMOS, and V_{THP} = -0.55 V and $\mu_p C_{ox}$= 52 μA/V^2 for PMOS transistors, respectively. In addition, the transistor sizes (in μm) of all NMOS are $(W/L)_n$ = 5/5, and of all PMOS transistors are $(W/L)_p$ = 25/5. The simulation results show that the circuit has a quiescent power consumption of only 342 μW, with a power supply voltages of ±1.5 V and the bias current of I_B = 6 μA. By using the resistor R_L=10 kΩ, the dc characteristic curve is shown in Fig. 5. We can see that the circuit provides a high linearity with a wide input current range. The maximum output voltage is about 21 mV for the input currents of I_1 and I_2 of ±10 µA.

Fig. 6 shows the application of the proposed multiplier as an amplitude modulator. The 10 μA sinusoidal input currents and the frequency are 1 kH_z and 15 kH_z have been applied to I_1 and I_2, respectively. Fig. 7 shows the result when the both input currents have been supplied by the same frequency 5 kH_z with peak amplitude of 10 μA. The frequency of 10 kH_z at the output voltage V_o is obtained. Fig. 8 shows the frequency response of the proposed circuit with the -3 dB bandwidth of 5.8 MHz. To measure the total harmonic distortion, a 10 μA dc current is applied to the input current I_2 and a 1 MH_z sinusoidal signal is applied to I_1. The total harmonic distortion (THD) is approximately 1.09%. The performances of the proposed circuit and the other multipliers are summarized in Table 1.

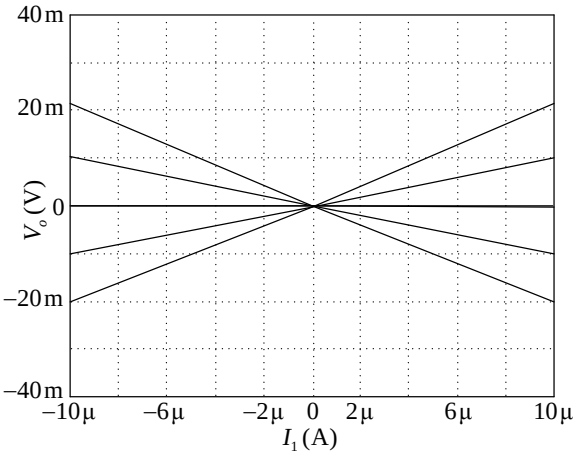


Fig. 5 *Characteristic curve of the proposed multiplier.*

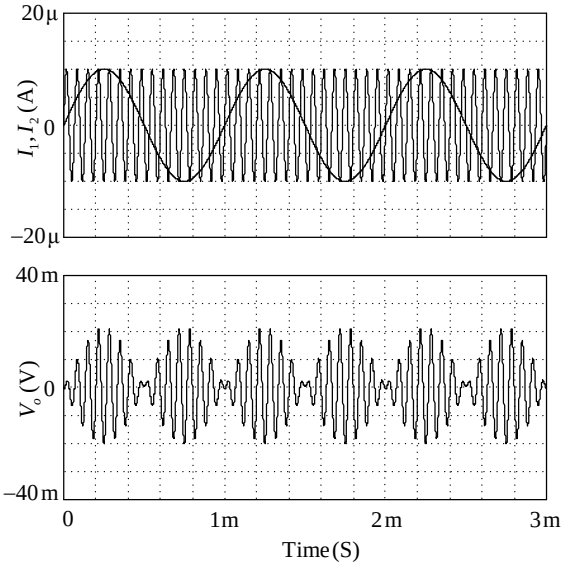


Fig. 6 *Sinusoidal signal amplitude modulation.*

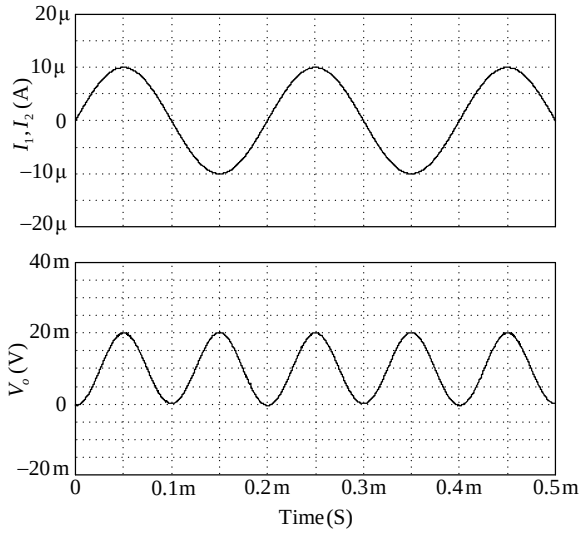


Fig. 7 *Multiplication for two sinusoidal inputs.*

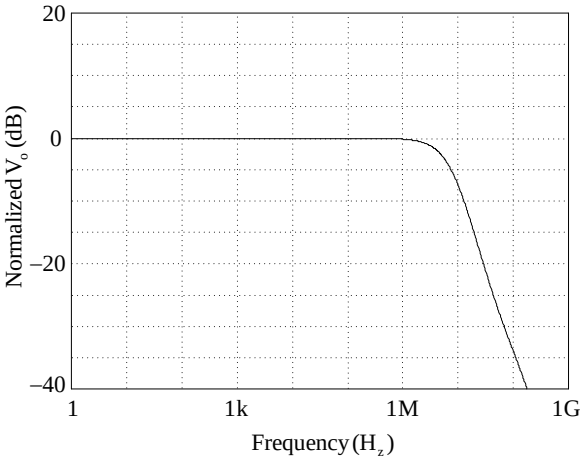


Fig. 8 *Frequency response of the multiplier.*

Table 1 *Performance comparision.*

Parameters	This work	[12]	[13]	[14]
Technology	0.25 μm	0.18μm	0.35 μm	0.5 μm
Supply voltage	±1.5 V	0.8 V	1.5 V	3.3 V
Power consumption	342 μW	0.78 μW	32 μW	-
Input range	±10 μA	25 mV	±0.2 V	±50 μA
Bandwidth	5.8 MH_z	650 kH_z	1.98 GH_z	66 MH_z
THD	1.09 %	1.3%	1.7%	-37 dB

4. CONCLUSION

In this paper, a class AB current-mode single-ended output four-quadrant analogue multiplier has been presented. The multiplier circuit structure is based on the modification of a CMOS class-AB amplifier to function as the current multiplier circuit core. Due to the requirement of the single-ended input to differential output current, a class-AB current conveyer (CCII) is employed. The performances of the proposed multiplier have been demonstrated using PSPICE simulation results. The circuit can provide current multiplication function with about 1.09% total harmonic distortion and with the -3dB bandwidth of 5.8 MHz. In addition, the multiplication function is independent from the design and process parameter of the CMOS transistor.

REFERENCES

[1] M. Loikkanen and J. Kostamovaara, “Four-stage 1.5V class AB power amplifier,” Proceedings of the 12th IEEE Mediterranean Electrotechnical Conference, May 2004.

[2] F. Op't Eynde, P. Ampe, L Verdyen, W. Sansen, "A CMOS large-swing low-distortion class-AB power amplifier", IEEE J. Solid State Circuits, vol. 25, no. 1, pp. 265-273, 1990.

[3] F. Silveira, D. Flandre, "Analysis and design of a family of low-power class AB operational amplifiers", 13th Symposium on Integrated Circuits and Systems Design, pp. 94-98, 2000.

[4] H. Lee, P. Mok, "Active-feedback frequency compensation for low-power multi-stage amplifiers", Proceedings of the IEEE 2002 Custom Integrated Circuits Conference, pp. 325-328, 2002.

[5] R. Castello, G. Nicollini, P. Monguzzi, "A high-linearity 50Ω CMOS differential driver for ISDN applications", IEEE J. Solid State Circuits, vol. 26, no. 12, pp. 1809-1816, 1991.

[6] Subodh Thankachan, Manisha Pattanaik, and S. S. Rajput, “±0.5V BiCMOS class-A and class-AB Current Conveyor structures,” TENCON 2008 - 2008 IEEE Region 10 Conference, Nov. 2008.

[7] A. Sedra, K.C. Smith, "A second-generation current conveyor and its applications", IEEE Transactions on Circuit Theory, vol. 17, pp. 132-134, 1970.

[8] O. Oliaei and P. Loumeau, “A low-input resistance class AB CMOS current-conveyor,” Proceedings of the 39th Midwest Symposium on Circuits and Systems, August 2002.

[9] Boonchai Boonchu and Wanlop Surakampontorn, “A CMOS current-mode squarer/rectifier circuit,” Proceedings of the 2003 International Symposium on Circuits and Systems, May 2003.

[10] Boonchai Boonchu and Wanlop Surakampontorn, “CMOS class-AB voltage-mode multiplier,” IEEE International Symposium on Communications and Information Technology, vol. 2, pp. 1489-1492, Nov. 2005.

[11] Boonchai Boonchu and Wanlop Surakampontorn, “CMOS voltage-mode analog multiplier,” 2006 IEEE International Symposium on Circuits and Systems, pp. 1989-1992, May 2006.

[12] Boonchai Boonchu, “Low-Voltage Low-Power Sub-Threshold CMOS Four-Quadrant Analogue Multiplier,” 2018 International Electrical Engineering Congress, pp. 316-319, March 2018.

[13] Chunhong Chen and Zheng Li, “A low-power CMOS analog multiplier,” IEEE Transactions on Circuits and Systems II, vol. 53, pp. 100-104, 2006.

[14] O. Oliaei and P. Loumeau, “A CMOS class AB current-multiplier,” IEEE International Symposium on Circuits and Systems (ISCAS), June. 1997.

[15] Wanlop Surakampontorn1 and Khanittha Kaewdang2,

"Development of Differential Amplifier Based the Second Generation Current Conveyors," ECTI Transactions on Electrical Engineering, Electronics, and Communications, vol. 10, no. 2, pp. 139-145, August 2012.

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